Audio Interface for the Zedboard

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1   Overview

This interface connects the ADAU1761 audio codec on the Zedboard to the Zynq PL. Audio signals can be received in stereo from the line in jack and/or transmitted to the headphone out jack. The design has originally been developed by Mike Field (alias hamster). In his design it is part of a system for filtering audio signals with the Zedboard (http://hamsterworks.co.nz/mediawiki/index.php/Zedboard_Audio).

We have extracted, modified and extended the audio interface part to provide an easy to use standalone IP core for using the audio capabilities on the Zedboard. The main differences to hamster's design are:

- ready to use, standalone IP block (filters and switches removed, new top level file)

- improved interface (synchronized to 100 MHz system clock)

- ported to Vivado

- added testbench to test line in and headphone out

- improved documentation

The source files can be downloaded from Git Hub:

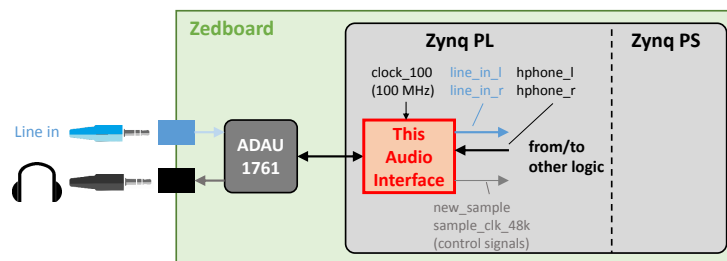https://github.com/ems-kl/zedboard_audio

Fig. 1: The audio interface

2   How to use the audio interface

24 bit audio samples are read from the blue line in jack and are provided by line_in_l and _r to the FPGA logic. Audio samples can be passed to the ADAU1761 for output on the black headphone jack via the hphone_l and _r input signals. New samples (from line in) are signalized by new_sample = 1 or the rising edge of sample_clk_48k. Note, that after a new sample from line in has been signalized, the design accepts a sample for output at the headphone within nearly one sample period (i.e. within approx. 2000 clock cycles).

Headphone input signals hphone_l and _r are simultaneously sampled on valid signal of channel l (hphone_l_valid). The valid signal of channel r (hphone_r_valid_dummy) is discarded and is only there to be able to easily form an AXIS interface in the Vivado Packager. For mono operation use channel l. Detailed waveforms are shown in Fig. 3.

Interface signals summary:

- **clk_100**: apply a 100 MHz clock

- **line_in_l** and **_r**: provide 24 bit data from the line in for left and right channel

- **hphone_l** and **_r**: input for 24 bit headphone data, valid data is signalized by **hphone_l_valid** = 1

- **new_sample**: high for one clock cycle, if a new sample has arrived (on rising edge of sample_clk_48)

- **sample_clk_48k**: clock synchronous to sample rate (48kHz), useful e.g. for sample rate conversion

A testbench is provided (audio_testbench.vhd), which can be used for testing or as a top level module for a reference design. Two tests are available: a simple loopback, which routes the line in signal directly to the headphone and a sawtooth generator for headphone output. To switch between the testmodes the corresponding code block has to be commented out in audio_testbench.vhd.

Furthermore two bitstream files are available (one for each testbench mode) for quick evaluation (generated with Vivado 2013.4). The applied board settings are shown below in Fig. 2.
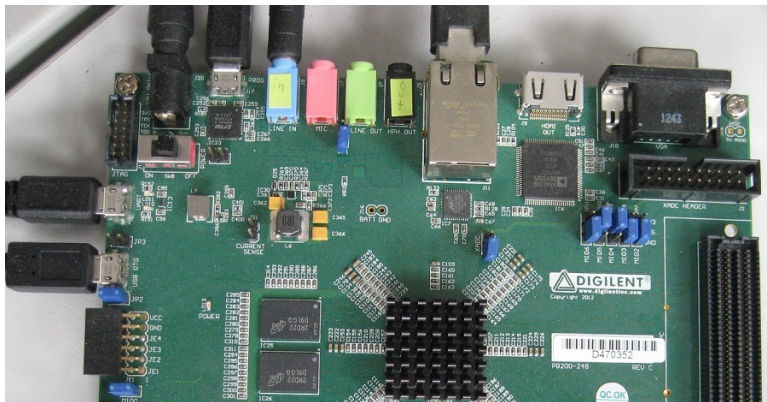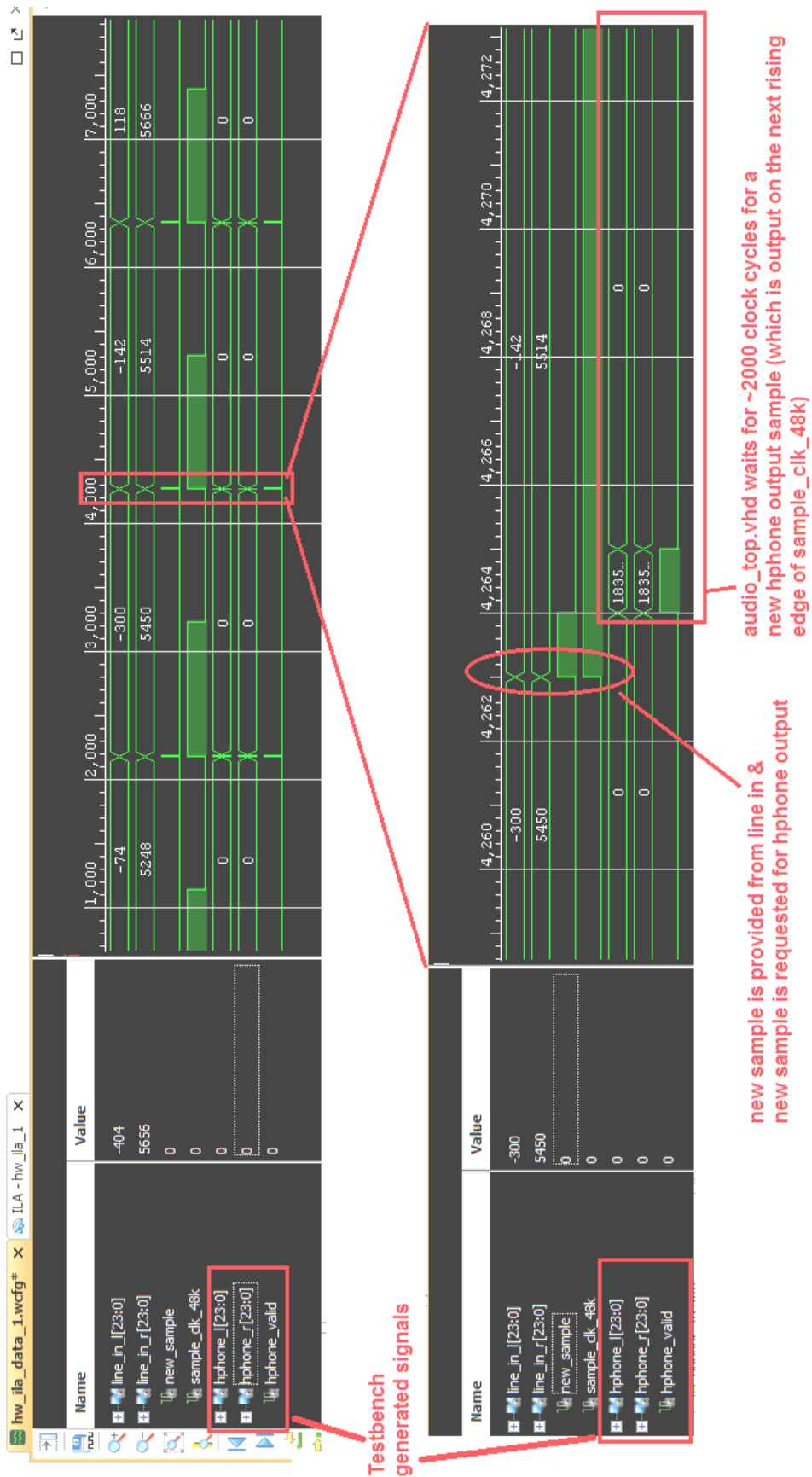

Fig. 2: Zedboard jumper settings

Fig. 3: Waveforms to clarify the usage of the IP core

3   Implementation Details

Configuration data for the ADAU1761 is provided via I2C by a small controller. Transmission of audio data to the ADAU1761 is accomplished by I2S. The interface to the FPGA logic is provided at 100 MHz (clk_100). Since the interior clock of the original Hamsterworks design works at 48 MHz, clock domain crossing (CDC) is required. The ADAU1761 chip is clocked by this design at $48\text{MHz}/2 = 24$ MHz.
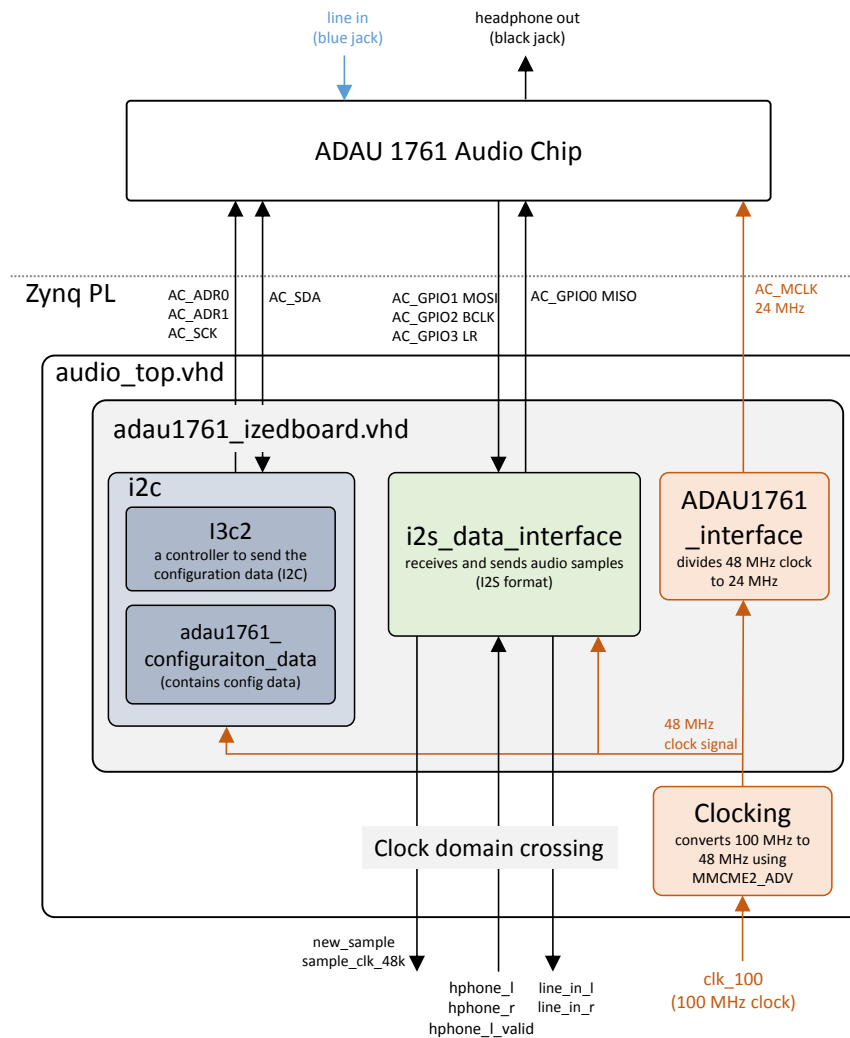

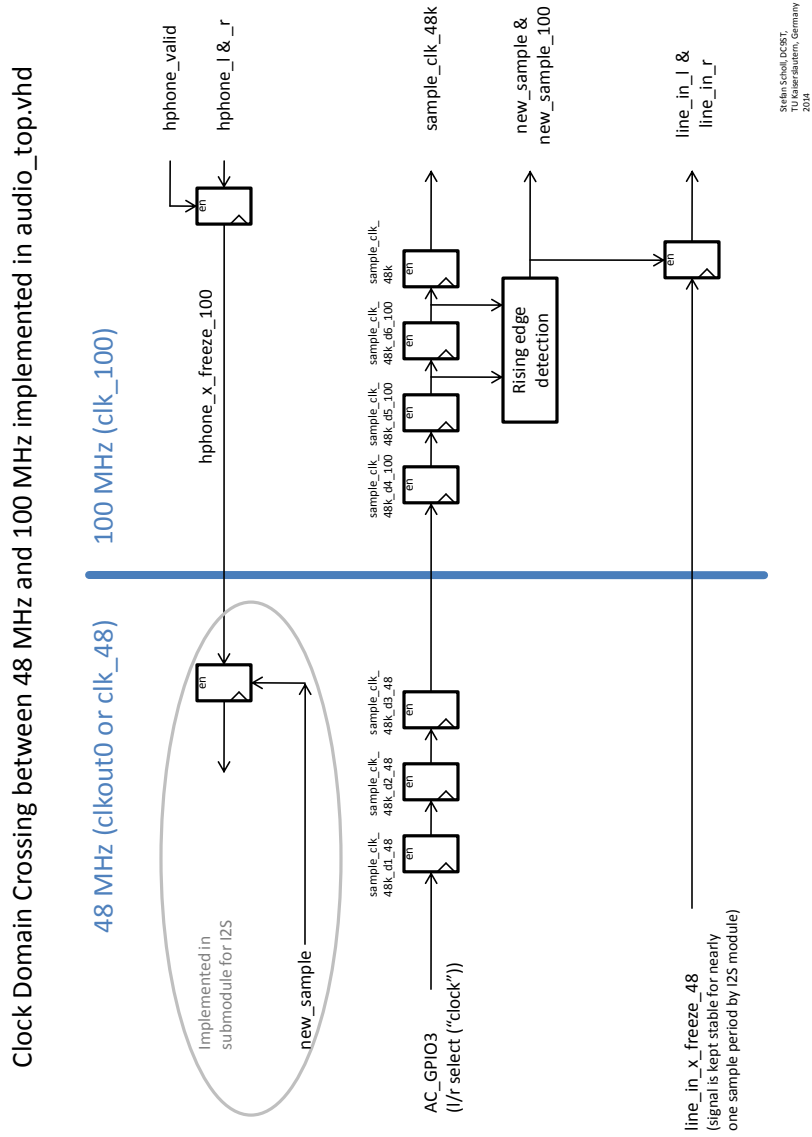Fig. 4: Block diagram overview (block names correspond to vhdl file names)

Fig. 5: Clock domain crossing between audio (48 MHz) and interface (100 MHz) clock domain