A counter-based read circuit tolerant to process variation for low-voltage operating STT-MRAM

Yohei Umeki, Koji Yanagida, Hiroaki Kurotsu,
Hiroto Kitahara, Haruki Mori, Shintaro Izumi,
Masahiko Yoshimoto,Hiroshi Kawaguchi
Graduate School of System Informatics Kobe University
1-1 Rokkodai, Nada, Kobe, 657-8501 Japan
umeki@cs28.cs.kobe-u.ac.jp

Shusuke Yoshimoto
The Institute of Scientific and Industrial Research,
Osaka University
8-1, Mihogaoka, Ibaraki, Osaka 567-0047 Japan

Koji Tsunoda, Toshihiro Sugii
Low-Power Electronics Association and Project (LEAP)
7 West, 16-1 Onogawa, Tsukuba, 305-8569 Japan

I. INTRODUCTION

The capacity of embedded memory on LSIs has kept increasing. It is important to reduce the leakage power of embedded memory for low-power LSIs. In fact, the ITRS predicts that the leakage power in embedded memory will account for 40% of all power consumption by 2024 [1]. A spin transfer torque magneto-resistance random access memory (STT-MRAM) is promising for use as non-volatile memory to reduce the leakage power. It is useful because it can function at low voltages and has a lifetime of over 10^{16} write cycles [2]. In addition, the STT-MRAM technology has a smaller bit cell than an SRAM. Making the STT-MRAM is suitable for use in high-density products [3–7]. The STT-MRAM uses magnetic tunnel junction (MTJ). The MTJ has two states: a parallel state and an anti-parallel state. These states mean that the magnetization direction of the MTJ's layers are the same or different. The directions pair determines the MTJ's magneto-resistance value. The states of MTJ can be changed by the current flowing. The MTJ resistance becomes low in the parallel state and high in the anti-parallel state. The MTJ potentially operates at less than 0.4 V [8]. In other hands, it is difficult to design peripheral circuitry for an STT-MRAM array at such a low voltage. In this paper, we propose a counter-based read circuit that functions at 0.4 V, which is tolerant of process variation and temperature fluctuation.

II. CONVENTIONAL AND PROPOSED READ CIRCUITS

Fig. 1 shows the conventional read circuit at a supply voltage of 0.4 V [8]. The load transistor draws a load current (I_{load}) to an MRAM cell. The node "S" corresponds to an input voltage to the sense amplifier. The voltage of the node "S" is determined by the datum of the target cell; that is, it is a balance between I_{load} and the readout current (I_P or I_{AP}). As shown in the figure, at the TT corner, this read circuit makes a 130-mV difference between the parallel and anti-parallel states. However, at the FS corner, it results in 40 mV, which implies that the conventional read circuit cannot read out correctly at any process corner. In addition, temperature fluctuation makes it difficult to read a datum accurately.

Fig. 2 shows the 1-Mb STT-MRAM macro with the proposed read circuit. The proposed read circuit converts a bitline voltage, which depends on a target cell datum, to a digital value. Two reference cell columns are further added. In the read operation, the bitline voltages of the reference cell columns are converted to digital values. Then, the threshold value is set as an average one of them. The target cell's bitline voltage is also converted to a digital value and compared with the threshold value. The output datum is distinguished by comparing to the threshold value. The detailed proposed read circuit is shown on the right side of Fig. 2, which is comprised of two circuits: a dynamic load circuit and a voltage-controlled oscillator with a counter. The dynamic load circuit changes its load curve over time, and the bitline voltage is digitized as a counting number of the oscillations. Because the frequency of the voltage-controlled oscillator depends on the voltage of the node "S", the datum of the target cell can be distinguished by the counter value.

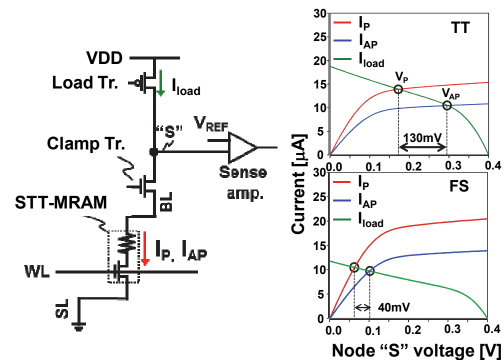

Fig. 1 Conventional read circuit and current characteristics.

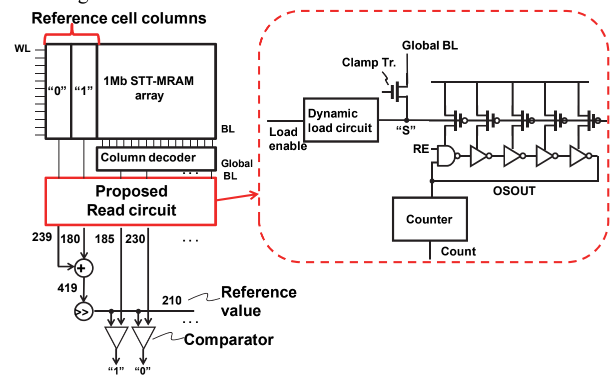

Fig. 2. Bitline voltage digitizing circuit.

Fig. 3 shows the dynamic load circuit. The dynamic load circuit has a negative resistance circuit and a four boost-gated nMOSes. The load curves on the left side in Fig. 4 correspond to variations in sequentially switching the LE signals from “0000” to “1111”. The right one shows the current characteristics in a case of LE<3:0>=“1001”. In the conventional circuit, I_{load} monotonically increased as the voltage of node “S” decreased. In contrast, in the proposed read circuit, the load current, I_{all}, has a local minimum value thanks to the negative resistance circuit. This proposed read circuit makes a larger voltage difference (H_{prop}) and hence a large oscillation counter value when the local minimum value is between I_P and I_{AP}.

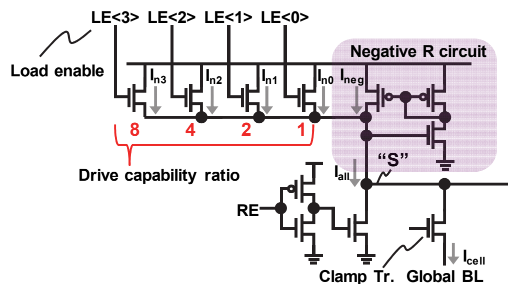

Fig. 3. Schematic of dynamic load circuit.

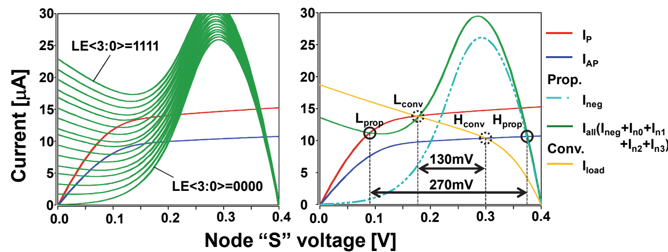

Fig. 4 Current characteristics of proposed read circuit.

III. Simulation Results

We simulated the proposed read circuit at the all process corners and on temperature conditions: –20 °C, 25 °C and 100 °C. For the MTJ, we set the MR ratio to 100%; the resistance are 3.5 kΩ in the parallel state, and 7 kΩ in the anti-parallel state. The operating voltage is 0.4 V. TABLE I show the count of the voltage-controlled oscillator. This result shows the proposed circuit is possible to distinguish the P and AP states even at the supply voltage of 0.4 V. TABLE II shows the energy consumption and the cycle time at the same voltage in read operation. In this simulation, the read operation was finished when the difference of the counts between the two states became ten.

TABLE I. Counts Of Voltage-Controlled Oscilaltor.

Process corner	Temperature(°C)	AP	P
TT	-20	98	122
	25	180	239
	100	237	387
FF	-20	261	359
	25	327	504
	100	144	425
FS	-20	88	119
	25	156	225
	100	146	304
SF	-20	85	99
	25	174	211
	100	298	412
SS	-20	30	34
	25	76	91
	100	172	234

TABLE II. Read Cycle Time And Energy Consumption.

Process corner	Temperature(°C)	Time[ns]	$Energy_{AP}$[pJ]	$Energy_P$[pJ]
TT	-20	666.67	2.14	2.59
	25	271.19	1.05	1.23
	100	106.67	0.60	0.66
FF	-20	163.27	0.85	1.01
	25	90.40	0.57	0.66
	100	56.94	0.56	0.65
FS	-20	516.13	1.95	2.47
	25	231.88	1.06	1.24
	100	101.27	0.71	0.78
SF	-20	1142.86	3.14	3.55
	25	432.43	1.50	1.72
	100	140.35	0.69	0.71
SS	-20	4000	7.11	8.26
	25	1066.67	2.61	3.09
	100	258.07	0.90	0.99

IV. Chip Implementation

We fabricated a 4-Mb STT-MRAM using a 65-nm process technology. Fig. 5 shows the layout of test chip and MTJ’s TEM micrograph. The area overhead of proposed circuit is 180 μm^2. The the area overhead of the proposed read circuit is merely 0.53%.

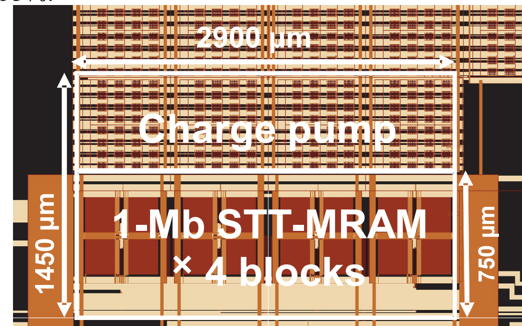

Fig. 5. Chip layout.

Acknowledgment

We would like to thank Toppan Technical Design Center Co., Ltd., for chip implementation. This work was performed as the “Ultra-Low Voltage Device Project” of the Low-power Electronics Association & Project (LEAP) funded and supported by METI and NEDO. Part of the device processing was performed by AIST, Japan.

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