A Wide-Operating Range Standard-Cell Based Memory in 28nm FD-SOI

Oskar Andersson, Babak Mohammadi, and Joachim Neves Rodrigues
Department of Electrical and Information Technology, Lund University, Lund, 221 00 Sweden
Email: {oskar.andersson, babak.mohammadi, joachim.rodrigues}@eit.lth.se

***Abstract*—This study presents an energy-efficient ultra-low voltage standard-cell based memory in 28 nm FD-SOI. The storage element (standard-cell latch) is replaced with a full-custom designed latch with 50 % less area. Error-free operation is demonstrated down to 450 mV @ 9 MHz. By utilizing body bias (BB) @ V_{DD} = 0.5 V performance spans from 20 MHz @ BB= 0 V to 110 MHz @ BB=1 V.**

I. Introduction

In the Internet of Things (IoT) era there is need for energy efficient ultra-low voltage circuits [1]. A well-established method to increase energy efficiency is to reduce the supply voltage (V_{DD}) and operate in the near-threshold (near-V_{th}) region, i.e., V_{DD} is in the vicinity of the threshold voltage (V_{th}) of the transistors [2]. However, with a scaled V_{DD}, traditional 6 transistor (6T) SRAM macros are no longer operational and other alternatives are required. One approach is to use full-custom SRAMs designed for near-V_{th} operational that use larger bitcells using additional transistors (8-14T) resulting in an increased area per bit. In addition, assist techniques for read- and/or write-operation is often used. This approach has been evaluated by several authors over time in different process nodes [3]–[5]. Another approach is to use a memory synthesized from standard-cells that use D-flip flops or latches as storage elements and read-logic implemented using CMOS multiplexers. These memories are larger than SRAMs for large memory capacities but have competitive area for capacities of a few kb [6]. Furthermore, by replacing the storage element by a full-custom cell creates a possibility to change the characteristics of the memory as the storage element accounts for $\sim\frac{2}{3}$ of total memory area. Thus, replacing a single standard-cell has a large impact of the overall memory.

II. Standard-cell based memory

A Standard-cell based memory (SCM) is an interesting alternative to an SRAM macro for small capacity storage arrays, e.g., register files, FIFOs, as they are highly configurable to specific needs with low engineering effort, i.e., word length, number of read/write ports, word count, read/write architecture [7]. Advantageously, SCMs are placed on the core rows and are thus closer to the logic, which reduces wire length and parasitic capacitance, which in turn, may lead to improved timing and lower energy dissipation. Furthermore, read logic implemented using standard CMOS multiplexers allows for voltage scaling down to the near-V_{th} region.

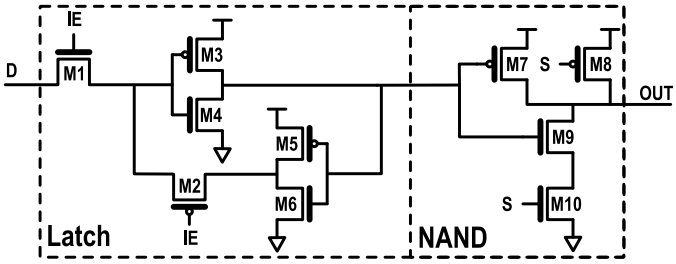

Fig. 1. Architecture of full-custom latch bitcell.

A. Proposed full-custom latch

A full-custom latch was designed based on the latch proposed in [6], and migrated from a 65 nm to a 28 nm FD-SOI process, see Fig. 1. By using a pass-transistor architecture instead of a conventional D-Latch in the standard-cell library the transistor count is reduced from 14 to 6 transistor in the storage element. Furthermore, the first multiplexer stage is integrated in the standard-cell to further reduce area impact, which leads to a total area reduction of 50 %. However, due to the voltage drop across M1 (inherently from NMOS devices being worse at passing logic '1') the write performance is degraded. In the 28 nm FD-SOI technology a wide-range body bias (BB) scheme allows for V_{th} tuning of the devices to mitigate the performance degradation.

III. Silicon Measurements

A prototype chip was manufactured using low-V_{th} (LVT) transistors in a 28 nm FD-SOI technology featuring an 8 kb standard-cell based memory with the proposed storage element organized as 256 words $\times$ 32 bits. A chip micrograph is shown in Fig. 2. A reference memory using standard-cell latches was also included to demonstrate the area reduction from using full-custom pass-transistor latches. The standard design occupies an area of $108 \times 216\,\mu\mathrm{m}^2$ and the full-custom latch design $108 \times 156\,\mu\mathrm{m}^2$, a reduction of 38 %. Correct functionality was verified using scan-chain interfaces and a built-in-self-test (BIST) structure.

A. Energy Dissipation and Maximum Operating Frequency

Figure 3 shows the measured maximum frequency and the average energy dissipation (normalized to the wordlength of the memory) when performing read and write-accesses for various V_{DD}. The results demonstrate performance when zero

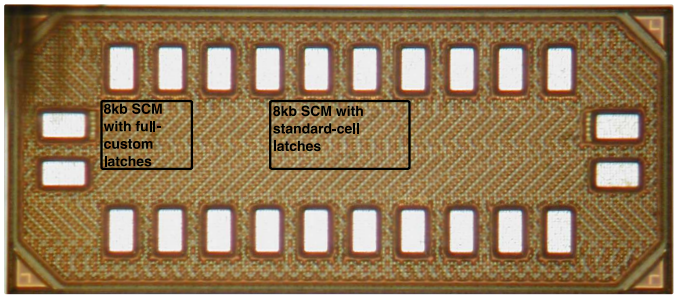

Fig. 2. Chip micrograph of the manufactured standard-cell memory.

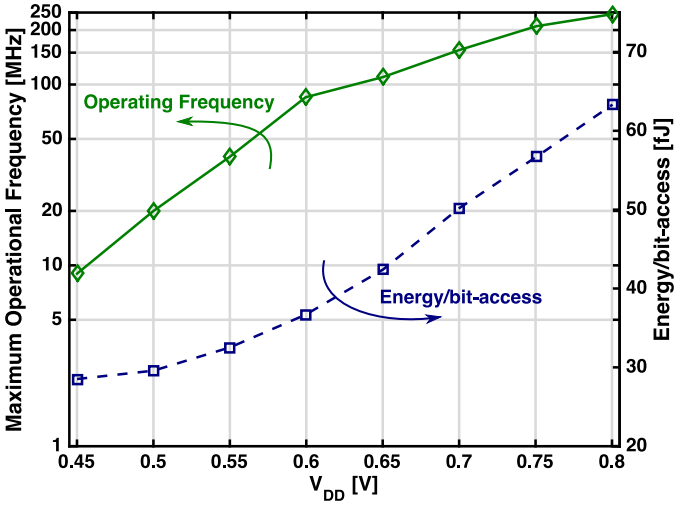

Fig. 3. Measured maximum operational frequency and energy dissipation at scaled V_{DD}.

body bias is applied. The lowest operational V_{DD} (V_{DDmin}), 0.45 V, is dictated by the retention voltage.

B. Effect of Body Bias

The effect of body bias is demonstrated from measurements at V_{DD} = 0.5 V with BB ranging from 0 V to 1 V, see Table I. An 5.5× performance gain is observed resulting in a performance span of 20 MHz to 110 MHz at no or marginal increase in energy dissipation.

IV. Comparison with the State of the Art

The manufactured memory is compared with manufactured 28 nm state-of-the-art memories, see Table II. It is seen that the proposed standard-cell based memory achieves the lowest average energy dissipation per bit-access and achieves the highest frequency at 600 mV. Even though the area of the storage element is reduced by 50 % compared to the vendor supplied standard-cell library latch, the area/bit including peripherals is still 10× larger than the 6T SRAM macro [8].

TABLE I
Chip performance @ $V_{\mathrm{DD}} = 0.5V$ showing the wide-dynamic range that body bias (BB) enables.

	BB = 0V	BB = 0.4V	BB = 1V
f [MHz]	20	56	110
$E_{\mathrm{bit-access}}$ [fJ]	29.6	29.6	38.5

TABLE II
Comparison with state-of-the-art memories in 28 nm.

	ISSCC'11 [8]	JSSC'14 [5]	**This work†**
Area/bit* [μm^2]	0.21	-	**2.06**
Bitcell	6T	10T	**6T Pass-Latch**
Memory size	128 kb	64 kb	**8 kb**
E_{min}/bit-access [fJ]	4375	35.9	**28.5**
V_{min} [mV]	600	350	**450**
f @ 600 mV [MHz]	20	13 (0.35 V)	**85**

*Including peripheral circuits. †Measurements performed with BB = 0 V.

V. Conclusions

An 8 kb standard-cell based memory with a full-custom storage element was presented. It was shown that by replacing a single standard-cell with a full-custom designed standard-cell optimized for area it is possible to reduce the area/bit by 38 %. In addition, the presented memory is 4× faster at 600 mV than a previously published SRAM macro and with orders of magnitude lower energy dissipation.

Acknowledgment

This work was kindly supported by Swedish Vetenskapsrådet (621-2011-4540) and Swedish VINNOVA Industrial Excellence Centre (SOS). The authors are grateful to STMicroelectronics for chip fabrication.

References

[1] S. Jain, S. Khare, S. Yada, V. Ambili, P. Salihundam, S. Ramani, S. Muthukumar, M. Srinivasan, A. Kumar, S. Gb, R. Ramanarayanan, V. Erraguntla, J. Howard, S. Vangal, S. Dighe, G. Ruhl, P. Aseron, H. Wilson, N. Borkar, V. De, and S. Borkar, "A 280mV-to-1.2V wide-operating-range IA-32 processor in 32nm CMOS," in *Proc. IEEE Internat. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb 2012, pp. 66–68.

[2] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, pp. 3–29, Jan 2012.

[3] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," *IEEE J. Solid-State Circuits*, pp. 680–688, March 2007.

[4] L. Chang, D. Fried, J. Hergenrother, J. Sleight, R. Dennard, R. Montoye, L. Sekaric, S. McNab, A. Topol, C. Adams, K. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in *Proc. Symp. VLSI Technol. Dig. Tech. Papers*, June 2005, pp. 128–129.

[5] F. Abouzeid, A. Bienfait, K. C. Akyel, A. Feki, S. Clerc, L. Ciampolini, F. Giner, R. Wilson, and P. Roche, "Scalable 0.35 V to 1.2 V SRAM Bitcell Design From 65 nm CMOS to 28 nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1499–1505, 2014.

[6] O. Andersson, B. Mohammadi, P. Meinerzhagen, , and J. Rodrigues, "A 35fJ/bit-access sub-V_{T} memory using a dual-bit area-optimized standard-cell in 65 nm CMOS," in *Proc. 40th Eur. Solid-State Circuits Conf.*, Sept 2014, pp. 243–246.

[7] P. Meinerzhagen, S. Sherazi, A. Burg, and J. Rodrigues, "Benchmarking of standard-cell based memories in the sub-V_{T} domain in 65-nm CMOS technology," *IEEE J. Emerg. Sel. Topic Circuits Syst.*, pp. 173–182, June 2011.

[8] M. E. Sinangil, H. Mair, and A. P. Chandrakasan, "A 28nm high-density 6T SRAM with optimized peripheral-assist circuits for operation down to 0.6V," in *Proc. IEEE Internat. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb 2011, pp. 260–262.