Design and Application of Integrated Multi-Sensor Electronics with Self-x Properties for Robust Intelligent Systems in Industry 4.0 and IoT Domains

Entwurf und Anwendung von integrierter Multisensorelektronik mit Self-x-Eigenschaften für robuste intelligente Systeme in den Bereichen Industrie 4.0 und IoT

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Abstract

The thesis presents a cost-effective approach to enhancing the autonomy and optimization capabilities of smart sensory electronic systems (SSES) through the integration of artificial intelligence (AI) at the lowest levels of automated test equipment (ATE). This integration aims to realize self-configuring, self-optimizing, and self-healing ("self-X") properties in SSES, leveraging the transformative power of machine learning to revolutionize traditional sensory systems. In the era of Industry 4.0, where the fusion of advanced digital technologies with the physical production and operational processes defines a new industrial revolution, the application of AI and machine learning in SSES represents a critical step forward in realizing intelligent, efficient, and highly adaptable manufacturing and production environments.

This work primarily focuses on electronic design automation (EDA) from the development of tuning knobs for enhanced adaptivity, through the advanced designing of extrinsic optimization techniques, culminating in the seamless integration of these methodologies on hardware specifically dedicated for the assessment and optimization of the chip. The implementation of a chip performance assessment unit on this hardware is crucial for enabling the development of self-X properties in SSES. The reconfigurable, fully differential indirect current-feedback instrumentation amplifier (CFIA) is intrinsically optimized using a single test sinusoidal signal stimulus and measures the total harmonic distortion (THD) at the output. Additionally, a power-monitoring module is integrated into the CFIA circuit to assess power consumption, ensuring a power-efficient and reliable configuration. The implemented assessment unit effectively manages data acquisition, THD computation via FFT, and executes an advanced optimization algorithm for dynamic system configuration, facilitating an adaptive and efficient data management and transmission protocol. The design of the architecture has been kept generic to ensure its easy integration with higher-level system designs, enhancing its applicability across diverse technological applications. Preliminary tests conducted on the fabricated chip, using the default configuration pattern from post-layout simulations, revealed an unacceptable performance behavior of the CFIA. Nevertheless, the proposed in-field optimization successfully restored the circuit's performance, resulting in a robust design that meets the performance achieved in the design phase. This architecture

resulted in a 34% increase in power efficiency while achieving a THD value of −72 dB with a 2 $V_{p\text{-}p}$ differential input signal at 1 MHz. Dynamic intrinsic optimization across a temperature range of −20°C to 40°C and a 25% reduction in supply voltage revealed the system's adaptability to process, voltage, and temperature (PVT) variations.

A novel experience replay particle swarm optimization (ERPSO) algorithm, embedded on Red Pitaya FPGA boards, acts as an AI agent for intrinsic in-field optimization of the CFIA. The proposed ERPSO algorithm expands the classical PSO selection process with an experience replay buffer (ERB) to reduce the likelihood of trapping in local minima. The ERB archives previously visited global best particles and uses an adaptive epsilon greedy method in velocity updating. The ERPSO algorithm's performance is verified using eight popular benchmarking functions. The evaluation of robust optimization for CFIA, using surrogate-based and archive-based methodologies, is conducted through simulation-based results due to timing constraints. Benchmark functions and direct application to CFIA highlighted this method's effectiveness in reducing the average expected error (AEE) and improving correlation metrics. This facilitated precise tuning of CFIA to achieve desired performance levels while effectively managing uncertainties and imperfections.

An evaluation of filter optimization using reconfigurable non-intrusive sensors provides a comprehensive examination of a novel approach to optimizing filter characteristics, particularly cutoff frequencies, through indirect measurements. The typical indirect measurement approach using regression models for the device under test (DUT) performance prediction is integrated with ERPSO for reconfigurable non-intrusive sensors. This work's novelty lies in optimizing the non-intrusive sensors by copying the DUT's tuning knobs, indirectly optimizing DUT performance without interrupting its operation. In-field optimization is based on low-cost sensor measurements, achieving a 92% correlation performance metric for regression tasks. The study also presents the filter's dynamic performance under temperature variations, illustrating robustness. The filter recalibrates with a maximum 3% discrepancy from intended cutoff frequencies, emphasizing its resilience and optimization strategy. A reinforcement learning approach further addressed layout-induced deviations, reducing the need for extensive physical measurements and adapting to fabricated chips.

The practical application of a reconfigurable analog front-end with self-X properties

for the tunnel magneto-resistance (TMR) sensor, provided by Sensitec, demonstrates seamless integration with higher system hierarchies. Configuration bits derived from the optimization algorithm highlight the integration of theoretical and algorithmic progress with practical implementation.

The research successfully demonstrates the potential of AI and machine learning to enhance the autonomy and optimization of SSES. Future work will focus on uninterrupted optimization processes, such as implementing real-time operating systems (RTOS) or time-triggered embedded systems (TTES) to interleave calibration and measurement tasks. Additionally, further investigations will explore the intrinsic evaluation of non-intrusive sensor-based indirect measurement techniques and the application of reinforcement learning methods to reduce the need for extensive physical measurements, thus enhancing the efficiency and robustness of smart sensory electronic systems. These future directions aim to provide more robust, adaptable, and cost-effective solutions for next-generation industrial applications.

Kurzfassung

In dieser Arbeit wird ein kosteneffizienter Ansatz zur Verbesserung der Autonomie und der Optimierungsfähigkeiten intelligenter sensorischer elektronischer Systeme (SSES) durch die Integration von künstlicher Intelligenz (KI) auf den untersten Ebenen der automatisierten Testausrüstung (ATE) vorgestellt. Diese Integration zielt darauf ab, selbstkonfigurierende, selbstoptimierende und selbstheilende ("self-X") Eigenschaften in SSES zu realisieren und die transformative Kraft des maschinellen Lernens zu nutzen, um traditionelle sensorische Systeme zu revolutionieren. Im Zeitalter von Industrie 4.0, in dem die Verschmelzung fortschrittlicher digitaler Technologien mit physischen Produktions- und Betriebsprozessen eine neue industrielle Revolution definiert, stellt die Anwendung von KI und maschinellem Lernen in SSES einen entscheidenden Schritt nach vorn bei der Realisierung intelligenter, effizienter und hochgradig anpassungsfähiger Fertigungs- und Produktionsumgebungen dar.

Diese Arbeit konzentriert sich in erster Linie auf die elektronische Entwurfsautomatisierung (EDA), von der Entwicklung von Abstimmknöpfen für eine verbesserte Anpassungsfähigkeit über die fortschrittliche Gestaltung von extrinsischen Optimierungstechniken bis hin zur nahtlosen Integration dieser Methoden in Hardware, die speziell für die Bewertung und Optimierung des Chips vorgesehen ist. Die Implementierung einer Chip-Leistungsbewertungseinheit auf dieser Hardware ist entscheidend für die Entwicklung von Self-X-Eigenschaften in SSES. Der rekonfigurierbare, vollständig differentielle, indirekte stromrückgekoppelte Instrumentenverstärker (CFIA) wird anhand eines einzigen sinusförmigen Test-Signalstimulus optimiert und misst die gesamte harmonische Verzerrung (THD) am Ausgang. Zusätzlich ist ein Leistungsüberwachungsmodul in den CFIA-Schaltkreis integriert, um den Stromverbrauch zu bewerten und eine energieeffiziente und zuverlässige Konfiguration zu gewährleisten. Die implementierte Bewertungseinheit verwaltet effektiv die Datenerfassung, die THD-Berechnung mittels FFT und führt einen fortschrittlichen Optimierungsalgorithmus für die dynamische Systemkonfiguration aus, der ein adaptives und effizientes Datenmanagement und Übertragungsprotokoll ermöglicht. Das Design der Architektur wurde generisch gehalten, um eine einfache Integration in übergeordnete Systemdesigns zu gewährleisten und die Anwendbarkeit in verschiedenen technologischen Anwendungen zu verbessern. Vorläufige Tests, die auf

dem hergestellten Chip unter Verwendung des Standardkonfigurationsmusters aus Post-Layout-Simulationen durchgeführt wurden, zeigten ein inakzeptables Leistungsverhalten des CFIA. Durch die vorgeschlagene Optimierung im Feld konnte die Leistung der Schaltung jedoch erfolgreich wiederhergestellt werden, was zu einem robusten Design führte, das die in der Entwurfsphase erreichte Leistung erfüllt. Diese Architektur führte zu einer Steigerung der Leistungseffizienz um 34% bei einem THD-Wert von -72 dB mit einem 2 $V_{p\text{-}p}$ Differenzeingangssignal bei 1 MHz. Eine dynamische intrinsische Optimierung über einen Temperaturbereich von 20 bis 40 °C und eine Verringerung der Versorgungsspannung um 25% zeigte die Anpassungsfähigkeit des Systems an Prozess-, Spannungs- und Temperaturschwankungen (PVT).

Ein neuartiger ERPSO-Algorithmus (Experience Replay Particle Swarm Optimization), der in Red Pitaya FPGA-Boards eingebettet ist, fungiert als KI-Agent für die Optimierung des CFIA in der Praxis. Der vorgeschlagene ERPSO-Algorithmus erweitert den klassischen PSO-Auswahlprozess um einen Erfahrungswiedergabepuffer (ERB), um die Wahrscheinlichkeit des Einfangens in lokalen Minima zu verringern. Der ERB archiviert zuvor besuchte global beste Partikel und verwendet eine adaptive Epsilon-Greedy-Methode bei der Geschwindigkeitsaktualisierung. Die Leistung des ERPSO-Algorithmus wird anhand von acht gängigen Benchmarking-Funktionen überprüft. Die Bewertung der robusten Optimierung für CFIA unter Verwendung von surrogat- und archivbasierten Methoden erfolgt aufgrund zeitlicher Beschränkungen durch simulationsbasierte Ergebnisse. Benchmark-Funktionen und die direkte Anwendung auf CFIA haben die Effektivität dieser Methode bei der Reduzierung des durchschnittlich erwarteten Fehlers (AEE) und der Verbesserung der Korrelationsmetriken hervorgehoben. Dies erleichterte die präzise Abstimmung von CFIA, um die gewünschten Leistungsniveaus zu erreichen und gleichzeitig Unsicherheiten und Unzulänglichkeiten effektiv zu bewältigen.

Eine Bewertung der Filteroptimierung mit rekonfigurierbaren nicht-intrusiven Sensoren bietet eine umfassende Untersuchung eines neuartigen Ansatzes zur Optimierung von Filtereigenschaften, insbesondere von Grenzfrequenzen, durch indirekte Messungen. Der typische Ansatz der indirekten Messung unter Verwendung von Regressionsmodellen für die Vorhersage der Leistung des zu testenden Geräts (DUT) wird in ERPSO für rekonfigurierbare nichtintrusive Sensoren integriert. Die Neuheit dieser Arbeit liegt in

der Optimierung der nicht-intrusiven Sensoren durch Kopieren der Abstimmknöpfe des Prüflings, wodurch die Leistung des Prüflings indirekt optimiert wird, ohne seinen Betrieb zu unterbrechen. Die Vor-Ort-Optimierung basiert auf kostengünstigen Sensormessungen und erreicht eine 92%-Korrelationsleistungsmetrik für Regressionsaufgaben. In der Studie wird auch die dynamische Leistung des Filters bei Temperaturschwankungen dargestellt, um die Robustheit zu veranschaulichen. Der Filter rekalibriert sich mit einer maximalen Abweichung von 3% von den beabsichtigten Grenzfrequenzen, was seine Widerstandsfähigkeit und Optimierungsstrategie unterstreicht. Ein Ansatz des verstärkten Lernens befasst sich darüber hinaus mit layoutbedingten Abweichungen, wodurch sich die Notwendigkeit umfangreicher physikalischer Messungen verringert und eine Anpassung an gefertigte Chips möglich wird.

Die praktische Anwendung eines rekonfigurierbaren analogen Frontends mit Self-X-Eigenschaften für den Tunnelmagnetowiderstandssensor (TMR), der von Sensitec bereitgestellt wurde, zeigt die nahtlose Integration in höhere Systemhierarchien. Aus dem Optimierungsalgorithmus abgeleitete Konfigurationsbits verdeutlichen die Integration von theoretischen und algorithmischen Fortschritten mit der praktischen Umsetzung.

Die Forschung demonstriert erfolgreich das Potenzial von KI und maschinellem Lernen zur Verbesserung der Autonomie und Optimierung von SSES. Zukünftige Arbeiten werden sich auf ununterbrochene Optimierungsprozesse konzentrieren, wie z. B. die Implementierung von Echtzeit-Betriebssystemen (RTOS) oder zeitgesteuerten eingebetteten Systemen (TTES), um Kalibrierungs- und Messaufgaben miteinander zu verzahnen. Darüber hinaus werden weitere Untersuchungen die intrinsische Bewertung von nicht-intrusiven sensorgestützten indirekten Messtechniken und die Anwendung von Methoden des Reinforcement Learning erforschen, um den Bedarf an umfangreichen physikalischen Messungen zu verringern und so die Effizienz und Robustheit intelligenter sensorischer elektronischer Systeme zu verbessern. Diese zukünftigen Richtungen zielen darauf ab, robustere, anpassungsfähigere und kostengünstigere Lösungen für industrielle Anwendungen der nächsten Generation bereitzustellen.

Erklärung

Hiermit versichere ich, dass ich die vorliegende Arbeit selbst angefertigt und verfasst habe und alle benutzen Hilfsmittel in der Arbeit angegeben habe.

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List of Abbreviations

ML Machine Learning

AI Artificial Intelligence

CPS Cyber-Physical Systems

IoT Internet of Things

IIoT Industrial Internet of Things

SoC System-on-Chip

SiP System-in-Package

CMOS Complementary Metal-Oxide-Semiconductor

ITRS International Technology Roadmap for Semiconductors

IRDS International Roadmap for Devices and Systems

AFE Analog Front End

SSE Smart Sensory Electronics

ICs Integrated Circuits

EDA Electronic Design Automation

PVT Process-Voltage-Temperature

EHW Evolvable Hardware

EP Evolutionary Processing Unit

SLM Silicon Lifecycle Management

PPAC Power, Performance, Area, and Cost

DUT Device Under Test

TK Tuning Knobs

AFEX Analog Front End with Self-X Properties

ATE Automatic Test Equipment

PSO Particle Swarm Optimizer

SSES Smart Sensory Electronic Systems

FPTA Field Programmable Transistor Array

FPMA Field Programmable Medium-Granular Mixed-Signal Array

USIX Universal Sensor Interface with Self-X Properties

IF Intermediate Frequency

GA Genetic Algorithm

FPAA Field Programmable Analog Array

CAB Configurable Analog Block

SPICE Simulation Program with Integrated Circuit Emphasis

DSP Digital Signal Processor

FPGA Field-Programmable Gate Array

OTA-C Operational Transconductance Amplifier-Capacitor

TMR Tunnel Magnetoresistance

BIST Built-In Self-Test

ANN Artificial Neural Network

CFIA Current Feedback Instrumentation Amplifier

EA Evolutionary Algorithm

ENOB Effective Number of Bits

GPR Gaussian Process Regression

IM Indirect Measurement

SSE Smart Sensory Electronics

PSO Particle Swarm Optimization

ERPSO Experience Replay Particle Swarm Optimizer

LDW-PSO Linearly Decreasing Inertia Weight Particle Swarm Optimization

LAC-PSO Linearly Varying Acceleration Coefficients Particle Swarm Optimization

SPSO Standard Particle Swarm Optimizer

THD Total Harmonic Distortion

ADC Analog-to-Digital Converter

DAC Digital-to-Analog Converter

ICMR Input Common-Mode Range

GBW Gain-Bandwidth Product

SNR Signal-to-Noise Ratio

DDF Differential-Difference Amplifier

CMRR Common-Mode Rejection Ratio

CMFB Common-Mode Feedback Amplifier

PMM Power Monitoring Module

CSR Current-Sense Resistor

FFT Fast Fourier Transform

VUE Velocity Update Equation

ERB Experience Replay Buffer

BMR Benchmarking Functions

RFR Random Forest Regressor

NS Non-Intrusive Sensors

PMOS P-channel Metal-Oxide-Semiconductor

NMOS N-channel Metal-Oxide-Semiconductor

TSC Temperature Sensing Core

CCO Current-Controlled Oscillator

BGR Bandgap Reference

PTAT Proportional to Absolute Temperature

PSRR Power Supply Rejection Ratio

BJT Bipolar Junction Transistor

MPC Multi-Project Chip

RF DAC Radio Frequency Digital-to-Analog Converter

RF ADC Radio Frequency Analog-to-Digital Converter

DRAM Dynamic Random-Access Memory

AXI Advanced eXtensible Interface

PCB Printed Circuit Board

SPI Serial Peripheral Interface

MSB Most Significant Bit

MC Monte Carlo

WC Worst-Case

PM Phase Margin

FTD Frequency-to-Digital Converter

DSS Digital Signal Synthesizer

RC Resistor-Capacitor

RTOS Real-Time Operating System

TTES Time-Triggered Embedded System

RMSE Root Mean Square Error

AEE Average Expected Error

MAE Mean Absolute Error

FoM Figure of Merit

VID Differential Input Voltage

AC Alternating Current

DSO Digital Storage Oscilloscope

LPF Low Pass Filter

Chapter 1

Introduction

The integration of machine learning (ML) and artificial intelligence (AI) with other emerging technologies, such as cyber-physical systems, big data analytics, cloud computing, and the industrial internet of things (I(I)oTs), is driving the transformation of the industrial domain. This transformation, commonly referred to as Industry 4.0, represents a new era of industrial revolution [1–5]. At the core of Industry 4.0 is the collection, analysis, and interpretation of data generated by I(I)oTs devices, which are increasingly being employed across various industries, including manufacturing, logistics, and transportation. A critical requirement for the success of Industry 4.0 is the development of accurate and reliable sensors and sensory electronics [5,6]. These sensors are responsible for collecting, processing, and transmitting data for further procedures. They play a vital role in capturing physical, chemical, and environmental information, enabling informed decision-making and process optimization.

Concurrently, advancements in integration technologies, such as monolithic systems-on-chip (SoC) and heterogeneous system-in-package (SiP) architectures [7, 8], are also enhancing the capabilities of computing systems, sensors, and sensory systems. Both traditional and innovative computing systems, drawing inspiration from biological nervous systems or neural networks, require efficient interfacing with a growing range of sensors while adhering to metrology constraints. The continuous progress in CMOS node technology, aligned with the 'More Moore' extension outlined by the 2015 International Technology Roadmap for Semiconductors (ITRS) [8] and the 2021 Edition of the International Roadmap for Devices and Systems (IRDS) [7], significantly contributes to the advancement of digital systems. However, the adoption of the latest node in analog

and mixed-signal circuits, particularly those involved in interfacing with sensor signals, often lags due to various technical challenges. Several studies have highlighted these difficulties [9, 10]. The realization of analog front ends (AFEs) that possess the necessary attributes of accuracy, robustness, and flexibility plays a pivotal role in ensuring the overall system quality and effectiveness. The development of such AFEs demands substantial design expertise both for chips in SiP and cells in SoC realizations.

1.1 Impact of Static and Dynamic Variations on AFEs

The performance of smart sensory electronics (SSEs) is strongly influenced by static and dynamic variations. These include irreversible effects such as aging [11, 12]. Static variations, particularly in advanced-node complementary metal oxide semiconductors (CMOS), arise from local (random/stochastic) and global (systematic) mismatches among chip devices [13]. These discrepancies can be attributed to imperfections in the manufacturing process, such as limitations in lithography resolution that cause deviations in device size, gate oxide thickness profiles affecting transistor threshold voltage, and variations in electron and hole mobility that ultimately impact MOS I-V characteristics [14]. Additionally, the application of mechanical stress to the chip during the die molding process, induced by packaging and assembly of integrated circuits (ICs), can lead to significant static mismatches in chip device characteristics [15]. Dynamic variations, especially, the reversible type, result from environmental fluctuations, changes in power supply voltage, as well as thermal drift caused by self-heating and temperature gradients arising from non-uniform power dissipation in ICs [16]. These variations are more pronounced in densely packed transistors in advanced node technology and SoC designs [17]. The reversible dynamic performance and static process variations can be effectively modeled using foundry process design kits (PDK), enabling evaluation through circuit simulation with electronic design automation (EDA) tools across various process corners and variations in voltage and temperature, commonly referred to as Process-Voltage-Temperature (PVT) variation. Modeling and predicting the impact of aging on circuit performance and ensuring long-term reliability remain significant challenges [18]. This is of utmost importance when assessing and implementing robust and reliable circuits for critical applications in real-world operating

conditions throughout the lifecycle of the integrated circuit (IC) [19].

1.2 Performance Optimization and Self-X in Industry 4.0

A high yield and performance exceeding targeted specifications can be achieved by designing a circuit surpassing the minimum performance requirements. By incorporating sufficient margins in the design, the actual operating point of the circuit can consistently fall within the acceptable performance range, irrespective of the PVT variations. However, this overdesigned circuit typically compromises other circuit characteristics of lesser importance for a specific application. For instance, the temperature coefficient and line sensitivity are critical circuit parameters in a high-precision voltage or current reference circuit. Therefore, designers may trade-off circuit area and power consumption to attain a low-temperature coefficient and minimal line sensitivity, disregarding PVT variations [20].

Extensive research has been conducted to find a more optimal trade-off among circuit characteristics, considering that attaining excessive performance margins may not always be practical. The concept of evolvable hardware (EHW) has been introduced as one of the robust approaches for addressing harsh environmental conditions in various domains, such as space [21]. EHW refers to configurable electronic hardware that can be self-configured using biologically inspired ML and AI techniques such as metaheuristic optimization algorithms [22, 23]. The evolutionary processing unit (EP) [24] autonomously reconfigurable the EHW to enable self-X properties, including including self-monitoring, -calibration[1], -trimming, -repair, -configuration, and -optimization. Figure 1.1 illustrates the block diagram of the sensory electronics with self-X features. Within this diagram, the assessment unit plays a crucial role in evaluating the system's performance. It accomplishes this by utilizing the optimization solutions and providing signals stimuli while measuring the output response under the control of the optimization unit.

The self-X methodology presents benefits by facilitating the calibration of sensory electronics systems even after chip packaging. This approach aims to achieve a more

[1]In the context of this thesis, for simplicity, the term "calibration" is used to describe the compensation for PVT variations through the utilization of reconfigurable tuning knobs. Conversely, as per the DIN 1319 standard [25], "trimming" refers to the modification of the equipment or hardware by utilizing reconfiguration resources in response to observed deviations. This distinction between calibration and trimming also extends to corresponding self-X activities.

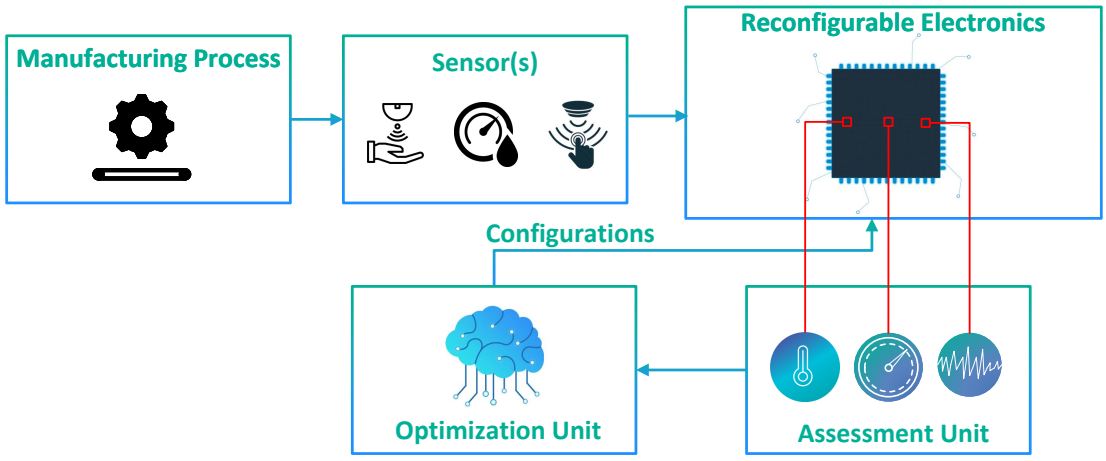

Figure 1.1: Block diagram of smart sensory electronics as lowest level of self-X hierarchy.

optimal trade-off among circuit characteristics by minimizing the area and power consumption overheads of the calibration/tuning circuit. The Industry 4.0 paradigm highlights the need for self-X capabilities, which are essential for ensuring the reliability and performance of smart sensory electronics. These capabilities enable a higher level of control and coordination across the entire value chain of products [26]. Moreover, the technology and sensor trends roadmaps released by the Association for Sensors and Measurement (AMA) and the User Association of Automation Technology in Process Industries (NAMUR) have both highlighted the importance of integrating sensory electronics enriched with self-X properties [6, 27]. This integration plays a crucial role in guaranteeing reliability, robustness, and adaptability across diverse applications, particularly within the demanding contexts of Industry 4.0 and other settings characterized by harsh environmental conditions [24]. Furthermore, it contributes a important role in enabling enhanced control and coordination throughout the entirety of the product chain [28].

Despite ongoing research on calibration/tuning circuits for analog circuits, the development of robust and reliable sensors and sensory electronics capable of operating in harsh environments is still necessary. This requires leveraging the potential offered by modern ML and AI techniques under the pyramid of Industry 4.0. Implementing self-monitoring, self-calibration, and data visualization at different levels of the self-X hierarchy can enhance the overall system performance and reliability. The focus is designing suitable electronics, the lowest and most critical level in a self-X hierarchy [5] (refer to Figure 1.2). Integrated solutions, in particular, can greatly benefit from adopting this

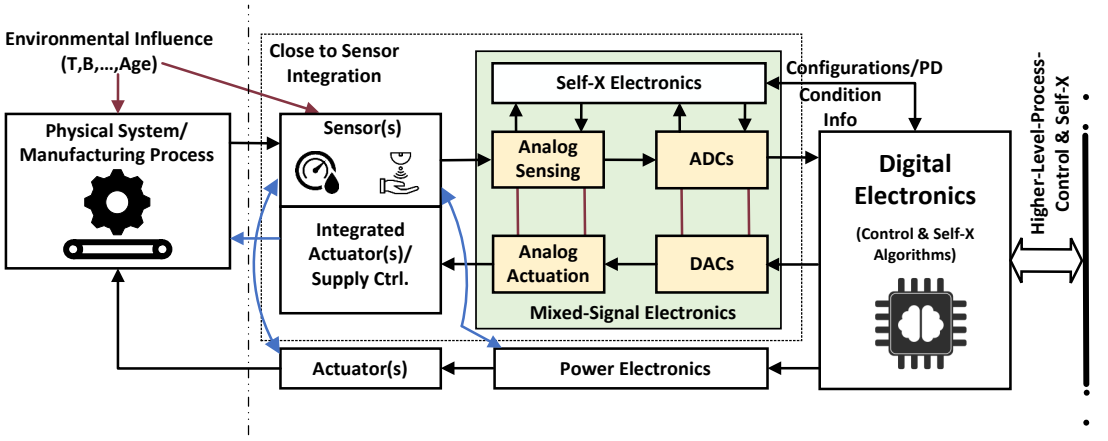

Figure 1.2: Sensor electronics with Self-X functionality includes the sensor element [5].

approach. Instead of costly individual calibration of systems, integrated solutions incorporate redundancy, reconfiguration, and correction features. These features are based on adaptation or learning/optimization techniques at different levels of abstraction. Numerous industrial examples, such as the Synopsys research and the previous work of Moortec, utilize Silicon Lifecycle Management (SLM) technology. This involves the implementation of in-built sensing devices and corresponding control loops within complex chips (SoCs), which facilitate long-term data collection [29–33]. Figure 1.3 illustrates Synopsys' goal of implementing self-monitoring, self-calibration, and data visualization at various levels of the self-X hierarchy.

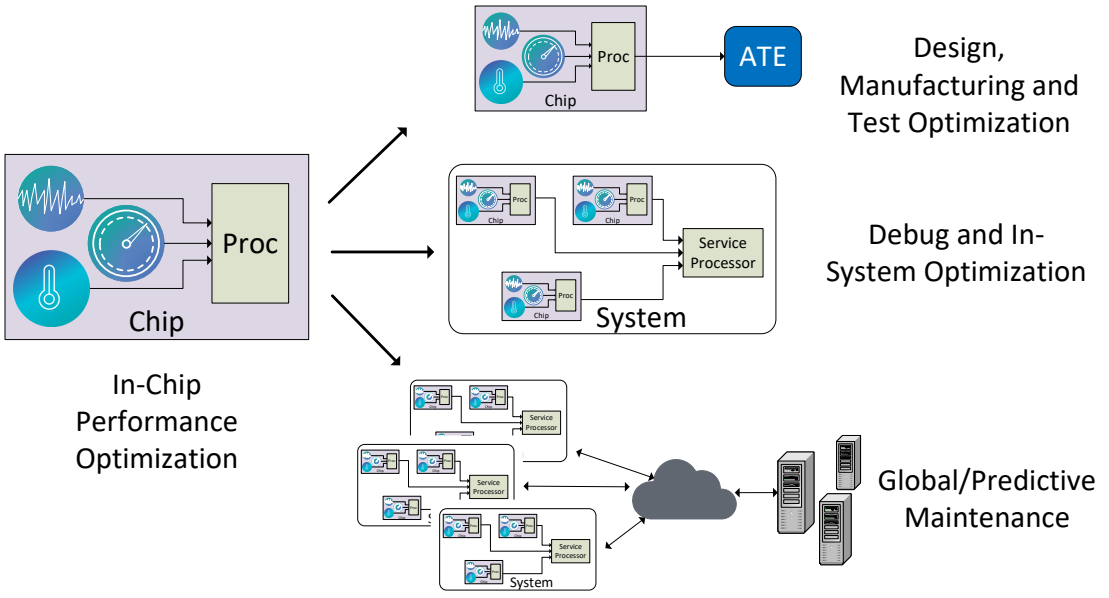

Figure 1.3: Vision to expand the lowest level of self-X hierarchy [33].

Transitioning from the conceptual phase of self-X sensory electronics to their practical

implementation within the framework of Industry 4.0 presents a variety of challenges. The primary hurdle lies in the intricacy associated with the optimization of circuit characteristics in an overdesigned system. While such a system offers advantages in terms of performance, it can impose significant trade-offs in power consumption and circuit area. Additionally, the introduction of observer imperfection further compounds the complexity of these challenges, an aspect this thesis aims to address.

In response to these challenges, this work aims to strike a balance between circuit characteristics, observer imperfection, and the inherent complexity of integrated systems. The goal is to design systems that are flexible and resilient, ensuring reliable performance under various environmental conditions, and simplifying the processes of observation and calibration. A key consideration in this work is the cost associated with performance measurement methods. Hence, exploring low-cost, indirect measurement methods serves as a significant part of this research.

This work contributes towards designing a system that not only offers high performance but also efficiently manages observer imperfection and complexity. Navigating through the intricate aspects of circuit design, the focus remains on the implementation of an assessment and self-X optimization architecture to enhance the performance of AFE in the presence of observer imperfection. This work aims to retain the simplicity and flexibility of traditional integrated circuit design, while leveraging the potential opportunities offered by the transition to Industry 4.0.

1.3 The Goals of the Thesis

This research aims to develop an in-field performance optimizer for the reconfigurable readout sensory electronics systems with self-X properties for Industry 4.0 and IoTs devices. This thesis mainly focuses on implementing assessment and self-X optimization architecture for the performance optimization of the AFE in the presence of observer imperfection. Alternatively, preceding work [34] focuses on the USIX (Universal and Self-X Integrated Sensor Interface) chip, to which our group's subsequent research [35] adds more evolved features such as reconfigurability in the AFE, thereby developing a hardware platform for the intrinsic evolution of the proposed methodology.

In the context of this study, "in-field" refers to the placement of the device under

test (DUT) within the operational environment, such as a smart factory, smart car, or smart farming system. As a result, access to bulky laboratory device performance testing equipment is no longer available. Additionally, these devices present limitations in terms of limited battery power, physical space, and data reliability. Therefore, in order to effectively optimize performance in the field, it is imperative to reassess the conventional approach to integrated circuit design and capitalize on the full potential offered by the Industry 4.0 era. The hardware of interest in this study is the reconfigurable analog front end with self-X properties (AFEX) proposed by Alraho [35–37]. The reconfigurability of the hardware is limited to the sensitive elements, leading to a reduction in device implementation area and improved dynamic performance by minimizing parasitic effects. However, it is important to note that parasitics can vary not only due to process variations but also between instances of the same chip. In other words, an algorithm that inherently incorporates parasitics in circuit design for one chip may not work effectively on another chip. Additionally, it should be acknowledged that as the number of reconfiguration options increases, there is a likelihood of introducing additional parasitics.

The overhead of the performance assessment unit is also considerably essential for SSE in terms of system complexity and measurement time of different quantities. It is crucial to consider key performance characteristics of analog integrated circuits, including open-loop gain, phase margin, slew rate, gain- bandwidth product, and common-mode range. However, implementing a direct performance evaluation setup for infield performance optimization is not feasible. Therefore, this work aims to explore low-cost indirect measurement methods as an alternative approach. These methods rely on statistical correlations between different DUT performance characteristics and simple test stimulation to estimate various performance parameters simultaneously. Additionally, an indirect power monitoring scheme will be investigated to enhance system power efficiency, long-term reliability and ensure a safe reconfiguration pattern in analog evolvable circuits while addressing the power, performance, area, and cost (PPAC) metrics of IC [38].

In-field performance optimization requires embedding an AI agent in the automatic test equipment (ATE) for realizing self-X properties. This work discusses placing an AI agent at the lowest hierarchical level within ATE, with the aim of attaining self-X. Due to the complex search space of smart sensory electronic systems (SSES), simple

derivation-based optimization techniques are not suitable. Therefore, a particle swarm optimizer (PSO), a population-based metaheuristic optimization algorithm, is selected. Modifications to the basic architecture of PSO are required to balance exploration and exploitation [39] in the complex search space imposed by SSES. Potential improvements over state-of-the-art PSO variants are investigated through benchmarking functions.

Furthermore, the optimization of ICs in the presence of observer imperfection is very rare. It leads to unacceptable system performance even after the calibration or optimization [40]. This research also aims to explore the concept of integrating a fallible observer and co-integrating the sensor system itself, observer or assessment electronics, and computational unit with AI algorithms for reconfiguration in a practical and effective manner. Dynamic intrinsic optimization on the chip will be conducted by adjusting the temperature and supply voltage, demonstrating the capability to handle all sources of variation, including process, voltage, and temperature (PVT).

The implementation of the entire architecture for in-field performance optimization of the smart sensory electronic systems needed to be kept generic and easy to integrate with any higher level of system hierarchy or cloud computing for further data gathering and processing. One application with this data will be presented by modelling the regression model of the AFEX for dynamic operating conditions and optimizing its performance using the pretrained regression model. Finally, the thesis will discuss the possible solution to address the interruption problem of sensory measurement during the calibration process. The proposed discussion will interleave the calibration and measurement processes to achieve continuous measurement without interruption.

1.4 Thesis Structure

This thesis is organized into seven main chapters, each focusing on a specific aspect of optimization algorithms within the context of Industry 4.0 and reconfigurable analog integrated circuits with self-X properties. The structure is designed to provide a systematic and comprehensive exploration of the subject. Below is an outline of each chapter:

1. **Introduction:** This opening chapter sets the stage for the thesis, outlining the research background, motivation, and overarching goals. It introduces the challenges

and opportunities in the field of reconfigurable electronics.

2. **State of the Art:** A thorough review of the current literature is presented in this chapter. It highlights existing research, identifies gaps, and frames the context for the subsequent chapters.

3. **Optimization Algorithms:** This chapter explores the critical role of optimization algorithms in addressing the escalating complexity of real-world problems. It delves into various types of optimization algorithms, including heuristics, metaheuristics, and nature-inspired techniques, and their application in the context of Industry 4.0. The chapter also introduces the proposed Experience Replay Particle Swarm Optimizer (ERPSO), detailing its development, implementation, and performance evaluation.

4. **Proposed Design Methodology:** Here, the novel design methodologies developed in the research are introduced. This chapter discusses the conceptual framework and theoretical underpinnings of these methodologies.

5. **Experimental Setup and Results:** This chapter is crucial in demonstrating the practical application and effectiveness of the proposed methodologies. It details the experimental setups and presents the results obtained.

6. **Sensory System Application:** The application of the developed methodologies in sensory systems is explored in this chapter. It discusses the translation of research findings into practical, real-world solutions.

7. **Conclusions and Summary:** The final chapter synthesizes the research findings, draws conclusions, and reflects on the research's implications, limitations, and future directions.

In addition to these main chapters, the thesis includes sections and subsections that provide detailed explorations of specific topics within each chapter, ensuring a comprehensive exploration of the research area.

Chapter 2

State of the Art

The growing demand for adaptable systems in diverse sectors has propelled the significance of reconfigurable analog integrated circuits (ICs). These ICs are capable of adapting to process and dynamic variations, ensuring their optimal performance. This chapter presents a comprehensive overview of the reconfigurable analog ICs and specifically focuses on the introduction of analog evolvable hardware (EHW) system designed for readout sensory electronics. The EHW systems discussed here integrate bio-inspired metaheuristic optimization algorithms as an evolvable optimizer to recalibrate system performance to mitigate variations from the manufacturing process and dynamic factors. Additionally, this discussion covers the field programmable transistor array (FPTA) concept, which allows for on-chip reconfiguration of various circuits at the transistor level. This concept, highlighted by the work of the NASA JPL group, enables significant adaptability, though it faces challenges in optimizing designs exclusively through extrinsic simulations due to potential disparities between simulation results and actual fabricated chips.

To combat these issues, the chapter introduces the concept of mixtrinsic evolution, which combines both intrinsic and extrinsic evaluation techniques, ensuring robust and generalized solutions. Subsequent enhancements led to the development of FPTA2, the second-generation FPTA, addressing existing challenges and incorporating programmable capacitors, resistors, and integrated photodetectors. Practical applications of these advancements have been demonstrated through the stand-alone board-level evolvable system (SABLES) and evolved into the development of evolvable Systems-on-Chip (SoCs).

Further exploration of configurable electronics has led to significant developments from institutions such as TU Kaiserslautern research group. The group contributed a novel approach to configurable electronics granularity with the introduction of the field programmable medium-granular mixed-signal array (FPMA), providing flexibility in implementing various algorithms.

The chapter also addresses the integration of self-X principles in sensor systems, resulting in the development of the universal sensor interface with self-X properties (USIX), offering robustness for physical measurements using a single chip. These advancements align with the requirements of Industry 4.0, emphasizing the need for flexible systems over traditional fixed-design electronic systems. The chapter then delves into the role of the assessment unit in evaluating the performance of reconfigurable hardware, with a special emphasis on the mixtrinsic evaluation approach. It also discusses non-intrusive sensors' integration within reconfigurable hardware and their potential to enhance prediction accuracy.

Finally, the chapter sheds light on the challenges related to observer imperfections in the control or optimization loops and how robust optimization techniques can address these uncertainties. The overall discussion underscores the need for rapid prototyping, system performance optimization, and the design of intelligent sensor systems for Industry 4.0 applications.

2.1 Reconfigurable Electronics as a Fundamental Part of Industry 4.0

Highly integrated sensor systems have become a standard feature in everyday objects. However, the implementation of such systems faces significant challenges in harsh industrial environments. Extreme ambient conditions, such as high operating temperatures or humid and chemically aggressive environments, hinder the reliable operation of sensitive electronic components. This renders standard electronics, process technology, and packaging impractical for use [41, 42]. The demand for robust and reliable electronics becomes even more critical in applications exposed to harsher or noisier environments, such as space technology, where extreme temperature and radiation can significantly degrade circuit characteristics. This highlights the necessity for electronics that can

effectively endure and function in such demanding situations [43].

Moreover, with the initiation of Industry 4.0, the demand for adaptable systems that can quickly respond to evolving requirements has become vital for manufacturers. Traditional electronic systems relying on fixed designs for mass-produced products and predictable demand are no longer sufficient. The focus has shifted toward flexible systems that can be efficiently reconfigured with minimal operational and capital overhead [44].

On-chip dynamic approaches are based on organic computing and evolutionary electronics [5]. EHW refers to configurable electronic hardware that can self-configure using bio-inspired optimization algorithms [22, 23]. This approach involves employing configurable elements within the circuit and system performance evaluation setup [5, 11, 45]. These configurable elements serve as design tuning or calibration knobs that can be adjusted to restore the circuit performance, facilitating design adaptation throughout the product life cycle. Industry 4.0 highlights the value of self-X properties in automation technology [5], with these features serving as new design principles for efficient and autonomous manufacturing process control [26]. To address these challenges posed by harsh environments and the demands of Industry 4.0, researchers and engineers have turned to the concept of reconfigurable analog integrated circuits, which is a key element of evolutionary electronics and organic computing.

2.2 Reconfigurable Analog Integrated Circuits in the Literature

Understanding the potential and scope of reconfigurable analog integrated circuits, several studies and literature have delved into this area. The present study is part of this endeavor, introducing an analog evolvable hardware (EHW) system for intermediate frequency (IF) filters [46]. The system utilizes a genetic algorithm (GA) as an evolvable optimizer and consists of a reconfigurable IF filter. After fabrication, variations in process and dynamic factors can negatively affect the performance of the IF filter. To address these variations, the Gm filter's transconductance is fine-tuned by adjusting the biasing current. The architecture of the reconfigurable IF filter is depicted in Figure 4.6.

The GA acts as an optimizer to recalibrate the system performance. The circuit

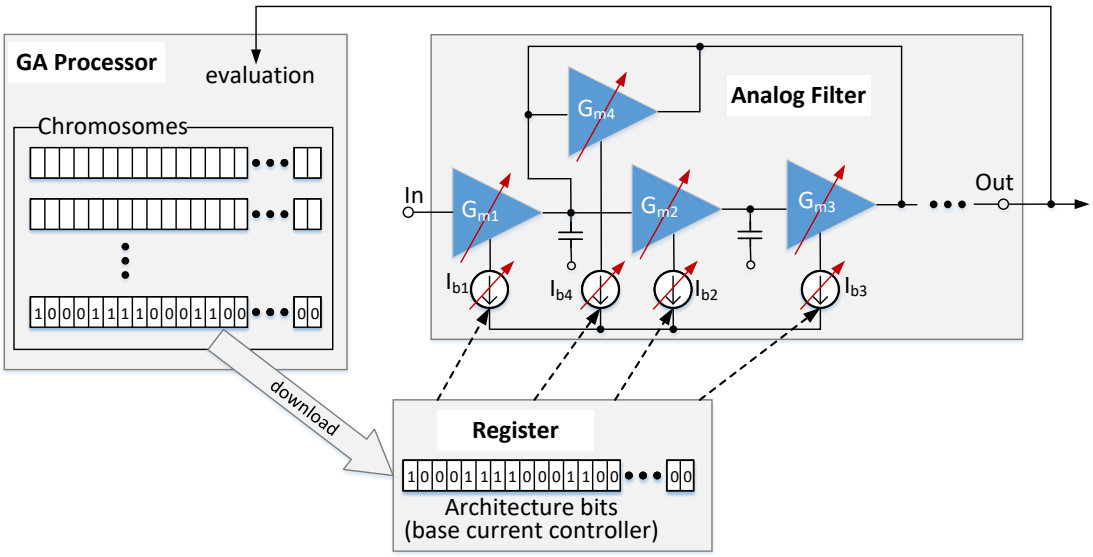

Figure 2.1: Analog evolvable hardware chip for intermediate frequency filters [46].

configuration can be modified by updating the binary string or architecture bits in the on-chip configuration register. These bits represent the chromosomes of the GA optimizer, indirectly controlling the transconductance of the Gm amplifier. The fitness value of the chromosomes is evaluated using the following equation:

$$\text{fitness} = \sum_{i=1}^{n} w_i \left| S\left(f_i\right) - O\left(f_i\right) \right| \tag{2.1}$$

where $S\left(f_i\right)$ represents the desired value, $O\left(f_i\right)$ represents the obtained value at frequency f_i, and w_i represents the corresponding weight. The chromosomes with higher fitness values are selected using an elitist strategy for the next iteration. Through the introduction of reconfigurability and optimization, approximately 95% of the IF filter can be recalibrated to meet the desired specifications.

Adrian Stoica from the NASA Jet Propulsion Laboratory (JPL) group presented an innovative concept termed the Field Programmable Transistor Array (FPTA), an analog EHW operating at the transistor level [47]. The primary FPTA chip, developed through 0.5 μm CMOS technology, encompasses 64 FPTA cells [48–50]. Figure 2.2 illustrates how these modules can cascade to form a versatile reconfigurable platform, allowing on-chip self-reconfiguration of digital, analog, and mixed-signal circuits [21]. The FPTA can be understood as a fine-grained FPAA architecture, equivalent to configurable analog blocks (CAB) at the transistor level [21, 49].

The evolutionary process at the transistor level enables the discovery of new and un-

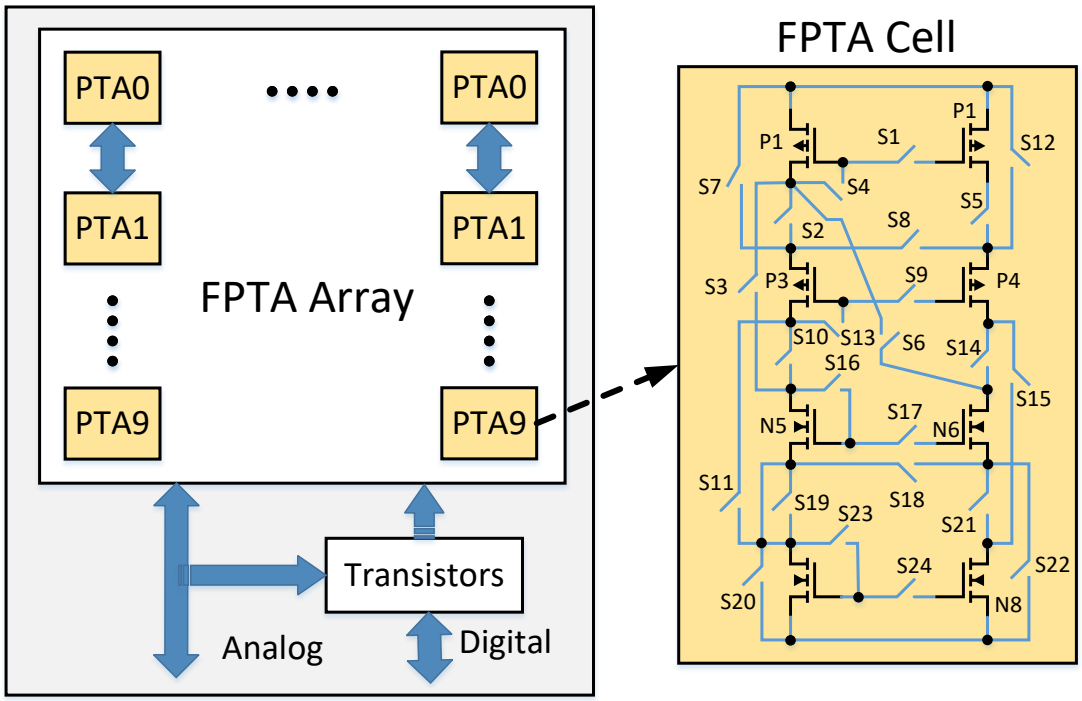

Figure 2.2: FPTA1 module from JPL [48].

conventional circuit topologies, going beyond conventional human designs. It also allows for the construction of standard topologies, which is particularly valuable for synthesizing robust and fault-tolerant hardware [51] under challenging operating conditions, such as extreme temperatures [52] throughout the operational lifespan. Figure 2.3 provides a visual representation of the evolutionary methodology, which is facilitated by a host machine running the Genetic Algorithm (GA). Within this research, the GA's chromosomes denote the binary bit patterns that determine the switching state of the elements in the reconfigurable hardware. For intrinsic optimization, control bitstrings are uploaded directly to the reconfigurable hardware, thereby enabling the circuit evolution on the hardware itself for assured solution validation. In contrast, in the case of extrinsic evaluation, the chromosomes are transformed into circuit models for fitness evaluation via the SPICE simulation. Subsequently, device reactions are evaluated against the intended specifications, and individuals are graded according to their fitness value. In the succeeding iteration, a new population is generated from the highest-ranking individuals of the previous generation. Nevertheless, relying exclusively on extrinsic simulation for optimization has its limitations due to potential disparities between simulation and fabricated chips [49].

Addressing the issue identified in previous research [52], there is a potential discrep-

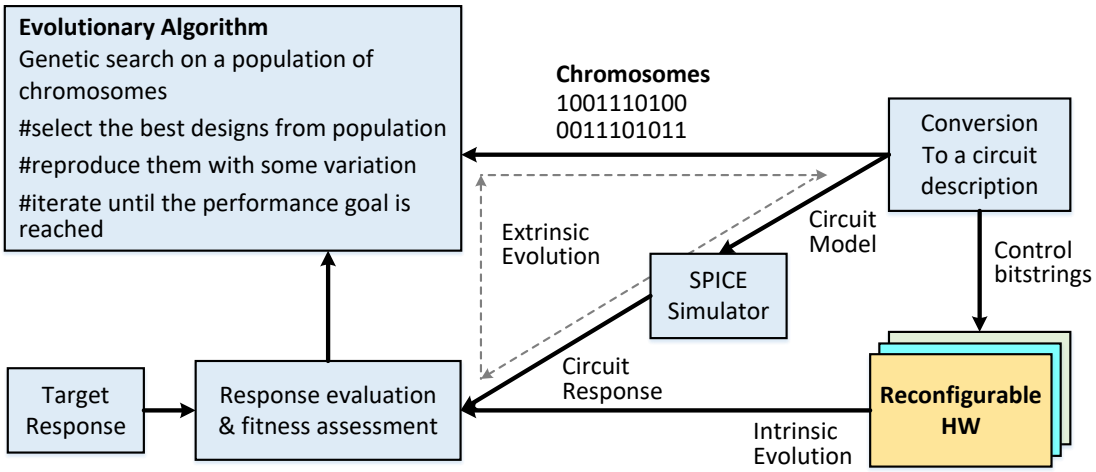

Figure 2.3: Analog EHW Chip for IF filters [48].

ancy between optimized solutions derived from extrinsic optimization and their evaluation on the real hardware. This discrepancy could arise from various factors including inconsistencies between models and physical hardware, limitations of the simulator and testing systems, and others [53]. To rectify this, a third approach to Evolutionary Hardware (EHW), known as mixtrinsic evolution, is introduced in [53]. Mixtrinsic evolution encapsulates an array of techniques that incorporate a variety of combination methodologies for the extrinsic and intrinsic modes. The most prevalent method entails the evaluation of each candidate solution in both software and hardware, assigning an average fitness value accordingly. Solutions generated through the mixtrinsic evolutionary process are robust and sufficiently generalized to satisfy the design constraints of both platforms.

The simulation of complex analog circuit modules can be considerably more time-intensive than hardware optimization. Several challenges are associated with the FPTA approach. This includes the influence of the on/off resistance and parasitic capacitance of CMOS switches on the performance of analog circuits, and the lack of passive components such as capacitors and resistors in the FPTA structure. Moreover, the immutable size of the MOS transistor in the FPTA introduces restrictions related to adaptability and optimization.

Despite these limitations, the authors developed the second-generation FPTA2, which incorporates configurable cells with programmable capacitors, resistors, and integrated photodetectors for mixed-signal tasks [54]. The FPTA2 chip, fabricated using 180 nm CMOS technology, offers enhanced granularity and the capability to

create complex analog blocks such as buffered op-amps, filters, and computational circuits [54]. It serves as a field-programmable mixed-signal array (FPMA) and lays the foundation for on-chip evolvable sensor interface systems.

To demonstrate the practical applications of evolvable analog circuits, the JPL group developed the stand-alone board level evolvable system (SABLES), featuring the FPTA2 as a compact, low-power, standalone evolvable board [55]. The SABLES system showcases rapid prototyping of fault-tolerant self-reconfigurable analog circuits and real hardware-in-the-loop autonomous applications. It addresses observer uncertainty, GA processor limitations, and signal stimuli challenges encountered in the adaptation loop. The system's success opens the door to the development of evolvable SoCs, integrating the GA on the same chip and enabling self-recovery capabilities for extreme temperature conditions [56]. In an enhanced version of SABLES, the digital signal processor (DSP) unit was replaced with a field-programmable gate array (FPGA) [24].

Following JPL's work, many research institutions, including the University of Sussex [57], Catholic University of Rio [58], and UERJ-Rio de Janeiro State University [59], have initiated development of evolvable platforms similar to SABLES, although based on discrete components. The authors of [60] created a FPAA with a continuous-time OTA-C filter that can perform various signal-processing tasks at frequencies up to 20 MHz, while offering a wide tuning flexibility [61]. Georgia Tech researchers [62] proposed an FGT-based CT FPAA, achieving higher bandwidth and a more compact architecture than previous designs. This design was later developed into an ultra-low-power SoC-based FPAA chip [63], enabling rapid reconfigurable analog and digital computation. Albert-Ludwigs-University researchers [64] presented a CT FPAA topology, offering capabilities for various high-speed filter circuits and promising for artificial evolution and rapid prototyping of configurable CT filters . The configuration's performance was tested through simulation [65]. A new OTA-C based FPAA [66] replaces conventional routing switches [67], improving reconfigurability and frequency performance, and enabling accommodation of multiple independent and cascading filters. The JPL group evolved from FPTA2's limitations to create the reconfigurable analog array [68], offering higher configurability and bandwidth. The group then further improved the design with the self-reconfigurable analog array [69], allowing real-time adaptation during operation while compensating for temperature fluctuations.

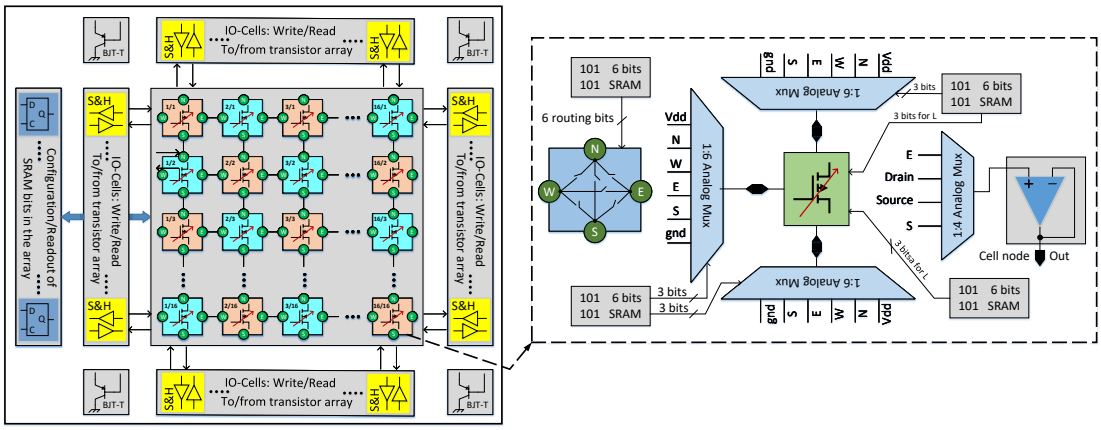

Figure 2.4: The simplified block diagram of the proposed FPTA proposed by Heidelberg group on the left and right given the NMOS transistor cell block diagram [70].

The research group from TU Kaiserslautern has demonstrated substantial progress in the exploration of granularity within the context of configurable electronics, focusing on fine (FPTA) and coarse-grained approaches (FPMA) [71, 72]. They introduced the field programmable medium-granular mixed-signal array (FPMA) as a hybrid granular level approach, designed for rapid prototyping of continuous-time circuits in sensory electronics [72, 73]. The FPMA enables the realization of self-X properties, such as self-healing and self-adaptation, and offers flexibility in implementing various algorithms. By integrating design knowledge and optimizing circuit topologies, the authors achieved predictable system behavior and reduced configuration switches, leading to improved dynamic performance and compliance with industrial standards [74, 75]. The FPMA demonstrated the implementation of configurable op-amps and the Generic Operational Amplifier (GOPA) with adaptability in topology and programmable elements, providing versatility in circuit selection and device sizing [74].

Measurement results of the first fabricated FPMA chip were presented, demonstrating manual and optimized configurations for specific circuit parts [76, 77]. Intrinsic and extrinsic optimization experiments were conducted to examine system performance under dynamic environments and temperature changes [78, 79]. The proposed reconfigurable sensor system, depicted in Figure 2.5, consists of reconfigurable hardware, an optimization unit employing evolutionary algorithms, and an assessment unit for measuring and extracting hardware specifications during the reconfiguration process [78, 79]. FPMA2, a revised version, incorporated layout techniques, reduced switches per transistor unit, and employed charge pumps for improved performance [74, 80]. The FPMA

approach also led to the development of an analog IC training board for rapid prototyping and educational purposes [81]. Comprehensive information about FPMA1, FPMA2, and the optimization approach can be found in [82, 83].

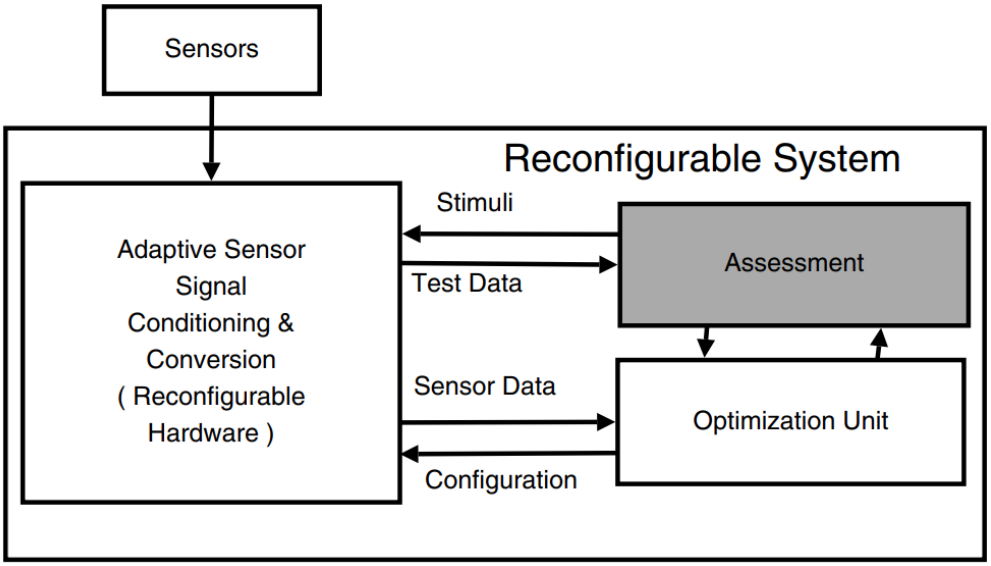

Figure 2.5: Conceptual block diagram of the evolvable sensor system. [79].

Furthermore, in [79], a novel approach called Mixtrinsic evolution was introduced, which addresses the challenge of simulating specifications that are difficult to measure due to cost and time constraints. It classifies hardware specifications into two distinct categories. The first category consists of specifications that present difficulties in measurement due to cost and time factors. Specifications such as open-loop gain, phase margin, and output resistance, which are less prone to deviations, fall under this category. For these, an extrinsic evaluation technique is adopted. Conversely, the second category comprises specifications that exhibit sensitivity to deviations and have a direct impact on signal distortion. Specifications including offset, swing output voltage, and common mode range (CMR), which are economically and easily measurable, belong to this category. For these, the approach employs an intrinsic measurement technique. The optimization criteria in this approach involve multi-objective optimization, where each individual is assigned both intrinsic and extrinsic objectives, as illustrated in Figure 2.6. It is important to highlight that, unlike in [53], this approach refers to "mixtrinsic multiobjective evolution," indicating the utilization of both intrinsic and extrinsic evolution for each individual with different objectives.

Moreover, the researchers expanded the concept of self-X vision to enhance the design

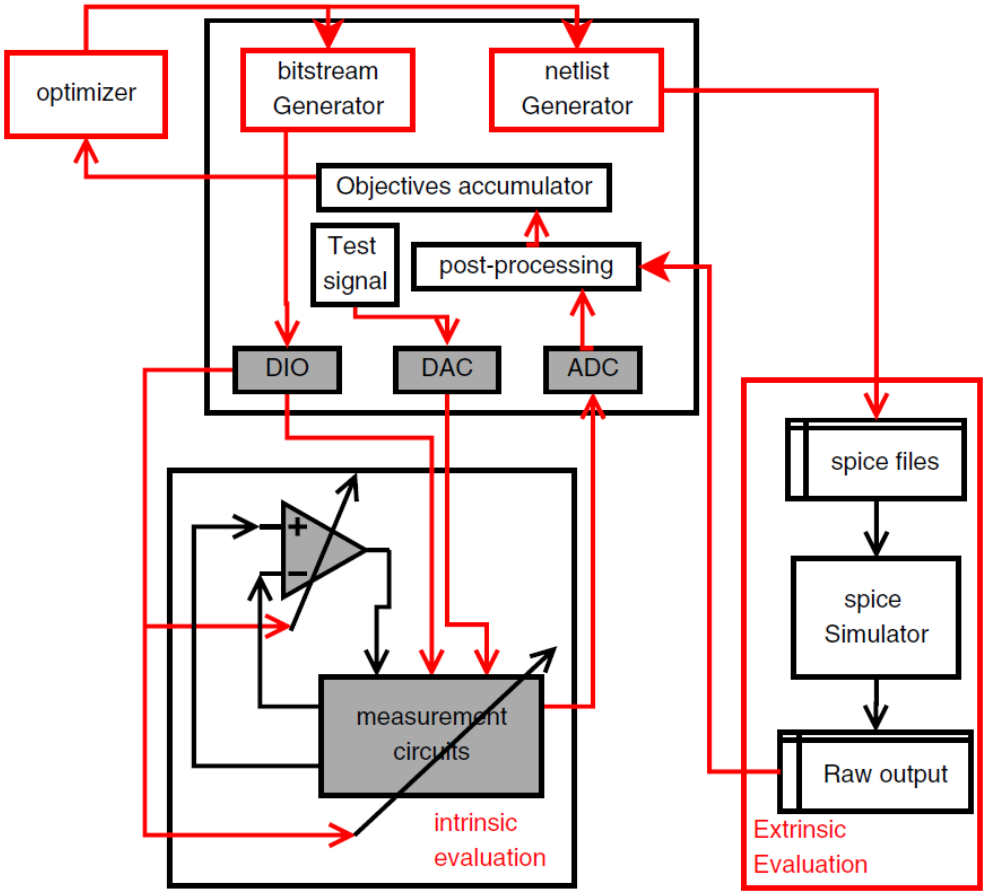

Figure 2.6: New type of mixtrinsic multi-objective optimization environment proposed by authors in [79].

of intelligent integrated sensor systems, introducing self-X principles at various levels of abstraction, including the sensor element within the optimization loop [84]. Integration of calibration actuators inside the sensor was proposed for error minimization [85–87]. The power consumption of wireless sensor nodes can be reduced through the control of sensor bridge power using a programmable current source controlled by the self-X system [88, 89]. To address the demands of Industry 4.0, a universal sensor interface with self-X properties (USIX) was developed, providing versatility and robustness for various physical measurements using a single chip [90]. The principal enhancements in the USIX 2.0 version predominantly focus on its optimization for integration with dual bridge magnetoresistive sensors (XMR), notably those with a high dynamic differential range, such as tunnel magnetoresistance (TMR) sensors. It also incorporates self-X functionalities for the TMR sensor by managing the reset coil during incidents of sensor saturation. Another key advancement is the integration of impedance spectroscopy measurements, which directly facilitates the evaluation and diagnosis of aging-related

effects [91, 92]. Overall, the research group work on granularity, reconfigurable electronics, and self-X vision contributes to the advancement of rapid prototyping, system performance optimization, and the design of intelligent sensor systems for Industry 4.0 applications.

A reconfigurable Tow-Thomas filter is discussed in [93]. This filter offers limited tunability restricted to sensitive elements only, reducing area and parasitic effects. The tuning of R(C) values optimizes the system performance while considering process variations. However, achieving higher resolution demands larger chip area and increased power consumption due to passive elements in the tuning knobs. Therefore, a compromise must be made between area, power consumption, and optimization quality when selecting the resolution.

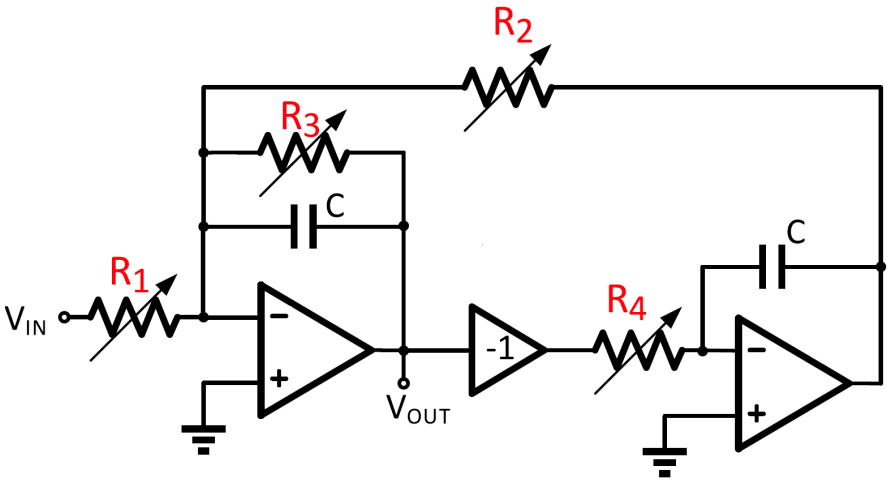

Figure 2.7: Tow-Thomas BPF circuit with tunable resistors R_1, R_2, R_3, and R_4 [93]. This figure has been adapted from [93] to align with the standard Tow-Thomas filter configuration [94], as the original deviated in the placement of '+' and '-' inputs.

The optimization of device under test (DUT) characteristics can be achieved indirectly through statistical correlation among different performance characteristics, as presented in [45]. Figure 2.8 shows the flow diagram of the proposed optimization process. The process starts with low-cost measurements from non-intrusive sensors. If the DUT's performance falls below the specified threshold, the optimization loop is executed to meet the desired specifications. This calibration process employs pretrained regression models to approximate the complex correlations among different characteristics of reconfigurable analog integrated circuits. In this work, an artificial neural network is used as a regressor. The proposed post-fabrication calibration technique is demonstrated on a 65 nm RF power amplifier based on fabricated chips from corners and typical wafers.

The minimum achieved performance yield is shown to be 92.3%.

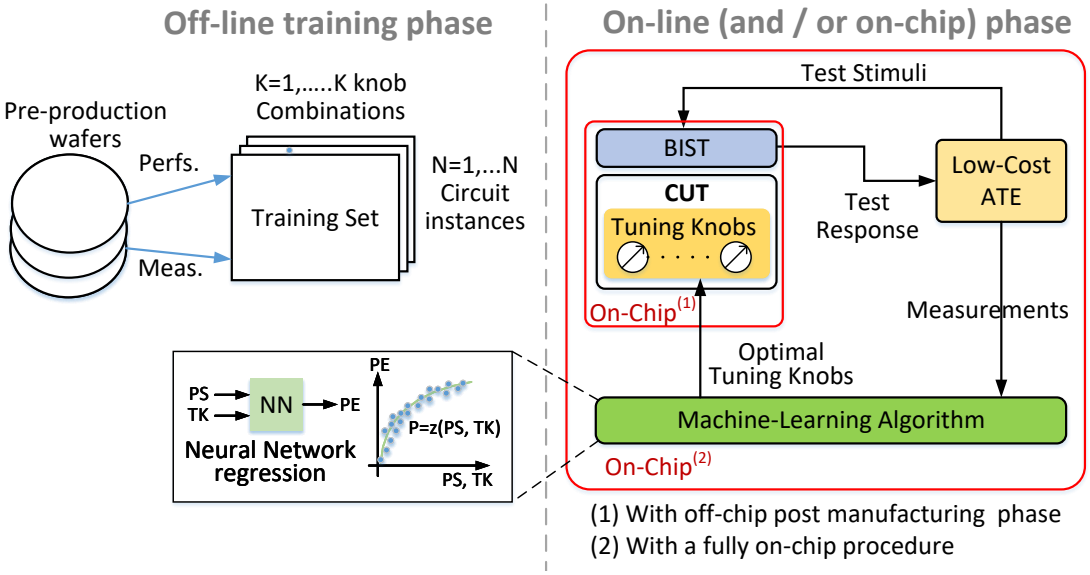

Figure 2.8: Flow diagram of the one-shot calibration procedure [45].

Furthermore, on-chip analog circuit optimization and built-in self-test are presented in [11]. By integrating the digital optimization unit and self-test circuits module on-chip beside the DUT, this scheme can automatically explore an operating point that accomplishes a nice trade-off among different competing characteristic goals. The intrinsic evaluation of this scheme is demonstrated by using a Tow-Thomas bandpass filter as a DUT. The complete conceptual representation of this scheme is presented in figure 2.9. It consists of a digital optimization unit and an analog BIST part. The performance characteristics of the DUT can be tuned by the N-dimensional vector $V \rightarrow = [x'1, x'2, \cdots, x'N]$, which represents the collection of tuning knobs, such as widths of transistors, bias currents, resistances, and capacitances. These tuning variables are implemented by using an array of resistors, transistors, and capacitors using digitally controlled switches.

This platform allows measuring and analyzing two types of responses: frequency-domain and time-domain. However, it does not utilize the full degree of freedom provided by modern edge and cloud computing IoTs and Industry 4.0 domain.

Fraunhofer and Globalfoundries are currently developing the Universal Sensor Platform (USeP) [95], which aims to provide a fast, reliable, and flexible platform for industrial applications. USeP adopts a three-layer architecture:

(i) Top-Level: Sensors and Core Functionality

(ii) Mid-Level: SoC Core System

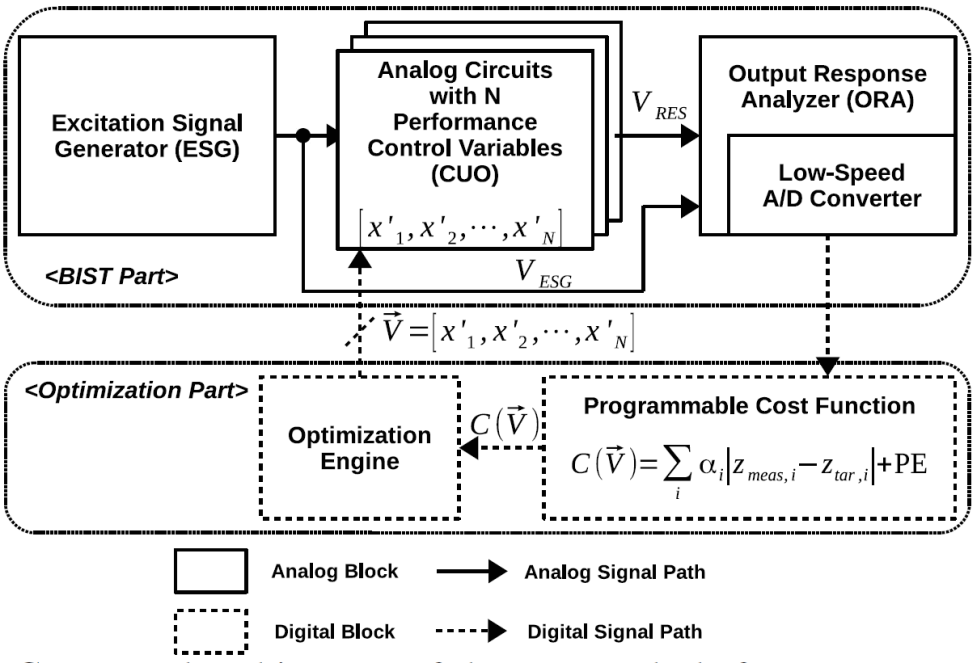

Figure 2.9: Conceptual architecture of the built-in self-test circuit optimization platform [11].

(iii) Bottom-Level: System Board

USeP intends to support the integration of various sensors for different physical parameters. It also plans to include multiple communication standards and integration in fog, edge, and cloud computing, while focusing on lower power consumption. The ongoing project "Intelligent Reliability 4.0" aims to develop new reliability models and methodologies for electronic systems and ICs [96]. This project specifically supports IC designers in achieving reliability objectives. The objective is to streamline the existing aging simulations process by incorporating a universally applicable methodology for evaluating reliability as a standard procedure within electronics design.

The Synopsys Silicon Lifecycle Management (SLM) product suite [30, 33] is specifically designed to enhance silicon devices' health and operational metrics throughout their lifecycle. By integrating in-chip observability, analytics, and automation, SLM enables a comprehensive understanding of devices at both the chip and system levels, as depicted in Figure 2.10. Crucially, built-in sensing devices, including PVT sensors, continuously monitor the dynamic operating conditions of the chip (voltage and temperature) as well as the static process characteristics, allowing for the in-field optimization of power consumption and speed performance based on the local chip conditions. This approach helps detect anomalies and correct them before complete failure, improving

long-term system reliability. PVT sensors play a vital role in validating power reduction techniques, ensuring power remains within the targeted window and thermal dissipation adheres to specified chip and package design requirements. Deviating from these metrics can result in compromised performance and device failure. The collected data can be analyzed on-chip to optimize performance and security or transmitted to the cloud through various on-chip interfaces for more complex analysis. Cloud-based analysis of aggregated system performance allows for two key objectives: maintaining device performance as intended and identifying and addressing unforeseen device issues.

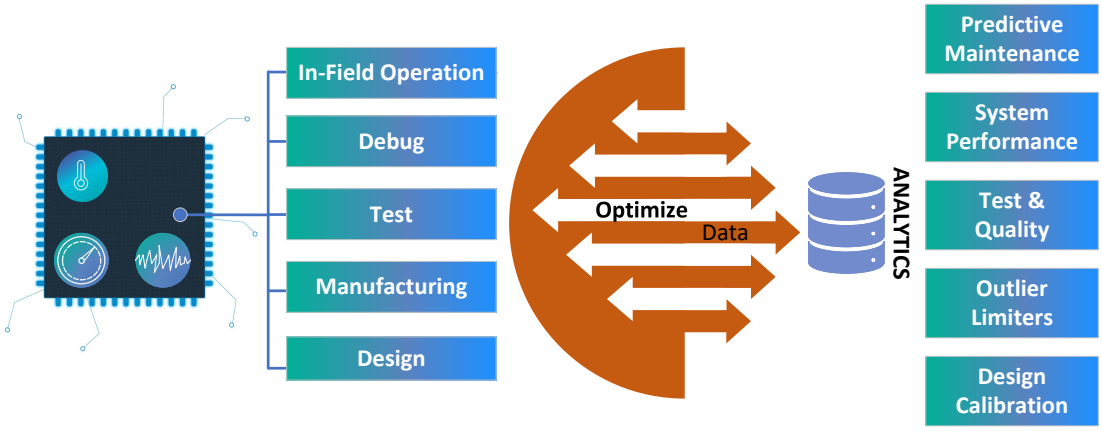

Figure 2.10: SiliconMAX Silicon Lifecycle Management (SLM).

In summary, field programmable electronic hardware, particularly with respect to analog and mixed circuits, is differentiated into three unique levels of granularity: coarse, medium, and fine. Coarse-granular field programmable analog arrays (FPAAs) are conducive to quick prototyping of intricate analog circuits, making them suitable for sensor signal processing and interfacing. However, their limited programmability often restricts the full execution of the evolutionary process, usually only supporting partial evolution.

Conversely, fine-grained evolution at the transistor level provides a versatile basis for bio-inspired optimization. It can adapt circuits to demanding operating conditions and potentially discover innovative design solutions. However, the resources required for switches and element arrays are significant, leading to an increase in the die area. This situation limits dynamic performance due to switch non-idealities and extensive routing. Moreover, the unpredictability of non-standard circuit solutions diminishes the appeal of fine-grained structures within the industry.

Medium-granular FPAAs offer a balanced approach, presenting flexibility and pre-

dictable output owing to their predefined circuit topology. This is in line with industry standards. The primary objective of configurable hardware is to support in-field self-X functionalities, guided by various evolutionary algorithms. However, in-field optimization requires an assessment unit to evaluate the system's performance under operational conditions. The use of laboratory equipment or ATE machines is not practical in such scenarios. Consequently, it is necessary to integrate cost-effective performance evaluation techniques into reconfigurable hardware. This aspect will be discussed in greater detail in the subsequent section.

2.3 Assessment Unit

The assessment unit is a crucial part of measuring and evaluating reconfigurable hardware performance. Performance assessment can be performed extrinsically, intrinsically, or mixtrinsically [82].

Extrinsic evaluations are conducted through simulation-based measurement setups, whereas intrinsic evaluations depend on real hardware measurements. Mixtrinsic evaluation, as the name suggests, combines both real and simulation-based measurements. This method was first proposed in [53], which used a genetic algorithm incorporating both intrinsic and extrinsic individuals. In prior work conducted at our institute [82], this concept was further developed by performing complex measurements extrinsically and executing simple measurements intrinsically, thereby reducing the complexity of the assessment unit [82].

Nonetheless, the reliance on simulations in both methods poses a challenge as it may not always yield accurate results compared to intrinsic evaluations with real hardware. Additionally, under conditions with significant process variations and discrepancies between hardware and simulation performance, a mixtrinsic approach might not be practical [97].

Evaluating the cost-effectiveness of intrinsic evaluation measurement setups is especially crucial for smart sensory electronics (SSE) with increasing system complexities. Performance measurement setups for a DUT can be categorized into two based on the evaluation principle of the desired performance parameters [11]. The first category directly measures performance characteristics, offering higher accuracy and precision but

also increased design complexity and chip area [11,20]. The second category employs indirect measurement (IM) methods, which leverage statistical correlation [11,45,98–103]. IM methods can estimate multiple system performance parameters simultaneously using simple test stimuli [45].

In [101], the authors applied an optimized multitone signal with the assistance of an evolutionary algorithm (EA) to the operational amplifier. They examined the transient response to indirectly estimate characteristics such as input common-mode range, gain, slew rate, and bandwidth. To enhance prediction accuracy, [102] proposes a substitute test flow centered on the two defect filters approach. A similar concept is presented in [103], where an envelope detector is employed to infer the target characteristics of the ICs. However, in the application of SSE, this category of IMs requires optimization due to limitations in computational resources.

To minimize the measurement and implementation costs of ATE, the authors in [104] introduced another distinct category of IM methods that utilize feature extractor sensors. These sensors can perform DC or low-frequency measurements. This capability significantly reduces testing costs. An essential characteristic of these sensors is their non-intrusive nature; they are electrically disconnected from DUT. Consequently, the monitoring operation does not affect the performance of the primary circuit [45,99,105]. Also, this implies that these sensors can be seamlessly integrated into the design without resizing the DUT to compensate for the sensor effect. The sensors are constructed using basic analog stages replicating a portion of the main circuit's topology. They also incorporate stand-alone layout components, such as transistors and capacitors, directly copied from the DUT layout. By placing the sensors in close proximity to the DUT, they experience the same process variations and local operating conditions. As a result, the sensor measurements correlate with the DUT performance. For non-intrusive sensor design, the correlation among them should be as minimal as possible. Contrarily, their correlation with the targeted characteristics of DUT should be as maximal as possible. As observed from Figure 2.11, during the designing of the proposed non-intrusive sensor the correlation among the sensors themselves is kept significantly small, while it has a good correlation with the performance characteristics of a fully differential indirect current feedback instrumentation amplifier (CFIA). Here CFIA is used as a test vehicle because of the non-intrusive property of these sensors it can be used to predict the

performance characteristics of other analog integrated circuits as well [45]. This figure shows three sensors, where Sensor 3 is referred to as the temperature sensor [35] and is specifically designed to address the chip's dynamic variations.

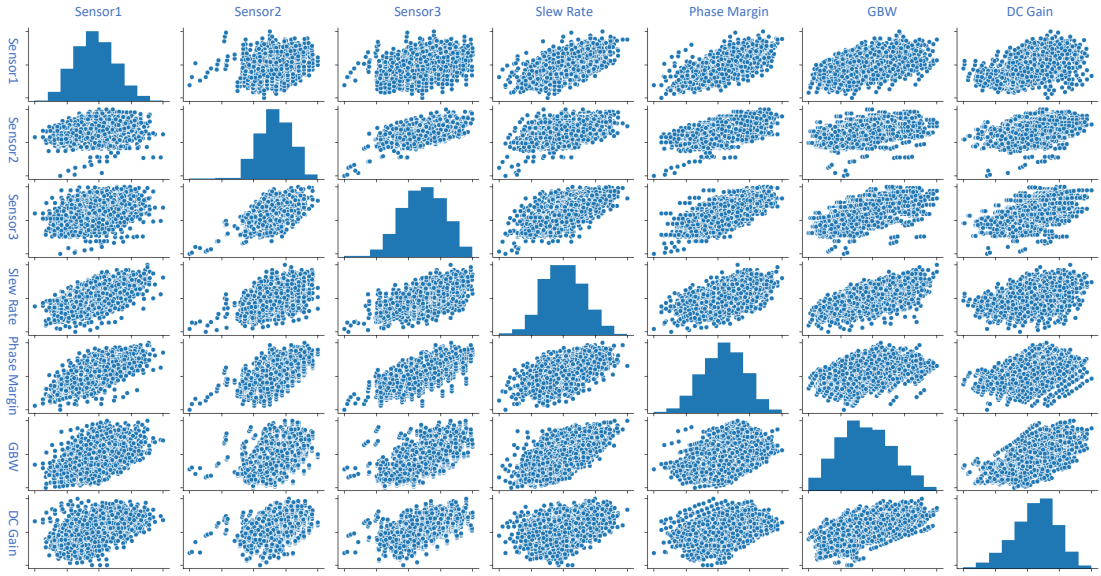

Figure 2.11: Correlation of the non-intrusive sensors with targeted performance characteristics of DUT.

Normally, regression models are utilized to indirectly estimate the DUT performance based on cost-effective, non-intrusive sensor measurements [45]. The optimization time using non-intrusive sensors-based indirect measurement methods is faster compared to executing tests with real measurements because it relies on simple measurements and the predicted performance provided by the regression model [105]. This methodology has attracted considerable attention [45, 106–110] and is worth investigating further for enhancing AFEX performance.

As the performance (Y) of the device being tested is influenced by variations in process, voltage, and temperature (PVT_r) as well as calibration adjustments (CK). This relationship can be represented by a function (f) defined as:

$$Y = f(PVT_r, CK). \tag{2.2}$$

Since directly measuring the PVT variations is not feasible, measurements (X) that are indirectly related to these variations through a function (g) are typically used:

$$X \approx g(PVT_r). \tag{2.3}$$

By combining equations (1) and (2), Y can be approximated as a function of X and CK:

$$Y \approx f(g^{-1}(X), CK) \approx z(X, CK). \tag{2.4}$$

The function z is unknown, and it is not possible to derive it analytically [45]. Therefore, a commonly employed solution is to utilize an artificial neural network (ANN) as a regressor to approximate the regression task. By employing an ANN, the desired performance can be predicted based on the gathered data. The training and testing phase for the IMs using non-intrusive sensors are graphically illustrated in figure 2.12.

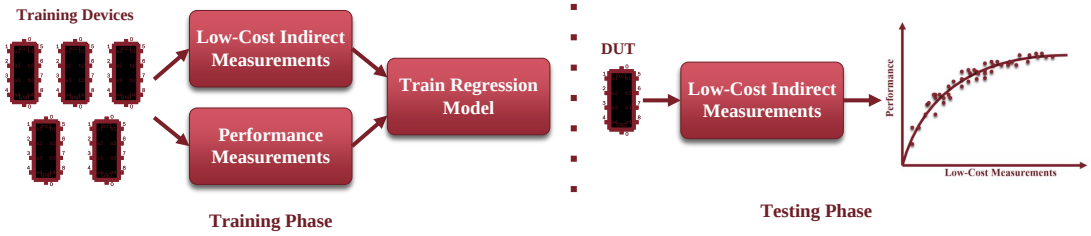

Figure 2.12: Training and testing phase for indirect measurement methods.

It is worth noting that the process of generating and collecting the necessary data for the training phase of the ANN presents considerable challenges. The complexity of this task increases exponentially with the complexity of the DUT. Moreover, the non-intrusive sensors discussed in existing literature primarily possess a static nature, offering only a snapshot of the current operational state of the IC. To fully integrate non-intrusive sensors into the optimization process, it is necessary to introduce reconfigurability within these sensors. This would enable the utilization of tuning parameters within the non-intrusive sensors themselves rather than relying solely on tuning parameters of the DUT using a pre-trained regression model. This approach would indirectly improve prediction accuracy, particularly under severe PVT operating conditions. By incorporating reconfigurability in non-intrusive sensors, the entire optimization process can be performed, allowing for more precise adjustments based on the dynamic feedback from the sensors.

2.4 Observer Imperfections

The realization of an observer within the control or optimization loop is an interesting and significant aspect to consider. Typically, this observer is constructed using the same components as the circuits being analyzed, which can introduce errors. Some studies have addressed this challenge by employing monitoring devices such as analog-to-digital converters (ADCs) with higher resolution and quality than the systems being monitored, as demonstrated in [79]. However, this approach is not practical as the observer should ideally be implemented using the same components as the rest of the system.

The inherent problem in observer implementation is that it becomes subjected to the same detrimental influences as the actual sensing system, given the 'all-in-one' objective. This problem becomes even more prominent when the observer is a crucial part of an intricate system where data reliability is essential, such as in advanced applications like smart cars. Most of the state-of-the-art research considers these observers in ideal conditions, potentially oversimplifying the actual scenarios the system might encounter. One notable example in the literature evaluated the performance of the ADC under extreme temperature conditions [24]. This study demonstrated that a 14-bit ADC could lose up to 5 to 6 bits of accuracy, leaving only 8 to 9 effective number of bits (ENOB). This loss translates into a significant 43% decrease in ADC performance, which can heavily impact the subsequent stage of artificial intelligence or machine learning-based performance predictors. This significant reduction in accuracy can result in an unacceptable system performance that may not be rectifiable through calibration or optimization processes [40]. Therefore, this underlines the real challenge: addressing all types of uncertainties associated with the observer without compromising the system's integrity or adding undue complexity.

One effective strategy to manage these uncertainties involves the application of robust optimization [111], which can be categorized into two main types [112]: archive-based robust optimization [112,113] and robust optimization that utilizes meta-heuristic optimization algorithms. These algorithms benefit significantly from the extensive exploration capabilities of the search agents during the optimization process, allowing for a more thorough noise minimization through repeated assessments of the same solution.

The estimation of effective fitness for a trial solution X on a noise-affected objective

surface is computed using the following integral:

$$f_{\text{noisy}}(X) = \int_{-\infty}^{\infty} (f(X) + \eta)p(\eta)d\eta \tag{2.5}$$

In this formula, $p(\eta)$ represents the probability distribution of noise η, which distorts the true value of the objective function $f(X)$. Owing to the dynamic variations induced by noise, evaluations of the same trial solution may yield varying outcomes. Typically, the closed-form analytical expression for the effective fitness function is not available for most noisy optimization scenarios [111]; hence, it is approximated through Monte Carlo methods.

Monte Carlo methods approach the estimation of a solution's fitness $f(X)$ by repeatedly measuring it across multiple instances—often referred to as sample size. The collected fitness values from these multiple evaluations of $f(X)$ are subsequently averaged to calculate the mean fitness estimate of X:

$$\bar{f}(X) = \frac{1}{n}\sum_{j=1}^{n} f_j(X) \tag{2.6}$$

$$\sigma(f(X)) = \sqrt{\frac{1}{n-1}\sum_{j=1}^{n}(f_j(X) - \bar{f}(X))^2} \tag{2.7}$$

$$\text{se}(\bar{f}(X)) = \frac{\sigma(f(X))}{\sqrt{n}} \tag{2.8}$$

This methodology leverages the power of averaging over multiple observations to reduce the standard error of the mean fitness estimate, enhancing it proportionally to the square root of the sample size, n. This increase in measurement accuracy effectively mitigates the impact of noise, thereby refining the precision of fitness evaluations under noisy conditions.

It is evident from 2.8 that sampling an individual's objective function n times reduces $\text{se}(\bar{f}(X))$ by a factor of n, thus improving the accuracy in the mean fitness estimation [111]. However, this approach requires additional memory resources. Initially, during the optimization process, the optimizer tends to prioritize exploitation and may select a suboptimal solution due to the imperfections of the observer. However, as the exploration progresses, the correctness of the solution is evaluated with the assistance of the archive

[112]. This method not only mitigates the observer imperfections but also enhances the robustness of the system against noise and variability during optimization.

The second category is surrogate-based robust optimization, which relies on methods such as Gaussian process regression (GPR) [114–116]. GPR, a well-known Bayesian statistical regression technique, falls under this category. It is widely used for uncertainty quantification and design optimization. In addition to fitting a wide range of functional models, GPR also provides confidence intervals for prediction values [115, 116]. GPR is capable of effectively representing uncertainty, enabling better estimation of uncertainty and facilitating robust optimization [117].

In this context, robust optimization strategies, specifically archive-based and surrogate-based robust optimization, present promising avenues for addressing these challenges. These strategies, which will be elaborated upon in the following sections, aim to alleviate the uncertainties and enhance the reliability and effectiveness of the 'all-in-one' design approach. Such endeavors will further advance the field by enabling observer implementation that is more resilient, adaptable, and capable of maintaining high-performance levels in the face of dynamic environmental conditions or component degradation.

Chapter 3

Optimization Algorithms

In this chapter, the intriguing world of optimization algorithms is explored. Recognizing their critical role in addressing the escalating complexity of real-world problems, the development and application of these algorithms across various fields are investigated, emphasizing their inherent strengths, limitations, and applicability.

The chapter begins with an overview of optimization algorithms, discussing their vital function in resolving intricate real-world issues. The crucial characteristics of an effective optimization algorithm, namely, the ability to balance exploration and exploitation functions, are elucidated. This balance lays the foundation for understanding optimization algorithm performance.

Following the general overview, the discussion transitions into the types of optimization algorithms, focusing on two primary categories: heuristics and metaheuristics. Their characteristics, differences, and specific applications are thoroughly explored, providing a comprehensive understanding of these powerful tools.

Subsequently, the chapter delves into nature-inspired optimization techniques. The unique ways in which these algorithms draw inspiration from biological processes, social behavior, and physical-chemical systems to solve complex problems are explored. The different categories of these nature-inspired techniques are also examined, highlighting their unique traits.

The later sections of the chapter focus on specific optimization algorithms and their applications. Particle swarm optimization (PSO) is discussed in detail, along with an overview of some popular modifications introduced in this algorithm. The proposed experience replay particle swarm optimizer (ERPSO) is also presented, offering a detailed

explanation of its operation and potential. Finally, the performance of ERPSO on benchmarking functions is evaluated, providing empirical evidence of its efficiency and effectiveness.

3.1 Overview of Optimization Algorithms

Owing to its substantial impact on industrial practices, the realm of optimization consistently gains the interest of a multitude of researchers hailing from both industrial sectors and academic environments. In our contemporary era, the complexity involved in resolving real-world problems has escalated exponentially. This complexity has been significantly increased due to the increased influence of external variables. As a direct consequence, classical optimization techniques oftentimes prove to be inadequate in providing viable solutions to these intricate issues.

Furthermore, the optimization landscape is in a state of constant evolution, enriched persistently by a deluge of innovative concepts, methodologies, and algorithms. This steady influx of innovation is largely driven by the relentless efforts of researchers engaged in this field. As postulated by the No Free Lunch Theorem [118], there exists no single optimal solution that can address every specific problem. This effectively means that there is always room for improvement and refinement of the existing optimization algorithms. This, in turn, engenders a prolific development of increasingly efficient optimization algorithms. These algorithms are implemented across an array of disciplines on a consistent basis. This surge in algorithmic development and utilization can be attributed not only to the rapid progression of technology but also to the significant advancements in computational capabilities.

The performance of an optimization algorithm can be effectively evaluated by maintaining an equilibrium between two vital characteristics: exploration and exploitation [100, 119, 120]. These characteristics are intrinsically related to global search and local search, respectively. The exploration function pertains to the ability of an algorithm to explore and analyze a wide solution space, while the exploitation function refers to its capacity to refine and optimize solutions within a localized area. The interplay and balance between these two functions form a crucial aspect of evaluating the efficacy of any optimization algorithm.

Optimization engineering problems are generally classified into two overarching categories: heuristics [121] and metaheuristics [122]. Heuristic techniques are usually reliant on the specific problem at hand, taking into account all the parameters and specifications unique to the problem. As a result, these methods are prone to falling into local optima. In contrast, metaheuristic algorithms are not bound by the specifics of the problem. These techniques delve into the solution space more exhaustively to ascertain superior solutions and can be leveraged as universal problem-solving tools or "black boxes". It is important to note, however, that despite their wide-ranging applicability, metaheuristic algorithms do not guarantee the achievement of a globally optimal solution when compared to iterative methods [123].

Nevertheless, metaheuristics exhibit substantial utility in discovering optimal solutions to real-world combinatorial problems. Their inherent simplicity makes it feasible for them to search through a vast array of potential solutions. A prominent subset of these algorithms are what's typically known as nature-inspired optimization techniques [124, 125], which have gained considerable traction among researchers in recent times.

As suggested by their name, nature-inspired optimization techniques embody a diverse spectrum of algorithms, each drawing inspiration from various natural phenomena. These algorithms can be classified into three primary categories: (a) bio-inspired, (b) swarm intelligence, and (c) physical-chemical systems [123, 126].

Bio-inspired algorithms derive their methodology from biological processes and mechanisms observed in nature [127–130]. Swarm intelligence algorithms, on the other hand, imitate the collective behavior of social colonies, such as ants, birds, and fish, in order to solve optimization problems [131–133]. The final category, physical-chemical systems, takes cues from the principles and phenomena inherent in physics and chemistry [134–136].

The choice of an optimization algorithm is contingent upon the distinctive attributes of the problem at hand. These attributes encompass elements such as the nature of the objective function, the imposed constraints, and the dimensionality of the search space. The objective function delineates the performance measure that the algorithm seeks to optimize, while constraints outline the permissible boundaries or conditions within which the solution must exist. The dimensionality of the search space, on the other

hand, refers to the number of parameters or variables that need to be optimized. Thus, a comprehensive understanding of these aspects is critical to select the most effective and suitable optimization algorithm for a given problem.

These nature-inspired optimization techniques have proven their efficacy in grappling with complex computational challenges, particularly those categorized as NP-hard [125]. An NP-hard problem is one for which no known algorithm can solve all instances quickly (in polynomial time), and a solution, once found, is not necessarily easy to verify. The ability of nature-inspired techniques to tackle these convoluted problems speaks to their robustness and adaptability, underscoring their growing popularity in the realm of optimization.

3.2 Optimization Algorithm for In-field Optimization

In the sphere of in-field optimization processes, the role of an AI or optimization agent becomes indispensable. It is vital for this agent to be embedded within the automatic test equipment (ATE) in a manner similar to the integration of the silicon lifecycle management (SLM) agent proposed by Synopsys (Concertio) [32, 137]. This AI agent can be positioned at varying levels within the system hierarchy, including the application layer, operating system, firmware, or hardware level [31,137], as illustrated in figure 3.1. ”

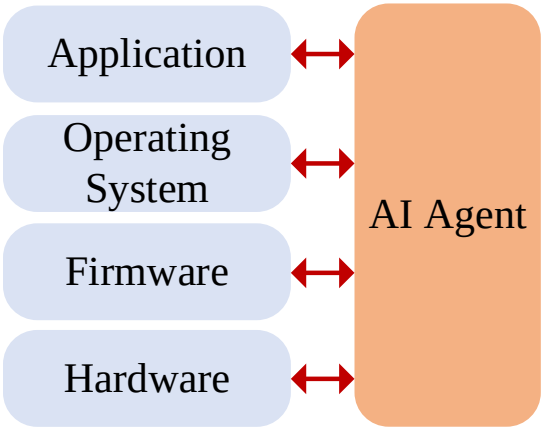

Figure 3.1: Illustration of potential AI agent placements across various levels of the system hierarchy.

As per the proposed methodology [100], the AI agent is positioned at the hardware

level, which is the closest level to the device under test (DUT). Concerning the selection of an optimizer for the calibration process, derivative-based optimizers are considered unfeasible due to the discontinuous nature of the objective space [138]. In contrast, meta-heuristic optimization algorithms have shown excellent effectiveness, regardless of the presence of discontinuities within the objective space. In order to meet the demands of complex search spaces and objective space optimization for smart sensory electronics (SSE), the conventional particle swarm optimization (PSO) [139] has been employed as an optimizer, following enhancements to its exploration capabilities. The primary reasons for selecting PSO as the optimization algorithm include its ease of implementation and rapid convergence rate [140].

3.3 Particle Swarm Optimization Algorithm

The particle swarm optimization (PSO) algorithm, introduced by Eberhart and Kennedy in 1995 [139], is an evolutionary computation technique inspired by the flocking behavior of birds and the schooling behavior of fish. It embodies an iterative method that seeks to improve candidate solutions with respect to a given measure of quality, usually in the form of a fitness function.

In PSO, each potential solution is conceptualized as a particle in a swarm, with each particle representing a solution for the given optimization problem. These particles are characterized by two vectors: the position vector and the velocity vector. The position vector corresponds to the values of each variable in the problem at hand, with its dimensionality equal to the number of parameters in the problem. For instance, if a problem involves two parameters, the particles would have position vectors in two dimensions. Consequently, each particle is capable of navigating an n-dimensional search space, where n denotes the number of variables involved in the problem.

The velocity vector plays a pivotal role in updating the position of the particles. This vector defines the magnitude and direction of the step size, effectively guiding the movement of each particle across each dimension independently. Therefore, the velocity vector is integral to determining how a particle explores the search space.

The position of the particles is updated at each iteration of the optimization process

according to the following equation:

$$\vec{x}i(t+1) = \vec{x}i(t) + \vec{v}_i(t+1) \tag{3.1}$$

where:

- $\vec{x}i(t+1)$ and $\vec{x}i(t)$ are the position of the i-th particle at time (t+1) and t respectively.
- $\vec{v}_i(t+1)$ is the velocity of the i-th particle at time (t+1).

This equation indicates that the position updating is straightforward, with the velocity vector being the primary determinant. The velocity vector is defined using Equation 3.2:

$$\vec{v}i(t+1) = w \cdot \vec{v}i(t) + c_1 \cdot rand_1 \cdot (\vec{p}best, i(t) - \vec{x}i(t)) + c_2 \cdot rand_2 \cdot (\vec{g}best(t) - \vec{x}i(t)) \tag{3.2}$$

where:

- $\vec{v}i(t+1)$ and $\vec{v}i(t)$ are the velocity of the i-th particle at time (t+1) and t, respectively.
- w is the inertia weight, which controls the momentum of the particles.
- c_1 and c_2 are cognitive and social scaling factors, respectively.
- $rand_1$ and $rand_2$ are random numbers in the range of [0, 1].
- $\vec{p}_{best,i}(t)$ is the best known position of the i-th particle until time t.
- $\vec{g}_{best}(t)$ is the best known position among all particles in the swarm until time t.
- $\vec{x}_i(t)$ is the current position of the i-th particle at time t.

Equation 3.2 balances the exploration (searching new areas) and exploitation (searching around the best-found solutions) during the search process. The terms involving c_1 and c_2 represent cognitive and social behavior, respectively. The cognitive component (c_1) pulls a particle towards its own best past position, while the social component (c_2) pulls the particle towards the best global position found in the swarm.

A well-tuned balance between these two components along with a suitable inertia weight can yield high-performing and robust optimization results, enabling the PSO algorithm to efficiently solve a wide range of complex optimization problems. This balance between position and velocity vectors lays the groundwork for various modifications and improvements on the PSO algorithm, as discussed in the following section.

3.3.1 Exploring Variations and Improvements of PSO

Building upon the foundation of PSO, many improved versions of the algorithm have been proposed over the last decade, aiming to extend its searching capability and minimize the probability of getting trapped into local minima [140, 141]. For instance, the linearly decreasing inertia weight (LDW-PSO) [39] modifies the inertia weight w (which appears in the velocity update equation 3.2) as follows:

$$w = w_{\max} - \text{currentIteration}\left(\frac{w_{\max} - w_{\min}}{\text{maxIteration}}\right) \tag{3.3}$$

where $w_{\min}$ and $w_{\max}$ represent the minimum and maximum value of the inertia weight w, respectively; $currentIteration$ denotes the current running iteration number, and $maxIteration$ represents the maximum number of iterations. Usually, a larger value of w achieves the global optimum exploration, and a smaller value performs the local exploitation. The PSO algorithm with linearly varying acceleration coefficients (LAC-PSO) was presented in [142]. The cognitive scaling factor or acceleration coefficient c_1 is linearly decreasing, while the social scaling factor or acceleration coefficient c_2 is linearly increasing, as follows:

$$c_1 = (c_{1f} - c_{1i}) \times \frac{\text{maxIteration} - \text{currentIteration}}{\text{maxIteration}} + c_{1i} \tag{3.4}$$

$$c_2 = (c_{2f} - c_{2i}) \times \frac{\text{maxIteration} - \text{currentIteration}}{\text{maxIteration}} + c_{2i} \tag{3.5}$$

where $c_{1i,2i}$ and $c_{1f,2f}$ represent the initial and final values of the acceleration coefficients respectively. Reference [143] recently proposed the sigmoid function based adaptive acceleration coefficients adjustments. These adjustments affect the cognitive and social components of the velocity update equation 3.2, resulting in significant alterations in the exploration-exploitation trade-off. These adjustments are given as:

$$c_1 = c_2 = F(D) = \frac{a}{1 + e^{-c(D-d)}} + b \tag{3.6}$$

where , $a = 0.5$, $b = 1.5$, $c = 0.0000353.81 \times$ search range (distance between upper and lower bound of particle), $d = 0$ and $D = P_{p \text{ or } g}(k) - x_i(k)$ represents the distance of the i^{th} particle to its personal or global best at the k^{th} iteration.

This continued research into the potential of PSO is also seen in the introduction of various topologies and updating strategies, including the pyramid, clusters, von Neumann, and ring structures [82,144]. Each of these variants introduces new elements into the fundamental structure of the PSO, allowing for greater flexibility and adaptability in solving complex optimization problems.

It is also noteworthy to mention the research on biological and sociological inspired methods, such as the aging theory-based PSO algorithm, the cultural-based PSO algorithm, and the niching PSO algorithm [145–148]. These modifications look to nature and society for inspiration, bringing novel perspectives into the algorithmic design of the PSO.

However, despite the advancements, the continuous research and development of these PSO algorithms are crucial, especially for complex, high-dimensional, multi-objective search spaces with many local optima, such as in the case of SSE optimization [120, 140, 149]. These challenging domains remain the frontier of PSO research, inviting novel modifications and applications of the algorithm.

3.4 Proposed Experience Replay Particle Swarm Optimizer

This section presents the experience replay particle swarm optimizer (ERPSO), an innovative optimization algorithm specifically developed in this research work to enhance the exploration capabilities of the conventional PSO algorithm. Drawing inspiration from nature, ERPSO mimics the behavior of birds, which not only remember their current globally best location (gbest) when searching for food but also retain memories of previous global best locations. In this algorithm, an experience replay buffer (ERB) functions similarly, solving complex objective space problems like SSE.

ERPSO builds on the classical PSO by incorporating a random selection of historical

global bests (gbests) via an ERB. This novel integration of an ERB into the velocity updating equation (VUE) provides ERPSO with unique characteristics. Just like birds recalling past food sources, the ERB archives previously visited gbest particles and leverages this collective memory to improve convergence accuracy. This approach is commonly used in reinforcement learning, as shown in references [150, 151].

The ERB minimizes the risk of getting stuck in local minima by drawing from past experience rather than relying solely on recent data. An adaptive epsilon-greedy algorithm is used to select from the ERB, striking a balance between exploration and exploitation [152]. The fundamental VUE of ERPSO is formulated as follows:

$$V_i^{j+1} = \begin{cases} wr_1V_i^j + c_1r_2(P_i^j - X_i^j) + c_2r_3(G^j - X_i^j) & \varepsilon < \eta * w \\ wr_1V_i^j + c_1r_2(P_i^j - X_i^j) + c_2r_3(G^j - X_i^j) + c_3r_3(A^j - X_i^j) & \varepsilon \geq \eta * w \end{cases} \tag{3.7}$$

where:

- V_i^j represents the velocity of the i^{th} particle in the j^{th} iteration.
- w is the inertia weight, with the value defined by equation 3.3.
- $r_{1,2,3}$ are uniformly distributed random numbers in the range [0, 1].
- c_1 and c_2 are the cognitive and social coefficients, respectively, with $c_1 = c_2 = c_3 = 2$.
- P_i^t and G^t are the personal and global best information of the whole swarm.
- ε is a random variable introduced to balance the exploration and exploitation through the epsilon greedy algorithm.
- η denotes the intensity factor that controls the exploration and exploitation.
- A^t represents the archive of previously visited global best positions of the swarm.

The position update equation of ERPSO is given as follows:

$$X_i^{j+1} = X_i^j + V_i^{j+1} \tag{3.8}$$

where X_i^j represents the position of the i^{th} particle in the j^{th} iteration. According to the proposed VUE, the particles attempt to converge rapidly towards the global optimum with a probability of $1 - \varepsilon$. As such, the VUE of the conventional PSO algorithm is employed for the initial scenario. Conversely, to diminish the chance of premature convergence, the ERPSO algorithm employs the epsilon greedy algorithm to stimulate recall of past gbest solutions from the experience replay archive with a probability of ε.

As depicted in figure 3.2, the ERPSO algorithm starts by randomly initializing the positions and velocities of all particles in the swarm. This initialization provides a diverse range of solutions and establishes the starting point for the optimization process.

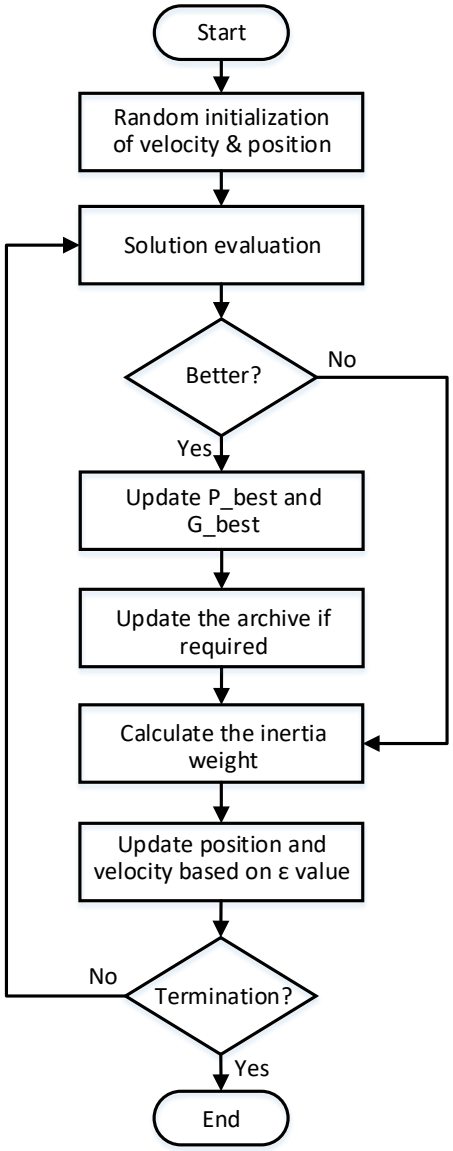

Figure 3.2: Flow diagram of the proposed ERPSO algorithm.

After the initialization stage, the fitness value for each particle is calculated. The

fitness value is a measure of the quality of the solutions provided by the particles. It quantifies how closely a particle's position matches the desired objective. These fitness values are essential as they determine which particles possess the best positions globally (gbest) and personally (pbest).

Following the fitness evaluation, each particle's fitness value is compared to its personal best (pbest) and the global best (gbest). If a particle's fitness surpasses its own pbest or the swarm's gbest, the particle's respective personal and global data are updated. This update means that the swarm has now discovered a better solution.

Concurrently, the inertia weight w, which balances the global and local search abilities of the swarm, is calculated according to equation 3.3. The inertia weight plays a crucial role in the ERPSO algorithm's convergence behavior and solution quality.

In the subsequent stage, the velocity of each particle is updated using the VUE. This update process considers the random variable ε and depends on whether ε is less than or greater than the product of the intensity factor η and the inertia weight w. Depending on this condition, the velocity update may or may not consider the archive of previously visited gbest positions, A^t.

Once the velocities have been updated, the position of each particle is adjusted based on its new velocity. The position adjustment nudges the particles closer to the areas of the search space with higher fitness values.

These steps, from the fitness evaluation to position adjustment, constitute a single iteration of the ERPSO algorithm. The algorithm proceeds with these iterations until it reaches a predetermined maximum number of iterations or another stopping criterion. Throughout this iterative process, the ERPSO algorithm progressively refines the solutions, steering the swarm towards the optimal solution.

3.4.1 Finding the Optimal Metaparameters for ERPSO

To achieve optimal performance with ERPSO, finding the appropriate metaparameters is crucial. The most significant parameters include the inertia weight (w), cognitive and social coefficients (c_1 and c_2), and the epsilon-greedy intensity factor (η).

Inertia Weight (w): A lower value favors exploitation, while a higher value promotes exploration. A balance must be struck to achieve optimal convergence rates.

Cognitive and Social Coefficients (c_1, c_2): These coefficients influence personal

and social influences on particle movement. Adjusting these values affects the particles' trajectories toward individual or global bests.

Epsilon-Greedy Intensity Factor (η): This controls the trade-off between exploration and exploitation. Higher values lead to more exploration through the ERB, while lower values lean toward exploitation.

Random Variables ($r_{1,2,3}$): Uniformly distributed random variables ensure diverse solution exploration.

The impact of each parameter on the algorithm's performance is thoroughly examined, ensuring that the chosen configuration minimizes premature convergence and enhances global optimality, particularly for the SSE objective space.

By leveraging the ERB and integrating the epsilon-greedy approach, the ERPSO algorithm presents a robust technique for overcoming local optima and premature convergence, issues commonly faced by the conventional PSO. As a result, it demonstrates higher efficacy in navigating complex, multimodal search spaces and achieving superior optimization results.

The effectiveness and efficiency of the ERPSO algorithm are validated in the subsequent section by testing it on a range of diverse and challenging benchmark functions. These tests will provide a comprehensive understanding of the algorithm's performance, assessing its robustness, versatility, and adaptability across various optimization landscapes.

3.4.2 Performance Evaluation of ERPSO on Benchmarking Functions

In evaluating the performance of the ERPSO on benchmarking functions, eight distinct benchmarking functions (BMFs) are employed, selected from existing literature to offer a comprehensive view of the optimization behavior of the ERPSO. Table 3.1 presents the specifics of these BMFs, encapsulating their respective names, dimensions, search space spans, and global best values.

These BMFs represent high-dimensional problems, mimicking the search space complexity of SSE. Among them, the Griewank function $f_1(x)$ is typically employed to examine the convergence rate of optimization algorithms due to its popularity in this context. The Rastrigin function $f_2(x)$ and Ackley function $f_3(x)$ present considerable optimization challenges owing to their numerous local optima. Furthermore, the Rosen-

Table 3.1: Configuration of benchmarking functions (BMF).

Function Name	**Functions**	**Dimension**	**Search Space**	**Global Minima**
Griewank	$f_1(x)$	25	$[-600, 600]$	0
Rastrigin	$f_2(x)$	25	$[-5.12, 5.12]$	0
Ackley	$f_3(x)$	25	$[-32, 32]$	0
Rosenbrock	$f_4(x)$	25	$[-30, 30]$	0
Schwefel 1.2	$f_5(x)$	25	$[-100, 100]$	0
Schwefel 2.22	$f_6(x)$	25	$[-100, 100]$	0
Levy	$f_7(x)$	25	$[-10, 10]$	0
Sphere	$f_8(x)$	25	$[-100, 100]$	0

brock function $f_4(x)$, also referred to as the Valley or Rosenbrock's Banana function, and the Levy function $f_7(x)$, are non-convex functions. The Schwefel 1.2 function $f_5(x)$ and Schwefel 2.22 function $f_6(x)$ are representative of typical multimodal and unimodal functions respectively, each of which possesses its own challenges in locating the global optimum. Lastly, the Sphere unimodal function $f_8(x)$ is utilized to scrutinize the convergence rate.

The experimental setup involves 30 particles, 25 dimensions, and 5000 iterations. Each experiment is repeated 100 times to mitigate the effects of random fluctuations or lucky shot results. The performance of the ERPSO algorithm is evaluated against four well-known PSO algorithms, namely, LDW-PSO, LAC-PSO, PSO, and SPSO. The convergence curves of the ERPSO algorithms are depicted in Figure 3.3, where the horizontal axis signifies the number of iterations and the vertical axis represents the mean fitness value (logarithmic scale) across all the PSO algorithms.

Upon analyzing these convergence curves, one can observe that the PSO and LAC-PSO display a significantly quicker convergence rate compared to the ERPSO algorithm. Nevertheless, the ERPSO algorithm achieves a superior fitness value for the global minimum, surpassing the other PSO algorithms. This stellar performance across all optimization BMs testifies to ERPSO's exceptional capability to avoid local optimum trapping. In the context of the Ackley and Levy function, the proposed ERPSO algorithm's performance is on par with LDW-PSO and surpasses the other algorithms. While the sphere function shows slightly less convergence for the ERPSO algorithm, it still successfully identifies the global optimum. The convergence rate of ERPSO could potentially be improved by reducing the exploration intensity η. However, considering the complexity of the SSE search space, exploitation is given preference over exploration.

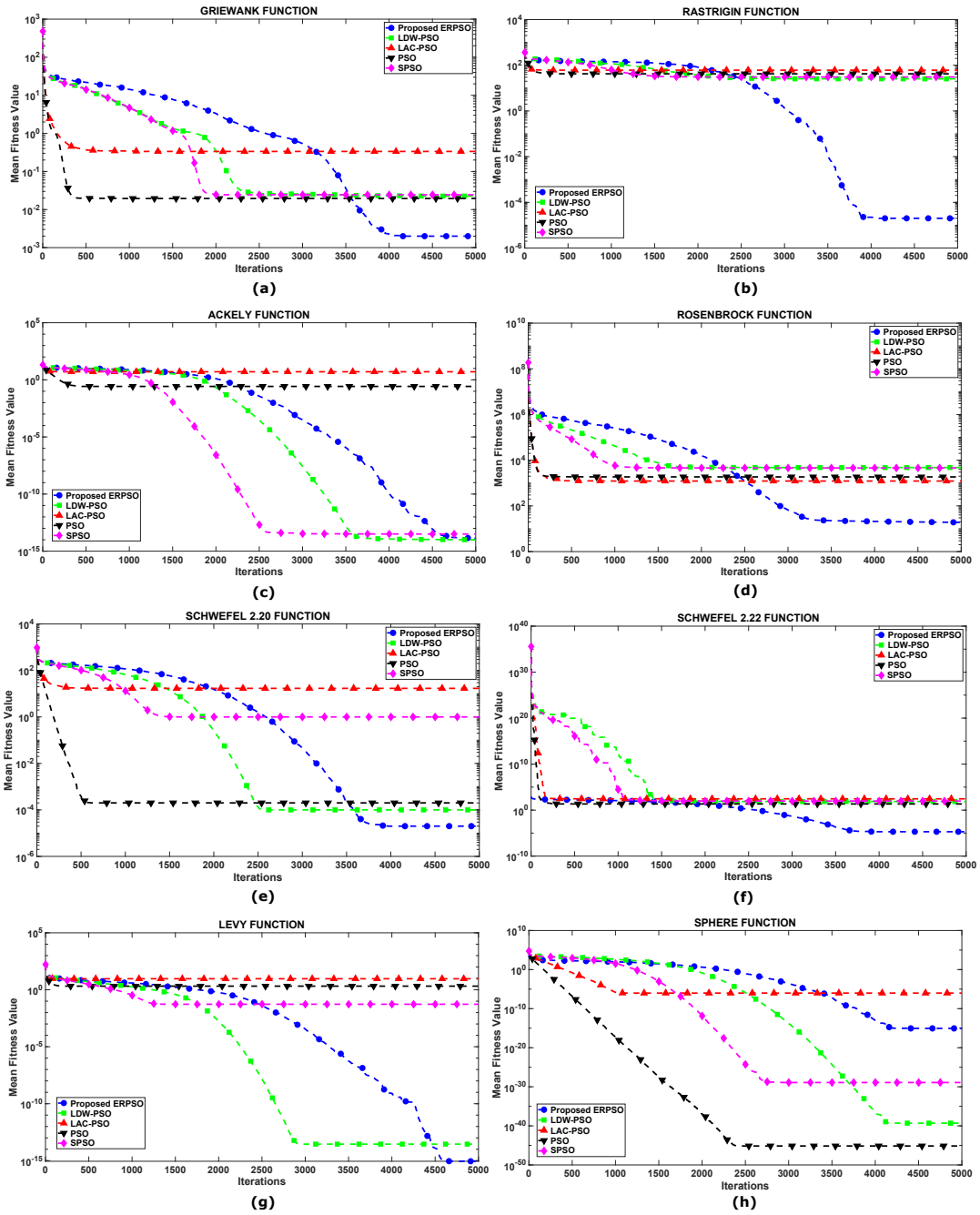

Figure 3.3: Optimization convergence curves for (a) Griewank function $f_1(x)$ (b) Rastrigin function $f_2(x)$ (c) Ackley function $f_3(x)$ (d) Rosenbrock function $f_4(x)$ (e) Schwefel 1.2 function $f_5(x)$ (f) Schwefel 2.22 function $f_6(x)$ (g) Levy function $f_7(x)$ (h) Sphere function $f_8(x)$.

Additionally, Table 3.2 offers a deeper insight into the optimization process, providing statistical data about the fitness value (minimum, mean, and standard deviation) of the various PSO algorithms for each BMF, and including the successful ratio of convergence. In most cases, the mean value of ERPSO is lower than the other PSO algorithms, suggesting ERPSO's superiority in achieving the global minima. As observed in the

Table 3.2: Comparison of different PSO algorithms on eight optimization BMF.

		PSO	**SPSO**	**LDW-PSO**	**LAC-PSO**	**ERPSO**
$f_1(x)$	Min	0.00	0.00	0.00	9.20×10^{-6}	0.00
	Mean	1.95×10^{-2}	2.40×10^{-2}	2.26×10^{-2}	3.40×10^{-1}	7.48×10^{-14}
	Std	2.77×10^{-2}	2.75×10^{-2}	2.34×10^{-2}	5.90×10^{-1}	6.44×10^{-13}
	Ratio	100%	96%	97%	37%	100%
$f_2(x)$	Min	1.89×10^{1}	9.95×10^{0}	8.95×10^{0}	6.10×10^{1}	0.00
	Mean	4.22×10^{1}	3.06×10^{1}	1.03×10^{1}	3.08×10^{1}	4.83×10^{-15}
	Std	1.43×10^{1}	1.11×10^{1}	2.34×10^{-2}	1.68×10^{1}	1.34×10^{-14}
	Ratio	0%	0%	0%	0%	100%
$f_3(x)$	Min	4.44×10^{-15}	7.99×10^{-15}	4.40×10^{-15}	1.80×10^{0}	8.88×10^{-16}
	Mean	2.60×10^{-1}	3.16×10^{-14}	9.91×10^{-15}	1.68×10^{0}	1.36×10^{-14}
	Std	5.91×10^{-1}	6.99×10^{-14}	3.44×10^{-15}	1.68×10^{1}	8.63×10^{-15}
	Ratio	82%	100%	100%	0%	100%
$f_4(x)$	Min	6.50×10^{-3}	1.90×10^{-1}	1.67×10^{-1}	7.58×10^{0}	3.17×10^{-3}
	Mean	1.85×10^{3}	4.57×10^{3}	4.77×10^{3}	1.22×10^{3}	1.89×10^{1}
	Std	1.26×10^{4}	1.97×10^{4}	1.96×10^{4}	9.01×10^{3}	1.79×10^{1}
	Ratio	4%	0%	0%	0%	7%
$f_5(x)$	Min	0.00	3.81×10^{-22}	3.81×10^{-14}	4.20×10^{-1}	0.00
	Mean	4.92×10^{-14}	1.00×10^{0}	2.42×10^{-12}	1.69×10^{1}	1.44×10^{-15}
	Std	8.84×10^{-13}	1.00×10^{1}	1.04×10^{-11}	2.22×10^{1}	1.23×10^{-14}
	Ratio	100%	99%	100%	0%	100%
$f_6(x)$	Min	8.12×10^{-65}	1.05×10^{-17}	1.98×10^{-28}	2.84×10^{0}	0.00
	Mean	2.20×10^{1}	6.11×10^{1}	7.30×10^{1}	2.82×10^{2}	4.88×10^{-13}
	Std	4.83×10^{1}	7.23×10^{1}	8.39×10^{1}	1.51×10^{2}	2.56×10^{-12}
	Ratio	81%	51%	48%	0%	100%
$f_7(x)$	Min	1.49×10^{-32}	1.50×10^{-32}	1.47×10^{-32}	2.41×10^{0}	4.13×10^{-31}
	Mean	2.08×10^{0}	2.91×10^{-18}	3.44×10^{-14}	9.28×10^{0}	1.22×10^{-15}
	Std	2.05×10^{0}	1.96×10^{-17}	1.30×10^{-12}	4.26×10^{0}	1.10×10^{-14}
	Ratio	23%	100%	100%	0%	100%
$f_8(x)$	Min	0.00	0.00	0.00	0.00	0.00
	Mean	2.90×10^{-45}	4.11×10^{-27}	2.90×10^{-40}	5.51×10^{-8}	1.58×10^{-13}
	Std	2.01×10^{-44}	4.10×10^{-26}	1.97×10^{-39}	1.16×10^{-7}	9.16×10^{-12}
	Ratio	100%	96%	99%	100%	100%

convergence curves, the convergence rate of ERPSO is slower than that of the other PSO algorithms, which is evident in this table by the mean value of the $f_8(x)$. Regardless, the proposed ERPSO algorithm finds the global minima with an improved mean value for other BMFs. Moreover, the convergence performance ratio (CPR) is another crucial metric to evaluate the algorithms' success in reaching the global optimum. Different variants of the PSO algorithms demonstrate quite low CPR, as seen in the Rastrigin function due to its vast local optima. Conversely, the proposed ERPSO exhibits a much higher CPR value, thanks to its extended exploration abilities. Despite a lower CPR in the Rosenbrock function optimization, the EPRSO still performs significantly better than the other algorithms.

Chapter 4

Proposed Design Methodology

In the ever-evolving field of smart sensory electronics, achieving both efficiency and reliability poses unique challenges, especially under varying and unpredictable environmental conditions. This chapter introduces a multi-dimensional design methodology to tackle these challenges, combining robust optimization techniques with innovative indirect measurement methods for in-field performance optimization.

A cornerstone of this methodology is the use of total harmonic distortion (THD) as a key metric for indirect performance evaluation. Leveraging a fully differential indirect current feedback instrumentation amplifier (CFIA) as the device under test (DUT), the framework employs THD to provide a holistic, low-cost assessment of system performance. This indirect measurement approach is augmented by advanced robust optimization techniques, specifically surrogate-based and archive-based robust optimization. These methods employ the experience replay particle swarm optimization (ERPSO) algorithm to consider multiple objectives, including THD and power efficiency, thereby offering a nuanced approach to optimizing complex electronic systems.

Further enriching the methodology, the chapter explores the use of non-intrusive sensors for indirect measurement. These sensors are placed near the DUT to experience identical process, voltage, and temperature (PVT) variations, thus ensuring accurate and consistent environmental impact measurements. A regression model correlates these sensor readings with the performance metrics of the DUT, providing an additional layer of indirect, yet efficient, performance estimation.

An application of this methodology is its incorporation into optimizing an anti-aliasing filter, which plays a crucial role in signal conditioning. Specifically, based on

the Sallen-Key architecture with a Butterworth approximation, this filter ensures noise elimination within the Nyquist bandwidth preceding its conversion by the ADC. Such an approach paves the way for an extended bandwidth range, but tuning over this range traditionally necessitated resource-intensive measurements. To address this, the methodology introduces a non-intrusive sensor-based indirect measurement, making the tuning process both cost-effective and efficient without disrupting the DUT's operation.

Throughout this methodology development, this work predominantly focused on the EDA aspect, involving tuning knobs, extrinsic optimization, and OCeaN programming. This emphasized designing and implementing efficient optimization algorithms and measurement strategies that complement circuit-level development.

By integrating low-cost indirect measurement techniques such as THD, robust optimization strategies, and non-intrusive sensing methods, this chapter aims to offer a comprehensive approach to optimizing complex sensory electronics. Subsequent sections will elaborate on the technical intricacies of CFIA, power monitoring modules (PMM), and the various optimization and measurement strategies discussed.

4.1 THD-Based Power-Efficient Indirect Measurement Method

As shown in Figure 4.1, the block diagram presents the proposed methodology designed to implement a low-cost indirect performance measurement for smart sensory electronic systems [97]. This approach uses a reconfigurable fully differential indirect current feedback instrumentation (CFIA), an essential component of the readout sensory electronics, as a test vehicle for intrinsic assessment of the proposed framework. The process starts with the digital-to-analog (DAC) converter of the Red Pitaya, which generates a sinusoidal signal of a defined amplitude and frequency. This signal is then fed into the CFIA to serve as a cost-effective test stimulus for the in-field optimization procedure. Subsequently, the CFIA's output is captured by the Red Pitaya board's high-speed analog-to-digital converter (ADC). The THD is evaluated from this sampled response, allowing for the simultaneous prediction of multiple performance characteristics of the CFIA by using single test stimuli.

An underpinning principle of this methodology is the insight that design imper-

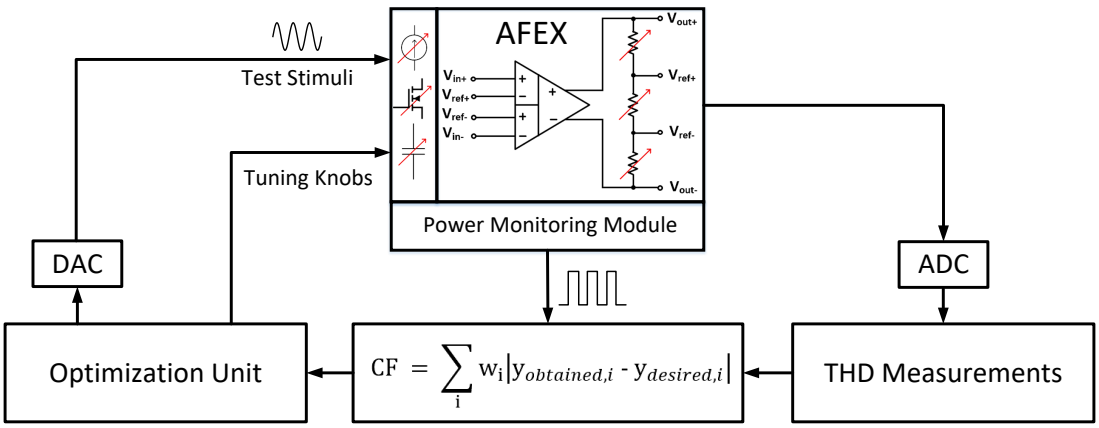

Figure 4.1: The block diagram of the proposed methodology of power efficient THD based indirect measurement method for AFEX.

fections like input common-mode range (ICMR), slew rate, gain-bandwidth product (GBW), full-power bandwidth, effective number of bits, and signal-to-noise ratio (SNR) manifest as nonlinear distortion at the output of the closed-loop amplifier. Optimizing evolvable analog circuits at the transistor level can lead to undesirable outcomes, like high currents that can either permanently damage the DUT or shorten its life cycle. This contrasts with the optimization of digital evolvable hardware, such as field-programmable gate array (FPGA) optimization, which doesn't present such risks. In order to tackle this problem, improve long-term reliability, and enhance the power efficiency of the CFIA, a cost-effective indirect PPM has been integrated alongside a THD-based optimization approach. Finally, the proposed experience replay particle swarm optimization (ERPSO) a modified variant of PSO [100] , is selected as the optimization unit.

4.1.1 Indirect Current-Feedback Instrumentation Amplifier

The instrumentation amplifier (In-amp) serves as the fundamental element of the AFE circuitry for the sensor signal conditioning and interfacing [153]. There are three primary topologies for designing in-amp circuits [154]. These include the capacitive coupling chopper-stabilized in-amp (CCIA) [155], the conventional in-amp that utilizes three operational amplifiers (op-amps), and the indirect current-feedback in-amp (CFIA) [156]. The CFIA operates on the basis of the active feedback amplifier (AAF) topology [157], which is alternatively known as the differential-difference amplifier (DDF) [158]. This design offers multiple advantages, including a high input impedance, substantial open-loop DC gain, and an expansive bandwidth [159]. When compared to the 3-opamp in-amp,

the CFIA stands out for its efficiency in both area and power. This is because its input and feedback transconductance stages utilize a unified output driver stage [153].

One distinctive property of the CFIA is its ability to separate and insulate the input stage's common-mode voltage from the feedback stage. This is accomplished through the implementation of two balanced differential stages [160], as depicted in Figure 4.2. This architectural choice facilitates the direct connection of sensor pairs with different common-mode voltages to the CFIA's output common-mode voltage. The input and feedback transconductance stages convert voltage signals into current signals while rejecting the common-mode voltage efficiently. This results in the CFIA boasting a higher CMRR compared to the 3-opamp in-amp [161]. Moreover, mismatches in the feedback resistor only affect closed-loop gain inaccuracy error [162] without detrimentally affecting the CMRR performance.

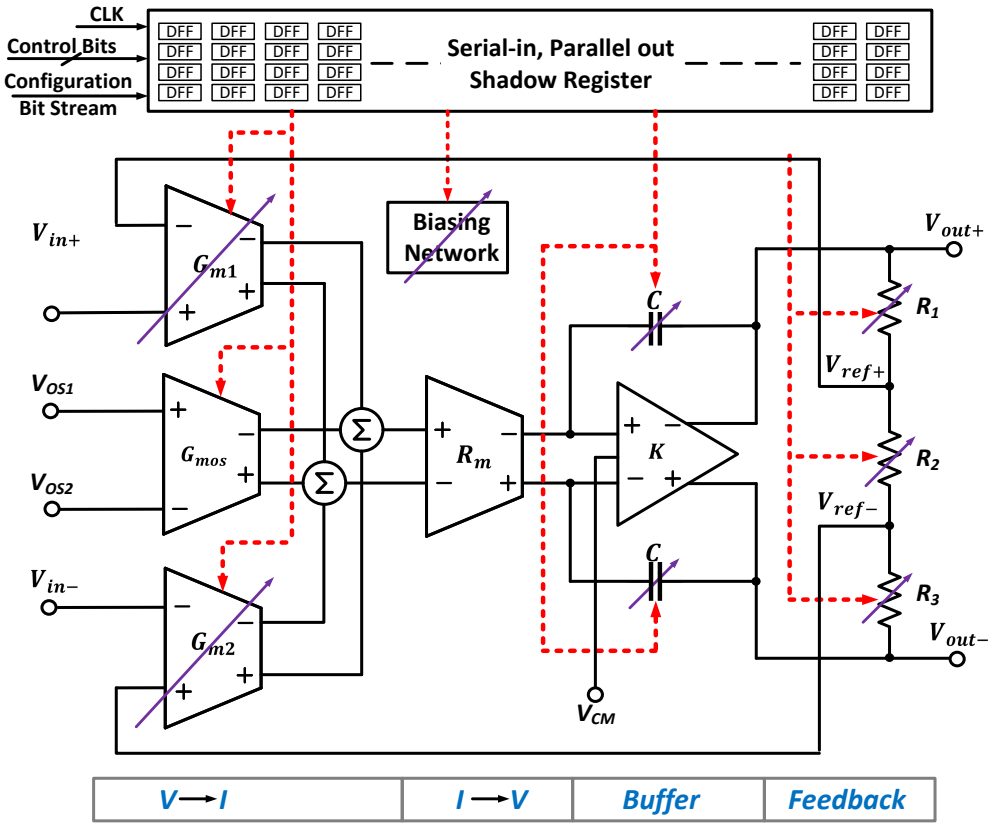

Figure 4.2: The block diagram of the proposed configurable fully-differential indirect current feedback instrumentation amplifier (CFIA).

Depending upon whether the input stage is NMOS or PMOS, the CFIA can amplify sensor voltages that approach either of the power supply rails, making it versatile for conditioning a diverse range of sensors. However, the CFIA has challenges, especially

when associated with the DDF core amplifier. The primary challenge is a gain inaccuracy error from the mismatch between the input and feedback transconductances. Nonetheless, this issue can be mitigated through the utilization of identical types of differential transistors for both the input and feedback stages and ensuring layout matching during the physical design phase.

Furthermore, the implementation of cascoded biasing currents offers the potential for achieving a higher degree of matching between transistors. The second issue arises from the constrained input differential range inherent to the input transconductance stage when operating in an open-loop configuration [158]. This constraint becomes acutely problematic when the CFIA is interfaced with high dynamic range sensors, such as those based on magnetoresistive technology. To mitigate this limitation, a novel approach was presented in [163], where a wide input range fully differential CFIA architecture was proposed. This architecture is based on the fully-balanced DDF topology [164]. This approach facilitated the simultaneous attainment of remarkable dynamic performance as well as extensive input range functionality.

To enable self-X features within the CFIA, configurable functionalities are integrated into the critical components of the circuit, as well as those elements that substantially impact circuit performance. The identification of these critical components is accomplished by applying an optimization algorithm to the CFIA and employing extrinsic optimization techniques [165, 166]. This is followed by a subsequent evaluation of the CFIA's performance. These selected components serve as tuning knobs for adjusting the performance parameters of the CFIA [37]. Their roles and placements within the circuit are illustrated in Figure 4.2 and indicated by arrow symbols. These elements are composed of digitally-weighted, scalable arrays that are controlled by configuration bits, generated by the optimization algorithm. To accelerate the optimization process, a shadow register memory featuring four rows is utilized for storing these configuration bits. This enables seamless transitions, commonly known as 'hot swapping,' between various pre-stored configurations, thereby enhancing optimization efficiency.

The presented design features programmable GBW functionality, accomplished through the fine-tuning of compensation capacitors to align with the stability criteria corresponding to the selected gain level. The design offers a selection of eight discrete gain levels, encompassing 1, 2, 4, 8, 16, 32, 64, and 128. Furthermore, the ability

to program the biasing current facilitates precise control over both the amplifier's non-dominant and dominant poles. This attribute significantly contributes to restoring the stability of the CFIA when faced with an unstable operational state.

Figure 4.3 illustrates the schematic diagram of the CFIA circuit, encompassing the PMM. Further details about the PMM will be presented in the next section. The amplifier utilizes a buffered class AB topology [97]. Additionally, a common-mode feedback amplifier (CMFB) is integrated to ensure the CFIA's output common-mode voltage remains in proximity to the desired voltage (V_{CM}). In order to optimize the output dynamic range, the value of V_{CM} is set precisely at the midpoint of the supply voltage, specifically at 1.65 V. As a result of employing NWELL CMOS technology, the bulk connections of NMOS transistors are tied to the ground, whereas those of PMOS transistors are connected to V_{DD}, unless explicitly stated otherwise. The power-down scheme is depicted in blue color, omitting the biasing circuit and programmable current source for clarity and simplicity. The Figure 4.4 displays the adjustable input and feedback transconductance (G_{m1} and G_{m2}) components.

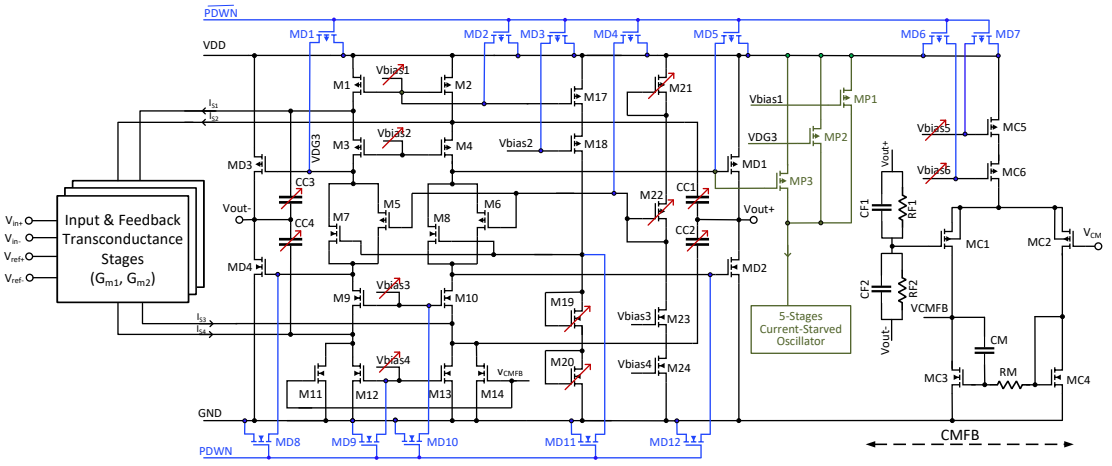

Figure 4.3: CFIA schematic diagram integrating the power monitoring module.

This architecture consists of three configurable stages, each of which can be multiplexed in accordance with both common-mode and differential-range voltages. The first stage is particularly well-suited for applications where sensor signals demonstrate high dynamic ranges and are centered around the midpoint of the CFIA's operational supply voltage. The second and third stages are augmented with degeneration resistors, offering advantages particularly when the sensor's common-mode voltage approximates either G_{ND} or V_{DD}, respectively. For additional details on the transistor dimensions used

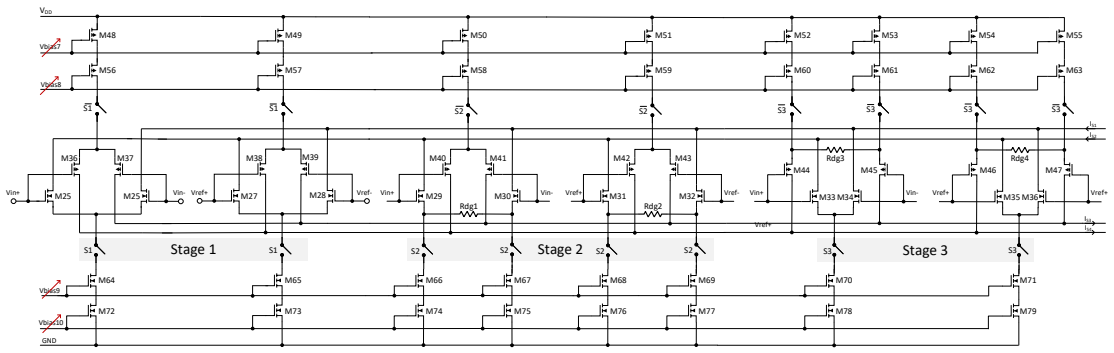

Figure 4.4: The configurable input and feedback transconductance of the CFIA.

in this configuration, reference may be made to publications authored by the research group [36, 37, 167].

4.1.2 Power Monitoring Module (PMM)

A widely used method for determining circuit current in the printed circuit board (PCB) community involves detecting the voltage drop on a small current-sense resistor (CSR) located on the main supply voltage path. This is accomplished through the use of a differential amplifier and an analog to digital converter [168]. There are several considerations that must be taken into account when using this approach. Firstly, the voltage drop on the CSR should not significantly reduce the circuit headroom voltage when high current flows through it. Secondly, the resistor tolerances to process variation and temperature drift should be negligible for precise measurement, which can be difficult to achieve using on-chip sheet resistors without trimming technologies. Thirdly, the CSR must be able to safely dissipate the generated power.

Moreover, the main issue with this approach is that it measures the power on the main supply rails, which may be shared with different circuits powered by the same power pads and supply ring. Therefore, it is not possible to measure the power of individual circuits using this method unless individual power monitoring schemes are incorporated and the supply rails and pads are separated, resulting in additional design constraints.

In certain scenarios, it may be sufficient to detect the threshold value of power, rather than measuring its absolute value. In [169, 170], the authors proposed a simple method for detecting maximum power using a basic current sense sensor. However, this approach shares the same issue as the previous method by utilizing a current sensing resistor in the supply rail path. In the work presented in [167], an alternative methodology

for indirectly estimating the current consumed by a CFIA circuit is introduced. This achievement is facilitated by transferring a scaled-down version of the circuit's current into a current-starved ring oscillator, as illustrated in Figure 4.3 by the components marked in green, with a scale-down factor of 240:1. The modulation of the drawn current, and correspondingly the power dissipation, manifests as changes in the clock frequency. The digital processing unit in smart sensory electronics can easily interpret the resultant signal. Due to the direct proportionality between the output frequency and the current drawn, this approach serves dual purposes: it not only identifies the power threshold value but also provides a reliable estimate of power consumption for diverse optimization strategies.

4.1.3 Experience Replay Particle Swarm Optimization

In the work outlined in [100], the experience replay particle swarm optimization algorithm (ERPSO) is introduced as the optimization unit underpinning the approach presented in this study. The schematic representation of the design methodology's flow is depicted in Figure 4.5. The optimization process begins with the random initialization of each particle's velocity and position parameters. Following this initialization, a fast Fourier transform (FFT) is executed on output response of the CFIA. For this analysis, a sinusoidal signal characterized by a known fundamental frequency is deployed as the test stimulus. The THD value is subsequently computed from the resulting output spectrum. Concurrently, the power consumption for the generated solution is approximated utilizing the embedded indirect PMM. The quantified values of power consumption and THD serve as objective functions, or fitness values, which guide the optimization process executed by the ERPSO algorithm. In the ensuing phase, the algorithm revises either the individual or collective best positions based on the fitness values, making adjustments as necessary.

To optimize the balance between explorative and exploitative behaviors within the search space, modifications are applied to the velocity update equation (VUE) of the standard PSO algorithm. Specifically, historical data regarding previously visited global best positions are incorporated into the VUE. The selection among these options is implemented using an epsilon-greedy algorithm. In accordance with the newly proposed VUE, particles are probabilistically inclined to converge swiftly toward the globally opti-

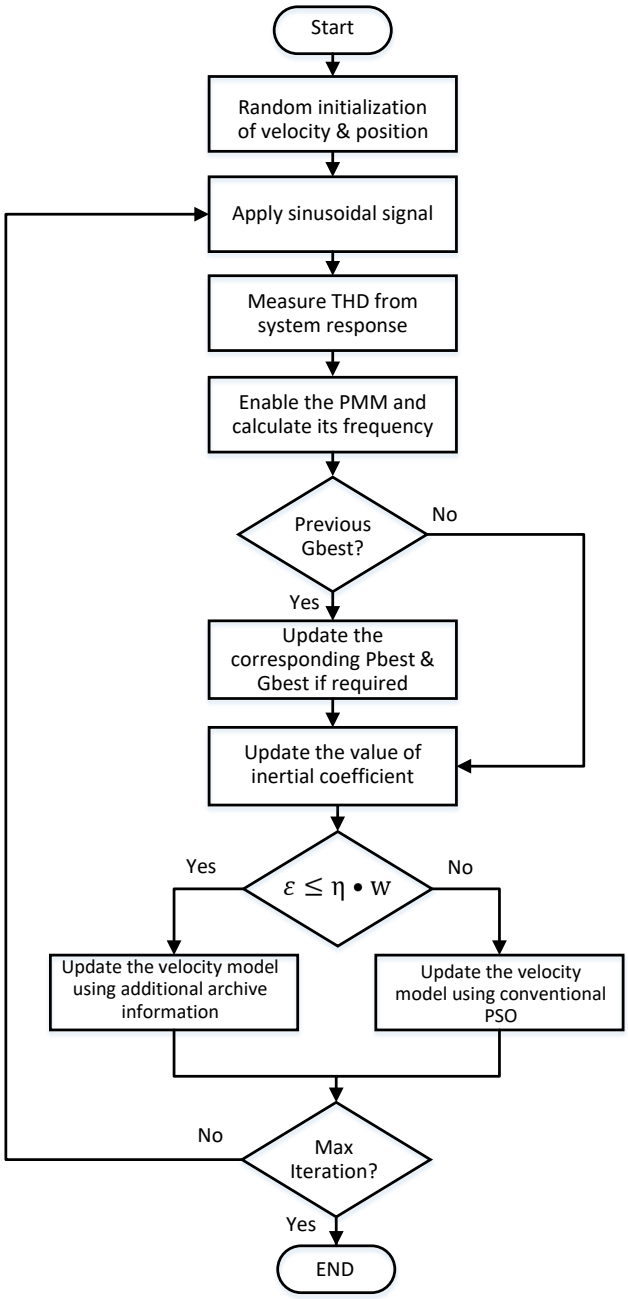

Figure 4.5: The proposed optimization methodology flow chart incorporating the ERPSO algorithm, PMM, and THD-based low-cost indirect measurements.

mal solution with a probability of 1 - ϵ. Consequently, for the first optimization scenario, the VUE of the traditional PSO algorithm is employed. To minimize the probability of premature convergence, an alternate mechanism is introduced: the ERPSO algorithm stochastically selects a historical global best position from an experience replied buffer (ERB) with a probability of ϵ. This iterative procedure continues until a predefined maximum number of iterations has been achieved.

4.1.4 Robust Optimization for Observer Imperfections

4.1.4.1 Surrogate-Based Robust Optimization

In the work detailed in [114], a block diagram illustrating the surrogate-based robust optimization methodology is presented in Figure 4.6. The DUT in this experiment employs CFIA, while ERPSO serves as the optimization algorithm. The Gaussian process regression (GPR) module evaluates the output response from the DUT to predict the level of uncertainty. Subsequently, a THD-based low-cost performance measurement approach is implemented, as explained in the previous section.

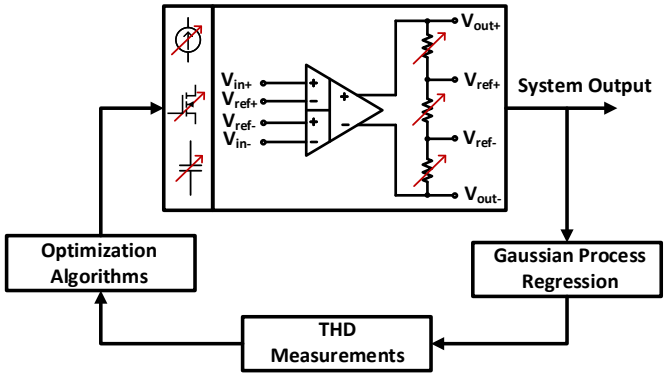

Figure 4.6: Block diagram of proposed surrogate-based robust optimization.

The schematic representation of the proposed THD-based low-cost robust particle swarm optimizer is depicted in Figure 4.7. The method initiates similarly to the original ERPSO-based optimization framework in the modified flow diagram. It commences with randomly initializing each particle's position and velocity parameters. Following this, a sinusoidal input signal is applied to the DUT. Unique to this adapted scheme is the subsequent utilization of GPR for uncertainty estimation related to the DUT's output.

Gaussian Process Regression is a form of constrained regression used to create surrogate models [116]. Mathematically, the GPR model is expressed as:

$$f(x) \sim GP\left(m(x), \kappa\left(x, x'\right)\right) \tag{4.1}$$

Here m(x) denotes the mean function, and $\kappa\left(\mathrm{x}, \mathrm{x}'\right)$ signifies the kernel function. The experiment optimizes Gaussian process regression (GPR) by fine-tuning the mean and kernel functions based on the training data set. Specifically, a combination of a white kernel, which captures noise variations, and an exponential sine squared kernel,

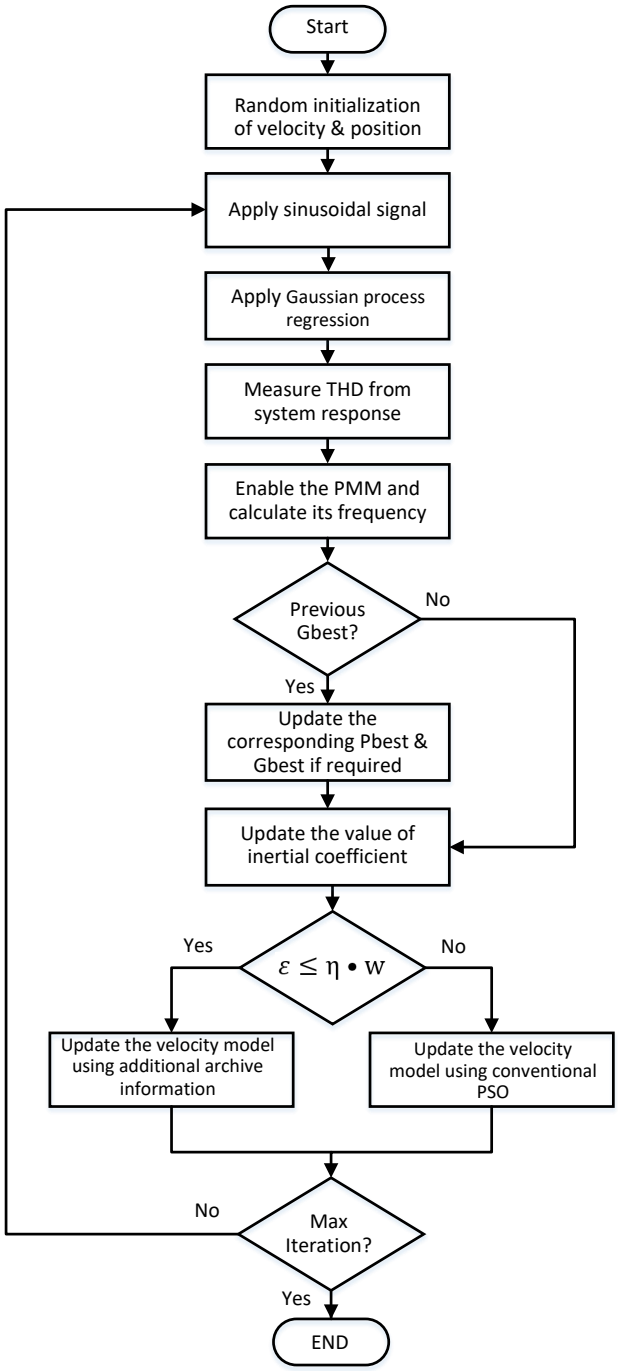

Figure 4.7: Flowchart of the proposed THD-based low-cost robust optimization.

accounting for the periodic component, is employed.

Upon completing this intermediate uncertainty assessment step, the methodology reverts to the conventional ERPSO framework. FFT is executed on the CFIA's output, and THD is calculated. Power consumption is also estimated in parallel, serving as another objective function. These metrics guide subsequent optimization steps executed by the ERPSO algorithm, which continues to balance explorative and exploitative be-

haviours in the search space and iterates until a predefined maximum number of cycles is reached.

By introducing the GPR-based uncertainty estimation block, this adapted flow adds an additional layer of robustness to the methodology. It ensures that the uncertainty associated with the output response of the DUT is accounted for before proceeding to the THD measurement, thereby offering a more comprehensive evaluation of the system's performance and reliability.

4.1.4.2 Archive-Based Robust Optimization

In the work detailed in [113], a block diagram showcasing the methodology of archive-based robust optimization is presented in Figure 4.8. The DUT in this experimental framework is a CFIA, and the ERPSO serves as the optimization algorithm. The archive stores both previously visited positions generated by the optimization algorithm and the output responses from the CFIA. This archived data is later leveraged to reduce the system's uncertainty levels. Following this, a THD-based low-cost performance measurement technique is executed, consistent with previous methodologies.

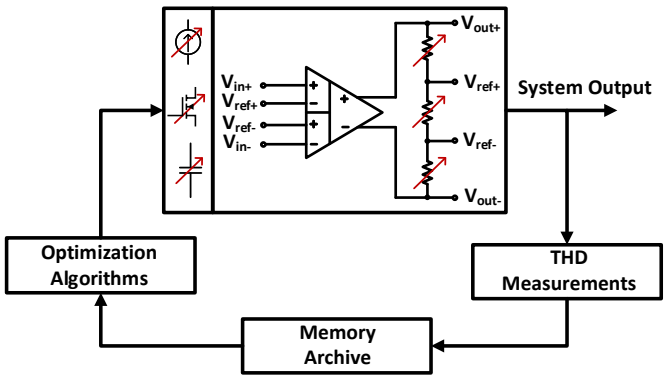

Figure 4.8: Block diagram of proposed robust optimization using archive-based robust optimization.

The flow diagram presented in Figure 4.9 shares many similarities with the proposed GPR-based robust optimizer depicted in Figure 4.7. Both methodologies start with the random initialization of each particle's velocity and position parameters, followed by the application of a sinusoidal input signal to the DUT.

However, the two approaches diverge in how they handle the uncertainty associated with the DUT's output. While the methodology in Figure 4.7 employs Gaussian Process Regression (GPR) for uncertainty estimation, the approach outlined in Figure 4.9 uses

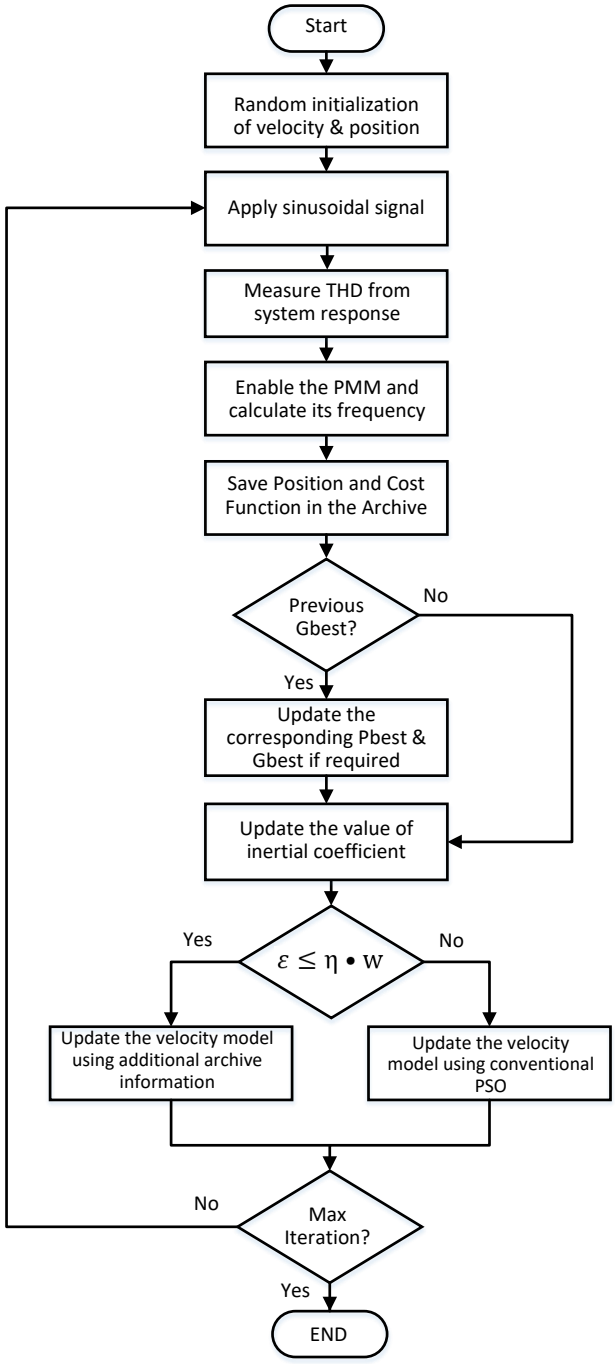

Figure 4.9: Flowchart of the proposed THD-based low-cost robust optimization using archive-based robust optimization.

an archive of previously visited positions by the optimization algorithm. This archive serves to minimize the uncertainty level of the system.

This unique feature is graphically exemplified in Figure 4.10 using the two-dimensional Griewank objective function. As the exploration activities of the searching agents become more focused around the global best position over time, the methodology becomes increasingly adept at minimizing the impact of observer inaccuracies.

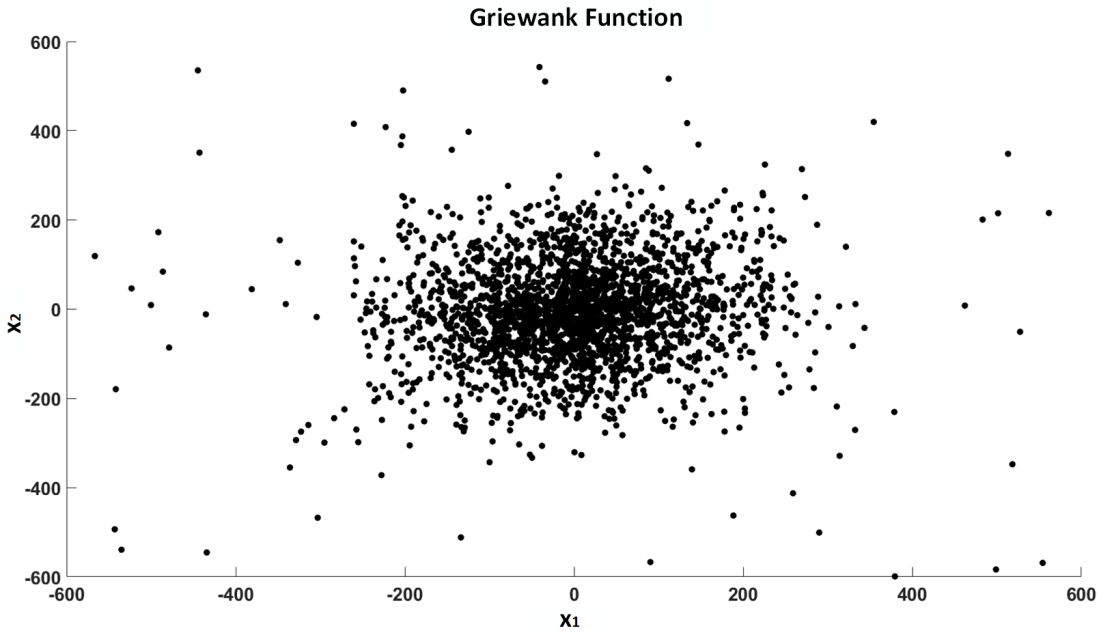

Figure 4.10: Visualization of the exploration capabilities of the PSO after 100 number of iterations.

After addressing the uncertainty, both methodologies revert to the foundational framework of ERPSO. FFT is executed on the CFIA output. Subsequently, THD and power consumption are calculated and used as objective functions to guide further optimization by the ERPSO algorithm. Iteration continues until a predefined maximum number of cycles is reached.

By substituting the GPR-based uncertainty estimation with an archive of previously visited algorithmic positions, the methodology in Figure 4.6 offers an alternative but equally robust way to account for uncertainties in system output, thereby providing an alternative evaluation of the system's performance.

4.2 Indirect Measurement Method based on Non-Intrusive Sensors

The work detailed in [171] presents a block diagram illustrating a methodology for non-intrusive sensor-based low-cost indirect measurement, as shown in Figure 4.11. Non-intrusive sensors are placed on-chip in close proximity to the main DUT, yet they are electrically disconnected from it. This configuration allows the sensors to experience the same PVT variations as the DUT, ensuring a consistent environmental impact on both.

A regression model is commonly employed to correlate the sensor data from the NS with the performance metrics of the DUT, enabling an efficient, indirect estimation of the DUT's operational characteristics [45, 98].

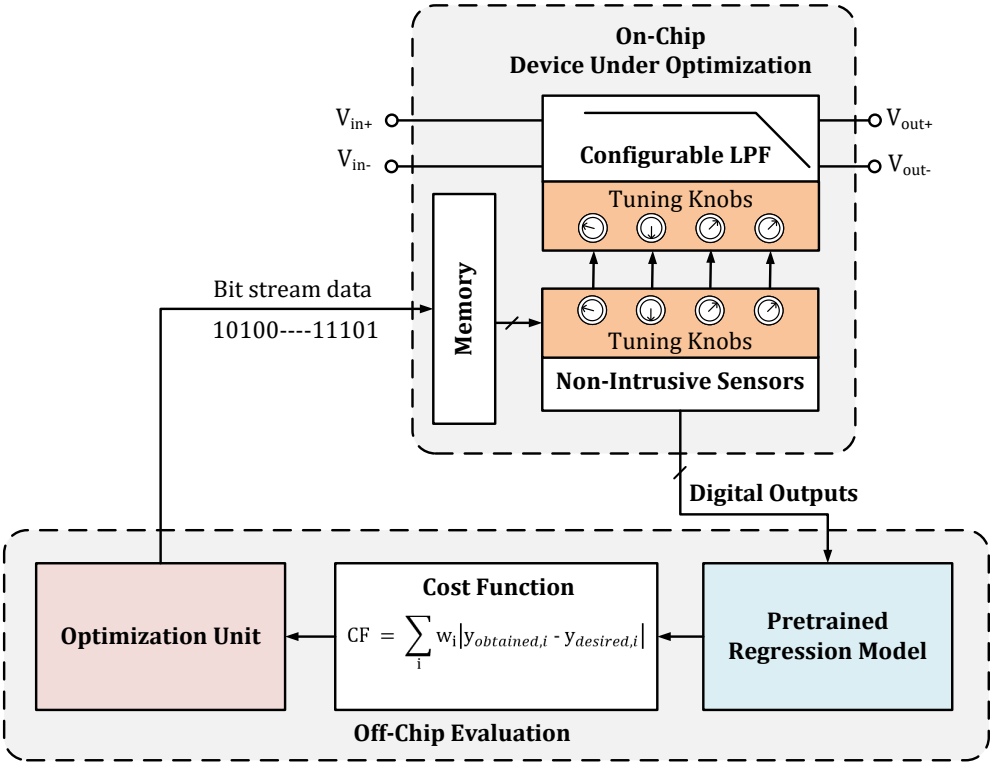

Figure 4.11: Block diagram of the proposed IMs method.

For demonstration, a wide tunable range anti-aliasing filter is used as the DUT. Both the non-intrusive sensors and the DUT operate with similar tuning knob values, thereby reducing the complexity of the search space and simplifying the machine learning task. Once optimization is complete, these fine-tuned tuning knob values are mirrored to the main DUT for performance improvement. The distinctive contribution of this methodology lies in executing the optimization algorithm on the non-intrusive sensors while mirroring the tuning knobs settings of the DUT. This strategy enables the indirect optimization of the DUT's performance without causing any interruption to its ongoing operation. In terms of modeling, a random forest regressor is employed to create a robust regression model. This model associates the non-intrusive sensors output and tuning knob settings with the DUT's performance metrics. The random forest regressor thus facilitates indirect performance prediction based on the non-intrusive sensors's low-cost, quasi-digital output frequency measurements. The complete workflow is illustrated in a flow diagram in Figure 4.12.

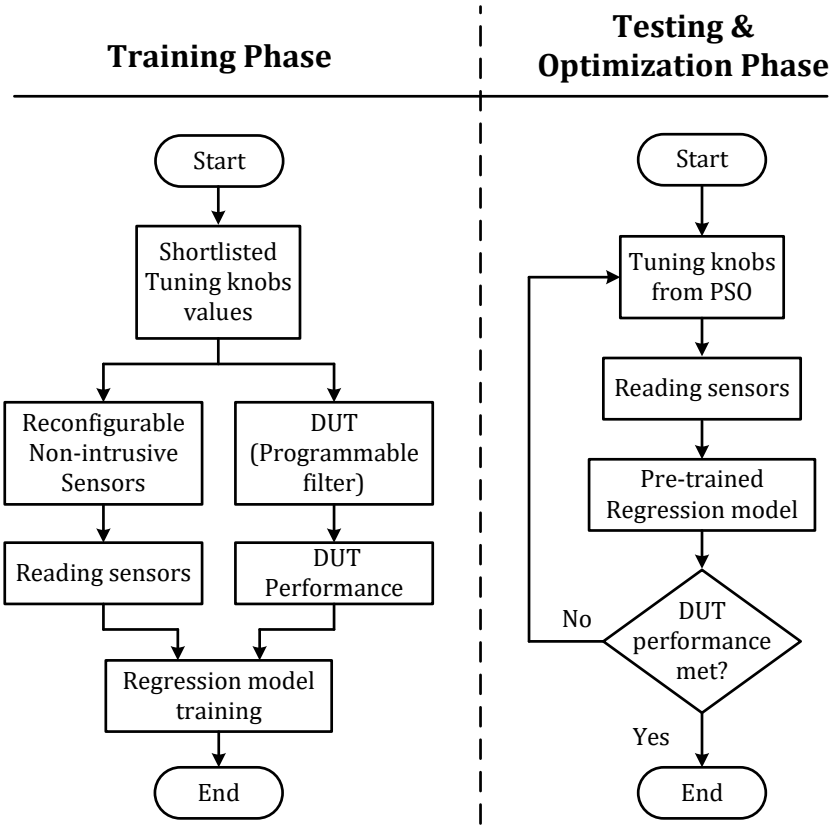

Figure 4.12: Flow chart of the proposed IMs approach.

During the initial stage, a subset of tuning knob values is chosen from the larger optimization search space. This is done to minimize the size of the training dataset as well as to reduce evaluation time. Both the non-intrusive sensors output and the DUT performance are then simulated under identical PVT conditions. From the entire dataset, 80% is randomly allocated for the training of the RFR, while the remaining 20% is used to assess model performance.

The testing and optimization phase starts with the initialization of a PSO, which employs a set of particles to represent potential solutions in the tuning knob value space. The PSO then selects an initial set of tuning knob values to apply to the non-intrusive sensors. The output from the non-intrusive sensors, influenced by these tuning knob values, serves as the input for the pre-trained random forest regressor model. The random forest regressor, in turn, estimates the performance metrics of the DUT based on this input. The PSO uses this indirect performance estimation to adjust the tuning knob values for the next cycle of optimization. Finally, the process evaluates whether the optimization has converged, based on criteria either reaching a predefined maximum

number of cycles or hitting an acceptable error threshold. Once the convergence criteria are met, the optimized tuning knob values are transferred from the non-intrusive sensors to the DUT, completing the optimization cycle.

4.2.1 Anti-Aliasing Filter

A key application of the methodology is its use in optimizing the performance of an anti-aliasing filter. This filter is vital for signal conditioning, specifically for eliminating noise within the Nyquist bandwidth before the signal is converted by the ADC. To accommodate a wide bandwidth range, a novel fully-differential fourth-order, tunable continuous-time active low pass filter was proposed, based on the Sallen-Key structure with Butterworth approximation, as outlined in the work [172]. The quality factor of this filter is set through well-matched capacitor ratios.

To accommodate the extensive tunable bandwidth, modifications were made to the metal-oxide-semiconductor (MOS) floating resistor [173], as well as adjustments to its biasing current, as detailed in the schematic diagram in Figure 4.13. Yet, tuning the filter within this extensive range is a challenging task that traditionally would require costly measurement processes for optimization.

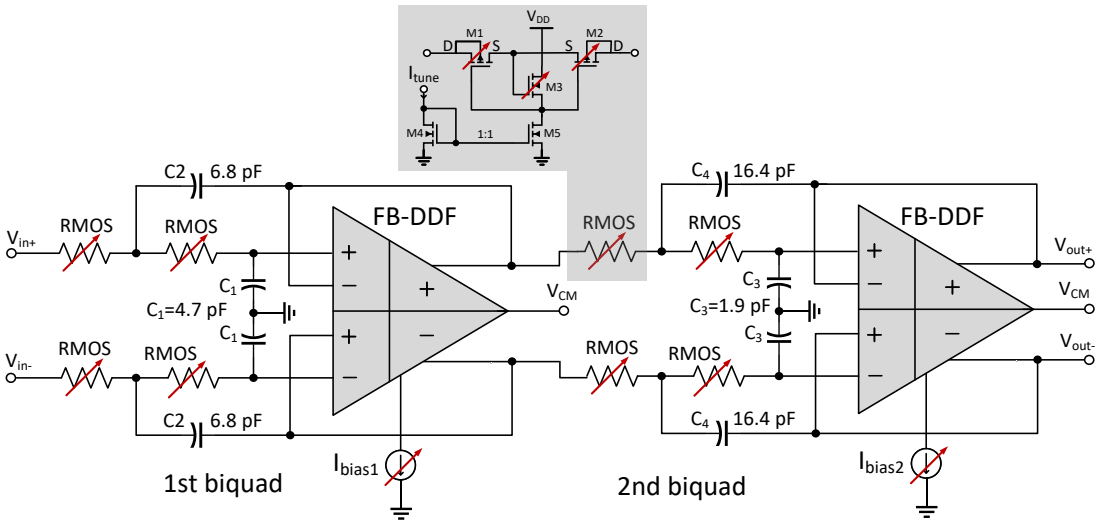

Figure 4.13: Simplified schematic design of the proposed anti-aliasing filter with tunable MOS resistor.

To mitigate this, an indirect measurement principle based on non-intrusive sensors is implemented within the chip. These sensors allow for a more cost-effective optimization process. Additionally, the core amplifier for this filter is designed as a fully differential

difference amplifier, similar to the one used in the design of the CFIA. Adaptations have been made to this amplifier to lower its output resistance to levels compatible with the Sallen-Key topology requirements. Furthermore, its GBW has been extended to meet the frequency requirements of the filter. This multifaceted approach not only enhances the filter's capabilities but also makes the optimization process more economical and efficient.

4.2.2 Non-Intrusive Sensors

In an effort to enhance the accuracy of the regression model, three different non-intrusive sensors are employed [98, 171, 174]. The first non-intrusive sensor is a clock generator based on a ring oscillator (RO) circuit, as depicted in Figure 4.14. This sensor is specifically designed for Process, Voltage, and Temperature (PVT) monitoring. To improve data correlation, the RO shares numerous circuit elements with the Design Under Test (DUT). Initial tests, however, reveal limitations in predictive accuracy, as quantified by the adjusted R-squared value of the regression model. These limitations suggest that while the RO is sensitive to PVT variations, its primary performance characteristics are governed by RC components, which do not provide sufficient correlational data with the DUT for effective regression modeling.

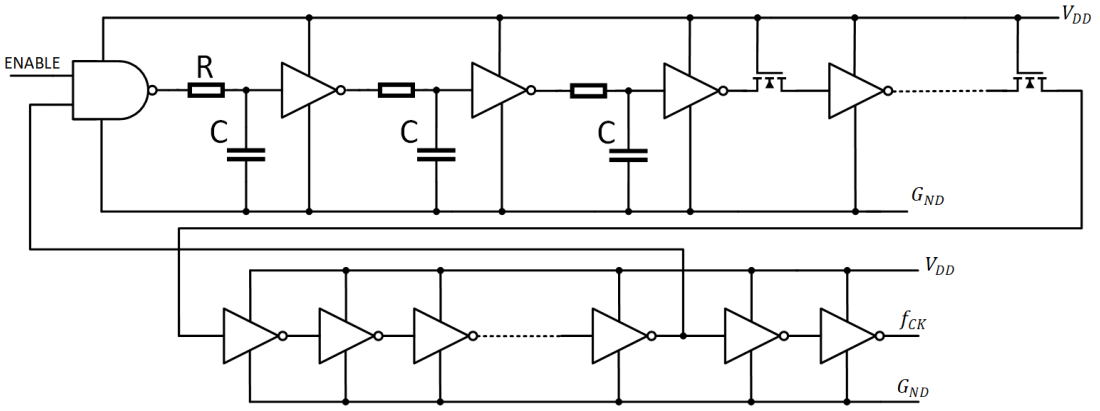

Figure 4.14: Ring oscillator as a low-cost non-intrusive PVT monitoring sensor.

A second non-intrusive sensor is introduced to address this limitation, as presented in Figure 4.15. Unlike traditional circuits that monitor only the threshold voltage (Vth) of PMOS transistors, the modified sensor also captures variations in NMOS transistors. This dual-monitoring approach enhances the model's predictive accuracy by accounting for complementary behaviors between PMOS and NMOS transistors.

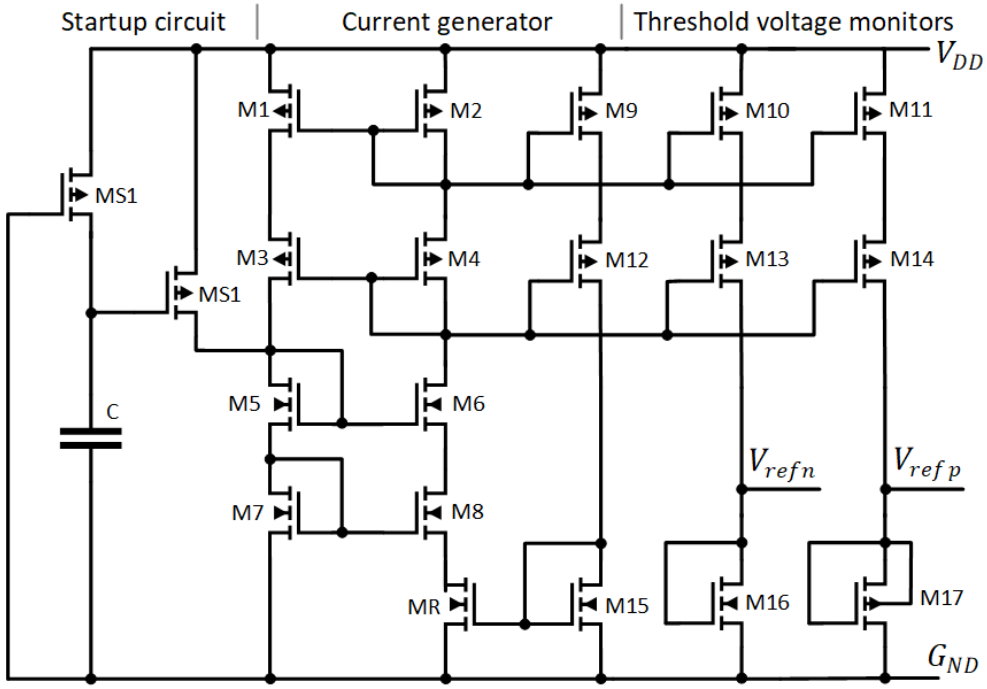

Figure 4.15: Threshold voltage monitor circuit.

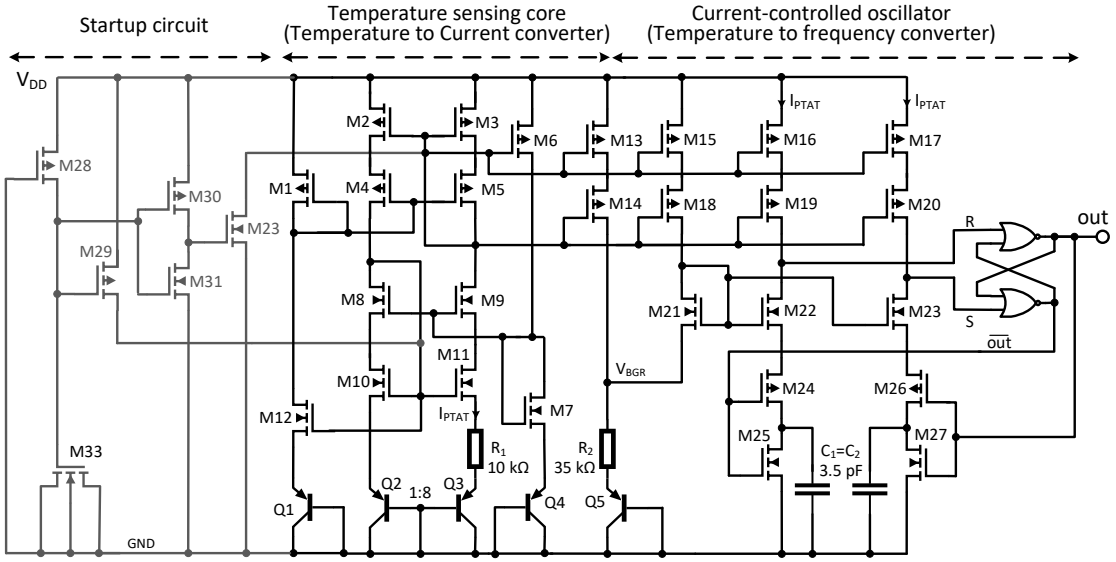

Figure 4.16: The proposed temperature sensor schematic circuit using the XFAB 0.35 μm technology.

The third sensor focuses on temperature variation detection and consists of two main units, as illustrated in Figure 5.45. The first unit is the temperature sensing core (TSC) that converts temperature variations into a current signal. The second unit, the current-controlled oscillator (CCO), then converts this current into a frequency signal. The TSC incorporates a bandgap reference circuit (BGR) to generate a proportional to absolute temperature (PTAT) current and a reference trigger voltage for the comparator in the

CCO stage. The PTAT current is mirrored to the CCO to create a quasi-digital signal that modulates temperature changes in frequency while maintaining a constant duty cycle. To achieve a high power supply rejection ratio (PSRR), the BGR circuit employs wide-swing cascode mirrors, though at the cost of incorporating two additional bipolar junction transistors (BJTs).

Chapter 5

Experimental Setup and Results

This chapter comprehensively explores the experimental setup and the results obtained from two distinct yet interconnected studies: the THD-based power-efficient optimization of the Current Feedback Instrumentation Amplifier (CFIA) and the evaluation of filter optimization using non-intrusive sensors. The experiments are designed to demonstrate the practical application of theoretical concepts in real-world settings, specifically focusing on the adaptability and efficiency of electronic systems in response to dynamic variations. The fabrication and packaging of the chip is carried out through the EUROPRACTICE program. The chip's layout and micrograph are depicted in Figure 5.1a, while Figure 5.1b illustrates the chip layout.

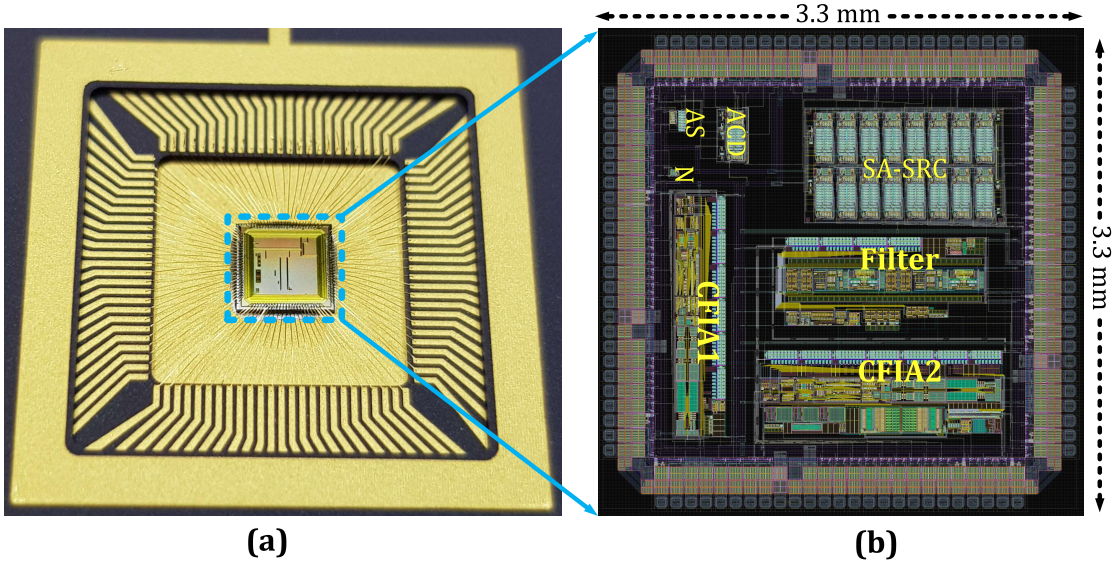

Figure 5.1: MPC USIX chip. (**a**) Chip layout including the pad frame. (**b**) Micrograph photo showing the bonding wires and the sealing ring.

The die is coated with a passivation layer for surface protection, obscuring the die

details. This chip is packaged in a Ceramic Pin Grid Array (CPGA) 100 package and is a multi-project chip (MPC). This MPC comprises various circuits, including amplitude and spike-domain analog front-end circuits with self-X properties (AFEX), forming the foundation of an advanced universal sensor interface called the USIX chip, with the spike-domain circuits being the work of another Ph.D. candidate in our research group [175]. This thesis, however, focuses primarily on the amplitude domain section of the chip, exploring its unique characteristics and capabilities within the broader context of the USIX chip's functionality.

5.1 Evaluation of THD-based Power-Efficient Optimization of CFIA

This section focuses on the experimental setup and comprehensive results of the research, centered on THD-based power-efficient optimization of the CFIA. The exploration revolves around a self-optimizing system's intrinsic implementation and architectural design, leveraging Field-Programmable Gate Array (FPGA) technology. Two Red Pitaya boards are employed to construct a robust framework for in-field performance optimization of the CFIA, utilizing principles of indirect measurement approaches for enhanced accuracy and efficiency.

The experimental procedure is designed to cover various aspects of the CFIA performance, including shadow register verification, testing under default and optimized configurations, and dynamic performance evaluation under varying environmental conditions. The setup is designed to address the challenges of continuous sensory measurement during device optimization.

Furthermore, the section presents a detailed analysis of measurement results, showcasing the impact of different optimization strategies on the CFIA's performance. This involves an examination of the circuit under both static and dynamic conditions, thereby providing a comprehensive understanding of its capabilities and limitations. The results indicate the CFIA's performance and the effectiveness of the employed optimization techniques in enhancing the system's overall efficiency and robustness.

5.1.1 Experimental Setup

5.1.1.1 Intrinsic Implementation and Architecture of the Self-X System

Figure 5.2 illustrates the intrinsic implementation of in-field performance optimization for the CFIA using an indirect measurement approach. This configuration employs two Red Pitaya boards. The first board (FPGA board 1) is dedicated to data acquisition, computing THD using FFT, and transmitting the data to a server. The second board (FPGA board 2) focuses on implementing the ERPSO, managing the serial data-transfer protocol for CFIA configuration, and determining the signal frequency for the power-monitoring module.

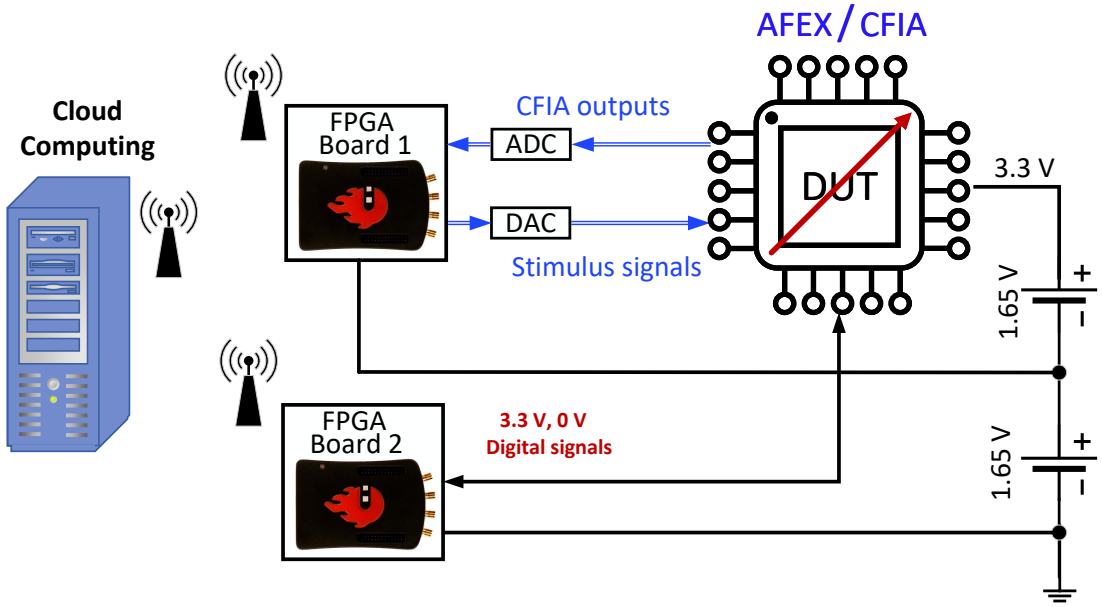

Figure 5.2: Block diagram illustrating the in-field optimization methodology for the reconfigurable CFIA circuit.

Given that the analog outputs of the Red Pitaya board are referenced to 0 V, FPGA board 1 undergoes a DC level shift of 1.65 V to align with the dynamic input range of the CFIA's single-supply operation, which is powered by 3.3 V. Alternative methods to match the dynamic range between FPGA board 1 and the CFIA chip include the use of a transformer balun, such as the Coilcraft PWB2010, or an active DC level shifter using wide-bandwidth, fully-differential amplifier circuits like the LMH6553 from Texas Instruments or the LTC6363 from Analog Devices. However, employing a transformer restricts the experiment to higher frequencies, and the latter solution is avoided to preclude any uncertainties that might arise from adding another analog component in

the prototyping demonstration.

The implementation of the self-X architecture on the CFIA circuit using Red Pitaya boards 1 and 2 is detailed in Figures 5.3 and 5.4. The generation of specific binary files facilitates the configuration of these boards is performed by using the Xilinx Vivado design suite. In this setup, the integrated RF DACs on the Red Pitaya boards are utilized to generate fully-differentiated stimulus signals, essential for evaluating the performance of the CFIA circuit. Concurrently, the RF ADCs on the boards are employed to capture the circuit's output response. Both ADC and DAC are 14-bits. The ERPSO algorithm runs on Red Pitaya board 2, while board 1 measures THD.

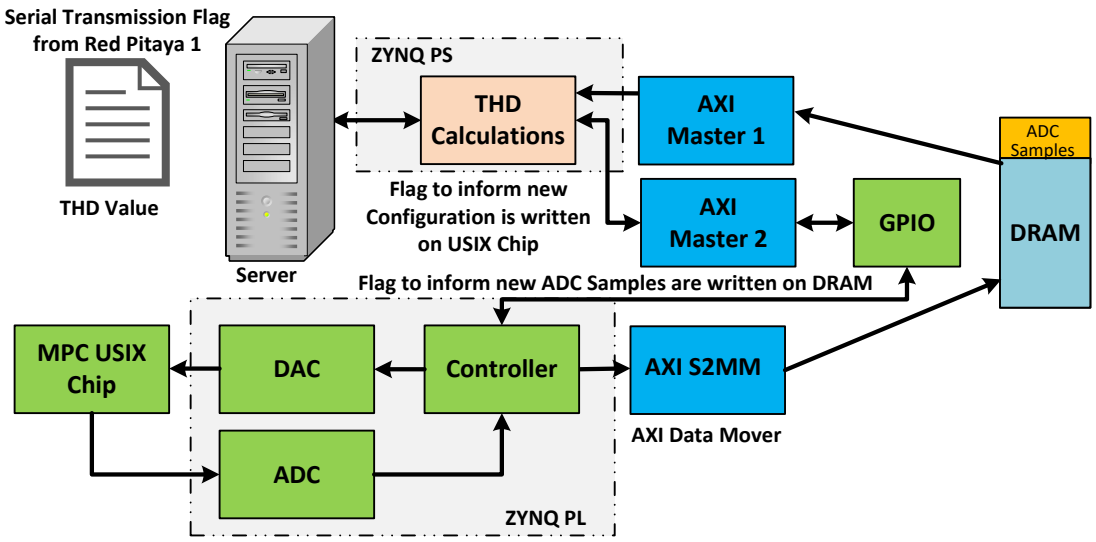

Figure 5.3: Detailed implementation of self-X architecture for Red Pitaya board 1.

5.1.1.2 Workflow of the Optimization Process

Figure 5.5 depicts the optimization process, paralleling the performance optimization framework of Synopsys [31]. This system includes two Red Pitaya boards equipped with ADCs/DACs to optimize THD while minimizing power usage through a multi-objective, agglomerative optimization strategy. Within the CFIA circuit, scalable elements function tuning knobs. The algorithm reconfigures the system by applying a configuration pattern to the CFIA, followed by measuring the CFIA's output response. This iterative cycle is repeated until a pre-established termination condition is fulfilled. A detailed report of the results will be provided upon concluding the optimization process.

The optimization process initiates with the serial transmission of ERPSO particle

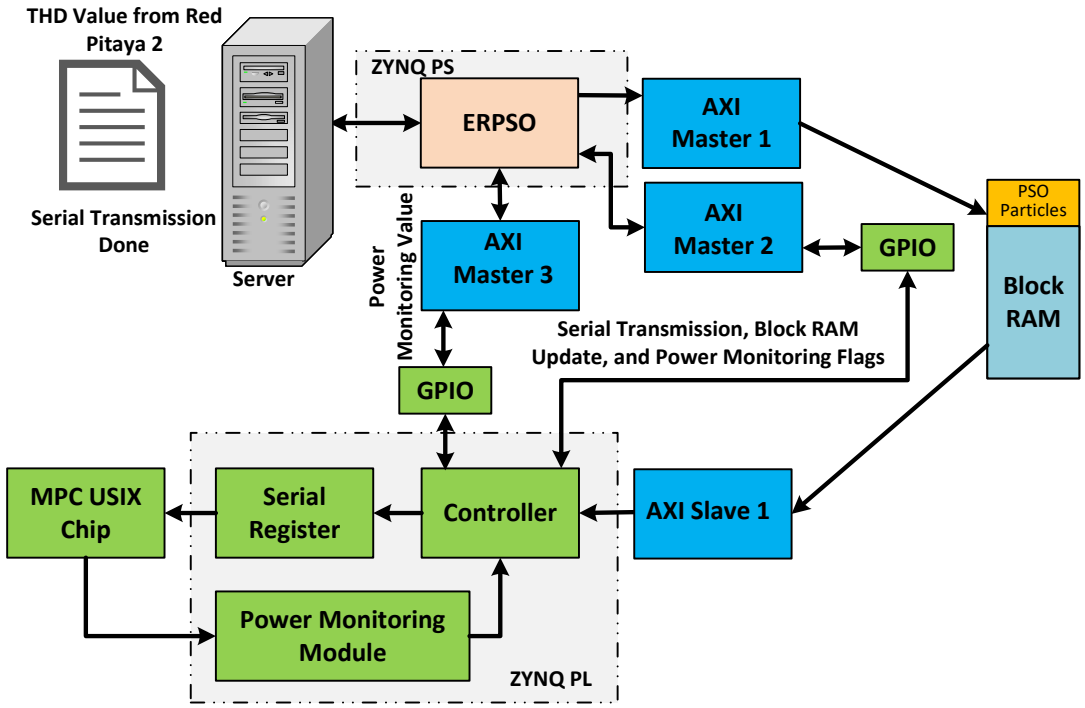

Figure 5.4: Detailed implementation of self-X architecture for Red Pitaya board 2.

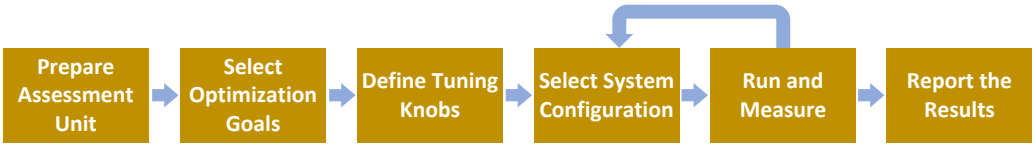

Figure 5.5: Performance optimization workflow for smart sensory electronics.

values to the CFIA's shadow register through Red Pitaya board 2. The CFIA is temporarily powered down during this data transfer to prevent potential transitional states. Once the data is successfully written, the CFIA is reactivated. Subsequently, Red Pitaya board 1, upon server notification, starts the THD calculation for the specific ERPSO particle solution.

Red Pitaya board 1 initiates the THD calculation by applying a fully differential sinusoidal stimulus to the input of the CFIA and then captures the resulting output response using its onboard RF DAC and ADC. These gathered data samples are subsequently stored in the board's shared dynamic random-access memory (DRAM), facilitated by an advanced eXtensible interface (AXI) stream to memory-mapped IP. Once this data transfer is complete, the controller module signals the end of the acquisition process by setting an acknowledgment flag, thereby informing the processing subsystems (PS) of the Red Pitaya board. The THD is then computed using these samples on the PS side

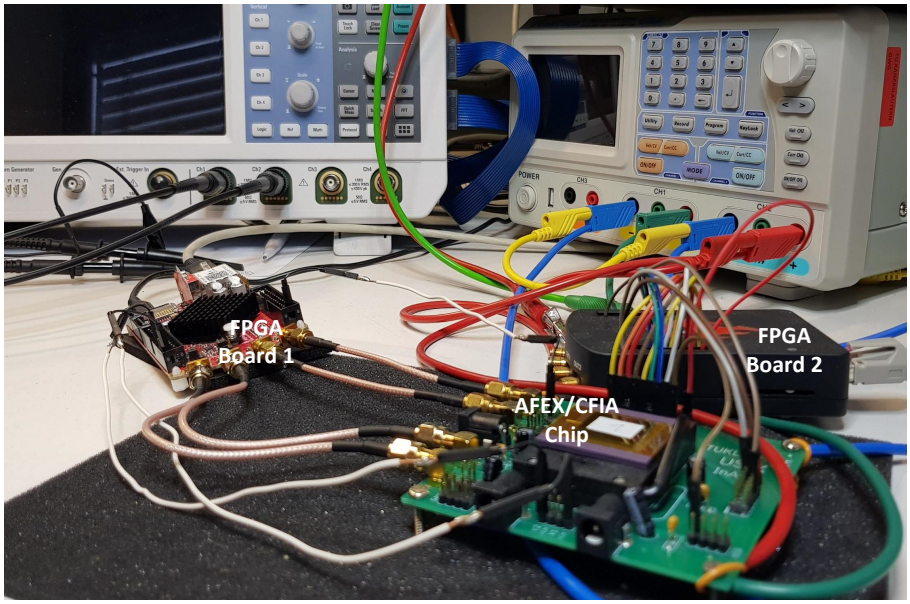

Figure 5.6: Lab setup for the evaluation of the proposed methodology.

of Red Pitaya board 1. This THD value is forwarded to Red Pitaya board 2 via the server for incorporation into the ERPSO algorithm.

In the next phase, the ERPSO activates the power-monitoring module to measure the output frequency from the CFIA's power-monitoring circuit, thereby indirectly assessing the DC power consumption of the current configuration. Notably, during THD calculations, the power-monitoring function is temporarily disabled to prevent any potential disturbances from transient pulse switching that might impact the analog outputs. This optimization process persists until the pre-set maximum number of iterations is reached. Figure 5.6 illustrates the experimental laboratory setup used in this methodology. The prototype, consisting of a four-layer printed circuit board (PCB), was designed using Eagle Autodesk software. Separate power and ground planes have been implemented to improve the system's noise performance, enhanced with decoupling capacitors placed near the chip's power pins for optimal noise reduction.

5.1.2 Measurement Results

5.1.2.1 Shadow Register Verification

The initial verification process is performed by loading the CFIA circuit with a default configuration pattern, as outlined in the post-layout extrinsic evaluation detailed in [36]. This configuration data is serially transmitted from the Red Pitaya to the CFIA's shadow

register at a transfer speed of 1 Kb/s, employing a mode akin to the SPI (serial peripheral interface) protocol mode 0. In this setup, the Red Pitaya acts as the master device, with the CFIA chip serving as the slave. The clock's polarity is maintained at a logical low during idle states. The shadow register is designed to sample data on the clock's rising edge, with data transitions occurring on the falling edge. Control of the shadow register's read and write operations is governed by four specific bits—two for write operations and two for read operations. Furthermore, the most significant bit (MSB) of the register is connected to the "Dout_Debug" pin on the chip, a crucial element for debugging the serial data in the register, as explored in [36]. Figure 5.7 demonstrates this debugging process. Following the completion of write operations across the register's four rows, the data initially written into the first row is successfully read back, confirming the effective transfer of the configuration data.

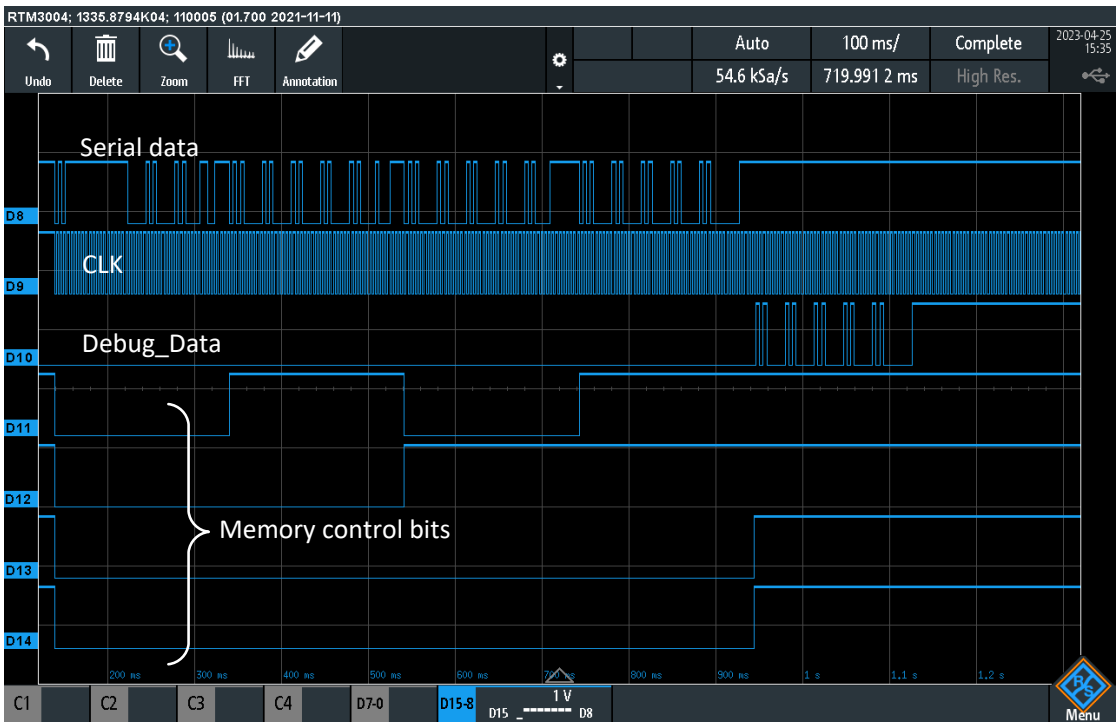

Figure 5.7: Shadow register function verification using the debugging pin.

5.1.2.2 CFIA Testing Using the Default Configuration

The CFIA circuit exhibited satisfactory performance in simulations using the RC extraction netlist and successfully passed PVT (process, voltage, and temperature) validations, including Monte Carlo (MC) and worst-case (WC) simulations. These simulations accounted for an extensive industrial temperature range (from −40 °C to 85 °C) and

considered supply voltage variations of ±10%. Notably, these simulations incorporated a process variation margin of 6 sigma. Despite this, actual measurements indicated a degree of instability in the circuit. This instability could potentially arise from deviations in device characteristics due to the fabrication and packaging processes.

Figure 5.8 presents the MC post-layout simulation conducted to assess the CFIA's phase margin (PM), serving as a measure of unity-gain closed-loop stability under the default configuration. This evaluation was performed using 500 samples and a Gaussian distribution function to mirror real process variations. The simulation included both process and mismatch variations across the entire CFIA circuit. The Figure shows that the CFIA maintained a stable PM even at extreme conditions, demonstrating a 100% yield for a targeted PM of over 45 degrees. Each differential output pair was connected to a 15 pF capacitive load and a 10 kΩ resistive load during these tests. Notably, in its default configuration, the CFIA uses only the two least significant bits of the configurable compensation capacitor and operates with reduced power in the output stage. This configuration leaves room for further PM enhancement, though based on simulation results, such an enhancement is not considered essential.

Figure 5.9 displays the observed practical behavior at the outputs when both inputs are connected to the common-mode DC voltage (VCM) of 1.65 V. The input capacitance of the mixed-signal storage oscilloscope (MSO) used, from Rohde & Schwarz, is 14 pF in the X10 channels with a 10 MΩ impedance, which aligns with the load capabilities of the CFIA.

On the other hand, the output signals of the CFIA provide crucial insights. They indicate that a symmetrically balanced layout leads to even and in-phase outputs, thereby achieving a high common-to-differential-mode rejection ratio. This is evident as the differential output signal (Vout_diff) displays a noticeably reduced oscillation amplitude. The inherent capability of the fully differential circuit to mitigate common signal noise is a significant advantage [176]. Nevertheless, the presence of oscillatory behavior at the output suggests that the CFIA struggles with linear response to the input signal.

Figure 5.10 highlights this issue by portraying the DC output characteristics of the CFIA when its inputs undergo a linear sweep from 0 to 3.3 V at unity gain, with a step size of 33 mV. These observed behaviors are then compared with the outcomes of the post-layout simulation for comparison. Additionally, Figure 5.11 presents the transient

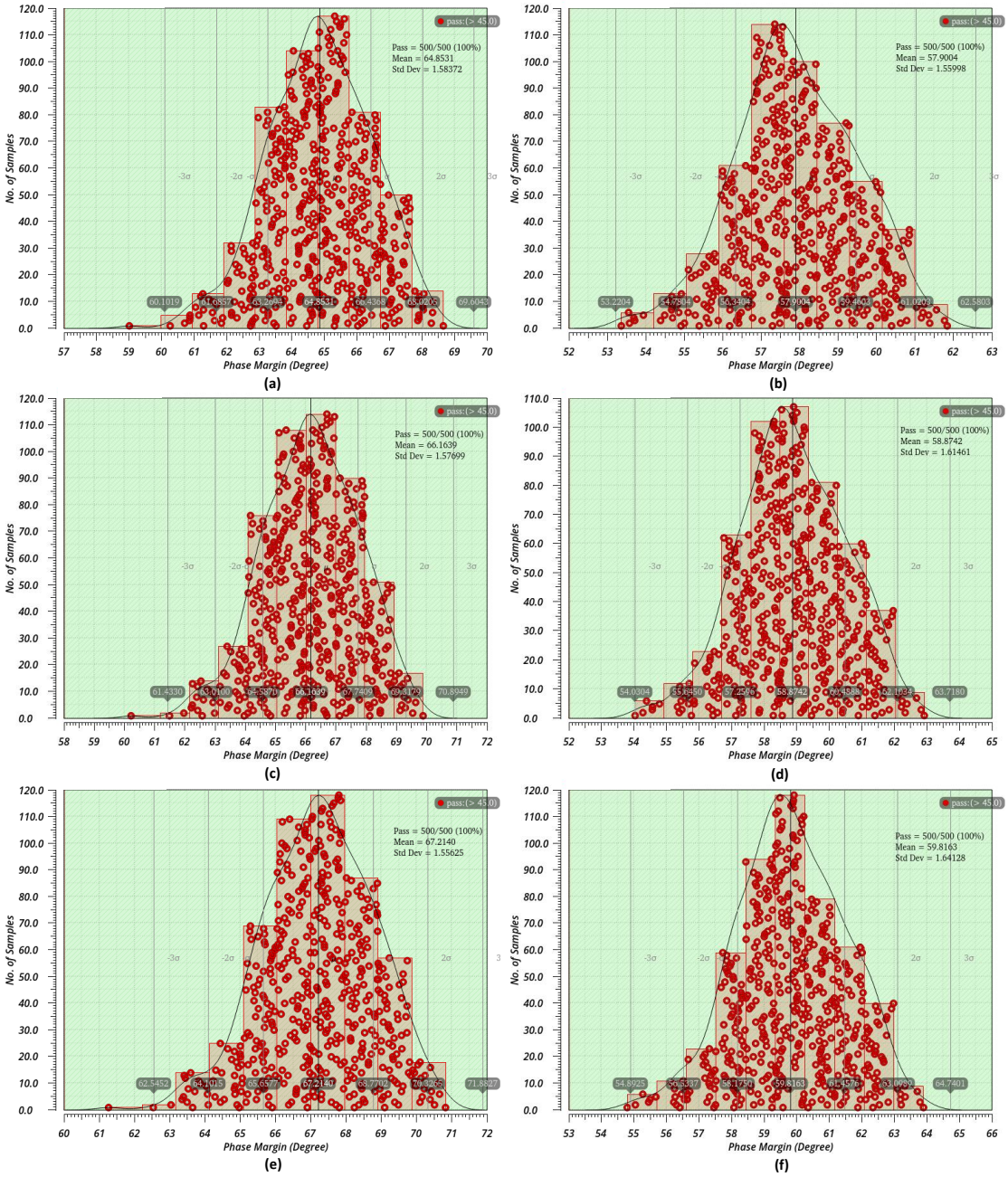

Figure 5.8: MC simulations on the post-layout CFIA netlist with RC exctraction type and using of 500 sample per corner: (a) $V_{DD} = 3.0\ V\ and\ T = -40\ °C$, (b) $V_{DD} = 3.0\ V\ and\ T = -85\ °C$, (c) $V_{DD} = 3.3\ V\ and\ T = -40\ °C$, (d) $V_{DD} = 3.3\ V\ and\ T = 85\ °C$, (e) $V_{DD} = 3.6\ V\ and\ T = -40\ °C$, (f) $V_{DD} = 3.6\ V\ and\ T = 85\ °C$.

response of the output to a fully differential sinusoidal input signal, characterized by a 1 Vp-p amplitude and a frequency of 1 MHz, thereby revealing the degree of distortion in the time domain. Furthermore, Figure 5.12 exhibits the differential output signal in the frequency domain obtained through the execution of the FFT. The nonlinearity at the output introduces harmonic distortion within the signal's frequency spectrum, which is directly related to the CFIA's nonlinearity. As a result, there is a direct correlation be-

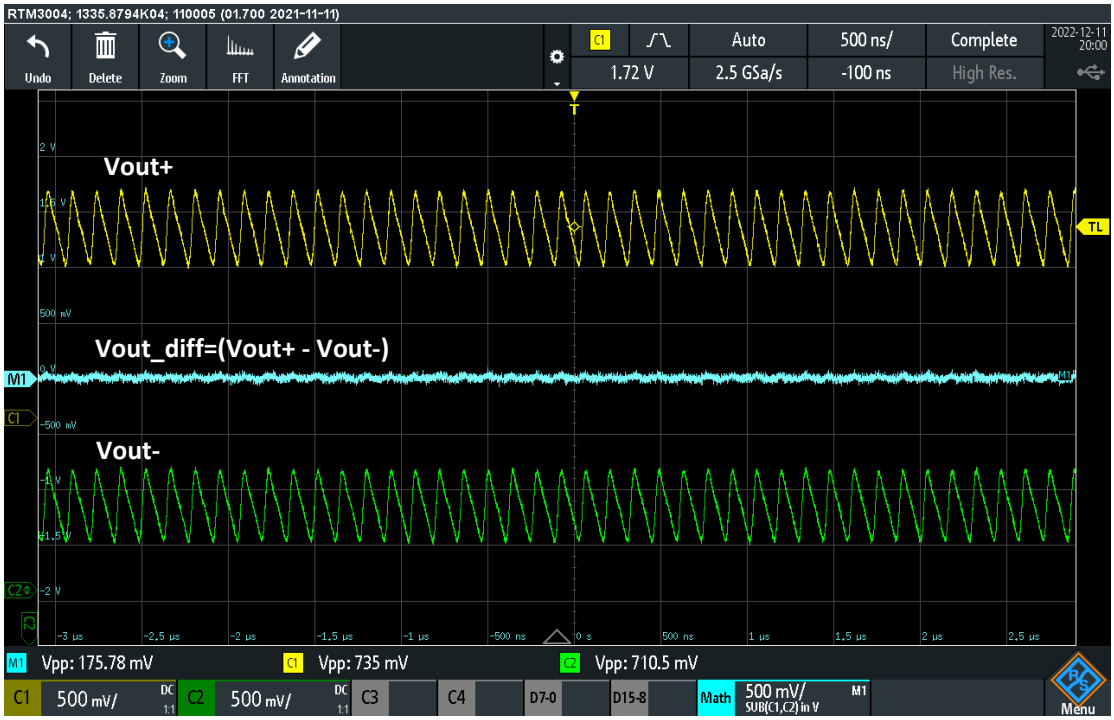

Figure 5.9: Unstable condition of the CFIA under default pattern configuration.

tween the nonlinearity of the CFIA and the observed Total Harmonic Distortion (THD) value. Specifically, a THD value of -30 dB signifies a considerable degree of nonlinearity in this case.

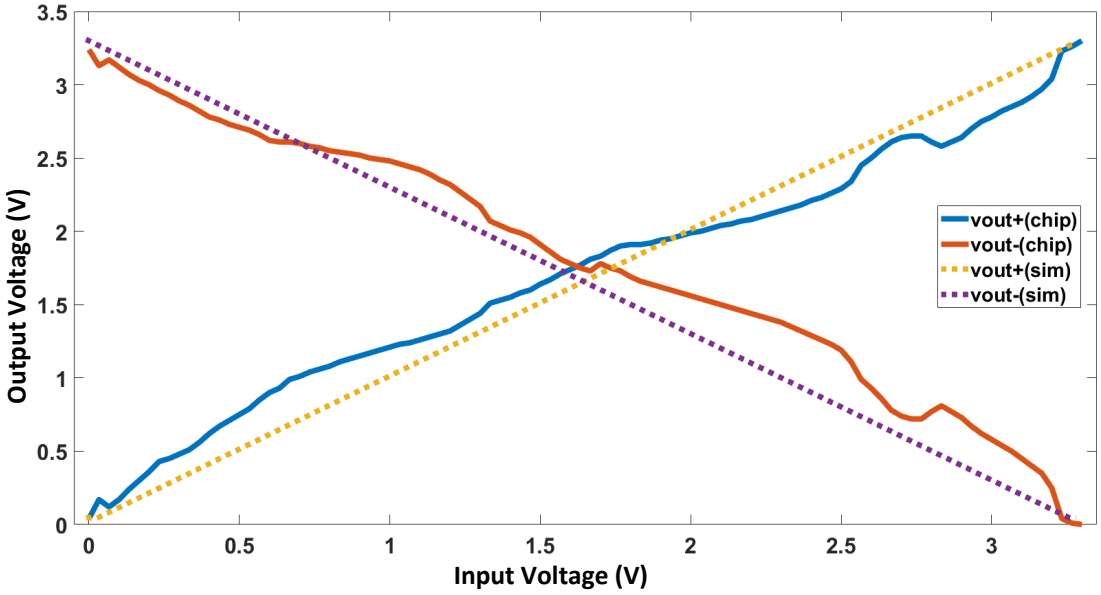

Figure 5.10: Output DC characteristics of the non-stable CFIA with unity gain configuration as compared to the post-layout simulation.

The experimental procedure outlined was initially carried out on a selection of 15 chips, which were part of a larger batch of 32 chips received from the foundry. These

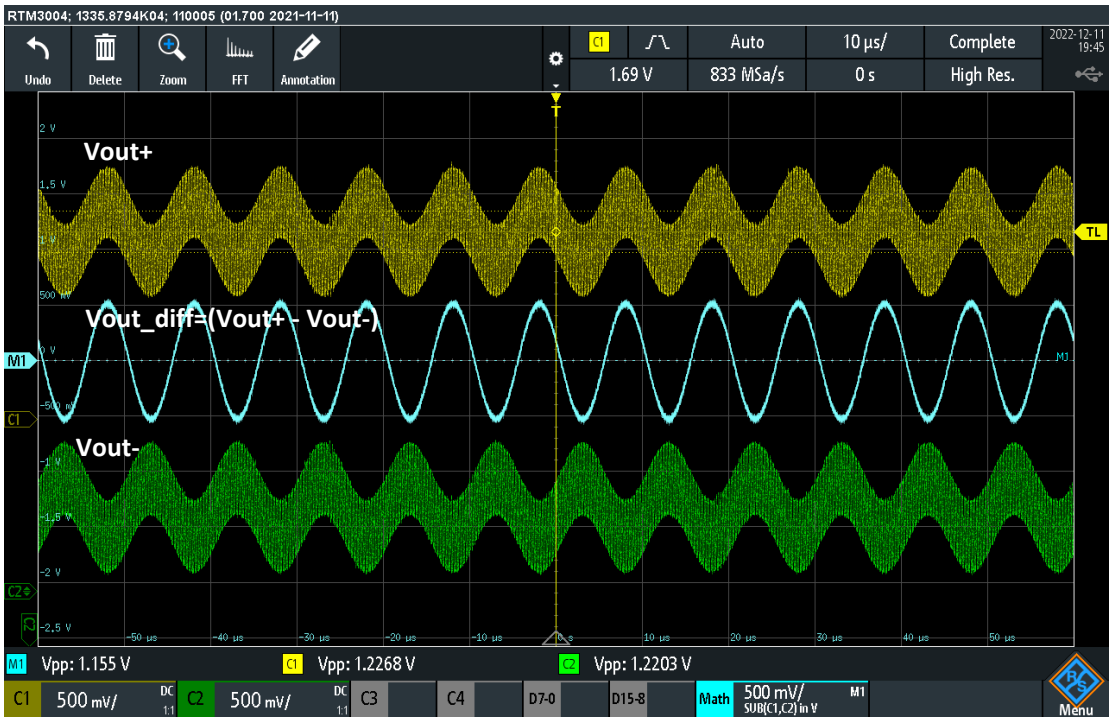

Figure 5.11: Output transient response to the fully-differential sinusoidal signal under non-stable condition.

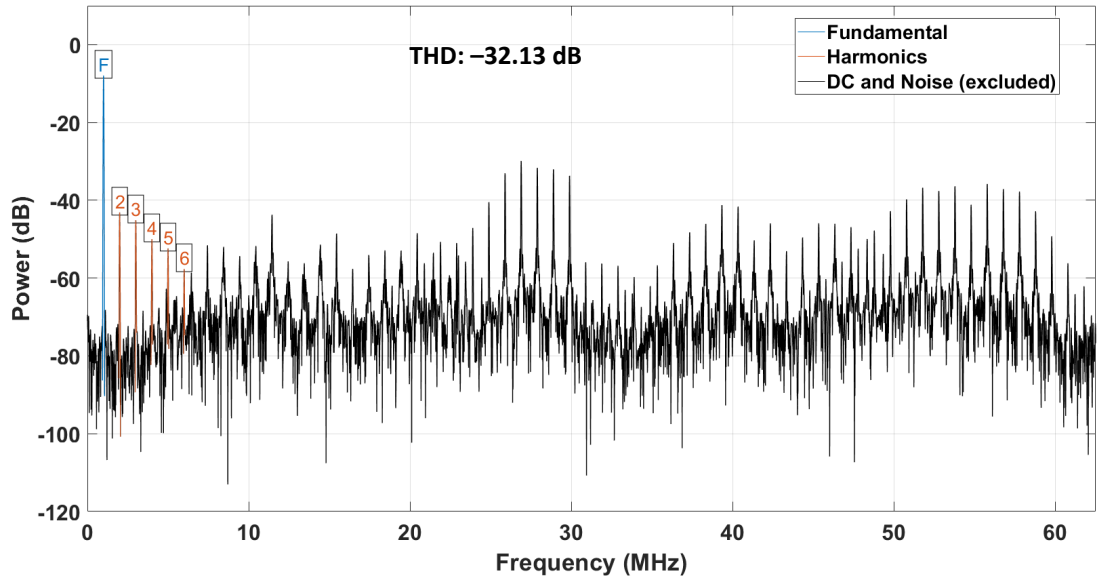

Figure 5.12: FFT output of the CFIA under non-stable condition.

chips were sequentially numbered, and for this experiment, chips numbered 1 and 3 – 16 were chosen for testing. All tested chips exhibited similar characteristics, likely due to their origin from the same wafer during fabrication. This uniformity implies that the entire batch would be discarded if the circuit were designed with fixed-size elements. This situation underscores the critical importance of having configurable circuits with

self-X properties, which offer adaptability in addressing such challenges. To explore this further, the subsequent experiment involved subjecting the chip to in-field optimization using the ERPSO algorithm. The aim was to identify the optimal configuration pattern to bring the CFIA into its best operational region.

5.1.2.3 PMM Characterization

Before the optimization, the power monitoring circuit was assessed by altering the CFIA's biasing current by configuring the current DAC. Subsequently, the corresponding output-pulse frequency of the module was monitored. The PMM circuit, functioning as a current-to-frequency converter, generates a quasi-digital signal characterized by a 50% duty cycle, as illustrated in Figure 5.13. The CFIA current was measured using the current meter of the power supply unit (PeakTech 6181), which provides a resolution of 1 milliampere. A Frequency-to-Digital Converter (FTD) was designed on the Red Pitaya to read the signal frequency from the PMM and convert it into a decimal value, as presented in Table 5.1 with specific parameters. When the initial rising edge of the output signal from the PMM circuit is detected, the FTD module commences counting until the subsequent rising edge is identified. Hence, the counter value represents the respective frequency. The FTD counter operates at a frequency of 125 MHz, synchronized with the Red Pitaya system clock. Since the maximum frequency of the PMM has been established to be less than 10 MHz, it can be concluded that the resolution provided by the FTD is sufficient for this specific measurement.

In Figure 5.14, it can be observed that the power monitoring scheme demonstrates satisfactory linearity. This characteristic proves advantageous for the optimization algorithm as it provides essential CFIA power data. This, in turn, facilitates the identification and selection of the most efficient solution within the search space. It is worth noting that the resolution of the current measurement influences the linearity graph.

5.1.2.4 CFIA Performance Optimization Using the THD-based Optimization Method

The experiment involved generating a fully differential sinusoidal signal with a 1 Vp-p amplitude and a 1 MHz frequency, utilizing the Digital Signal Synthesizer (DSS) of the Red Pitaya 1, part of the Xilinx Vivado IP blocks suite. This signal served as the primary

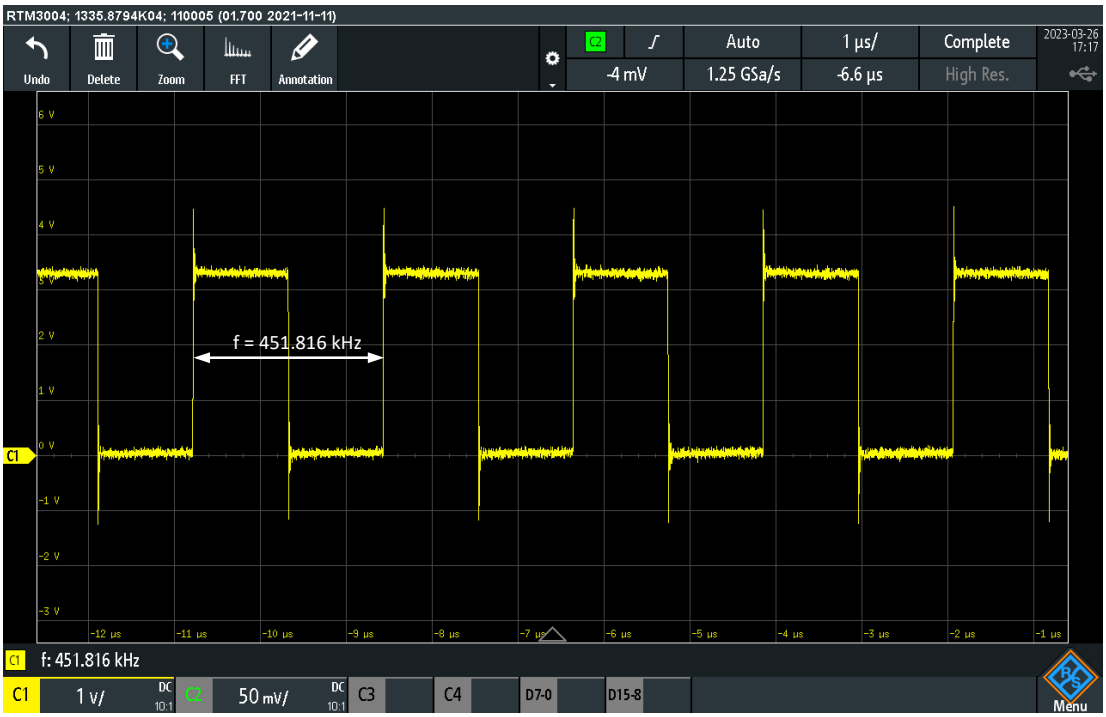

Figure 5.13: Output signal of the integrated power monitoring module.

Table 5.1: Recorded values of frequency-to-decimal conversion of the power monitoring module.

Config Nr.	Clock Frequency	Decimal Equivalent	CFIA Current
1	325 kHz	24,561	1 mA
2	520 kHz	15,372	2 mA
3	701 kHz	11,401	3 mA
4	875 kHz	9162	4 mA
5	1.05 MHz	7233	5 mA
6	1.21 MHz	6618	6 mA
7	1.42 MHz	5627	7 mA
8	1.57 MHz	4725	8 mA
9	1.71 MHz	4566	9 mA
10	1.82 MHz	4404	10 mA
11	4.45 MHz	1626	24 mA
12	4.53 MHz	1595	25 mA
13	4.86 MHz	1489	27 mA

test stimulus in the performance enhancement process of the CFIA. The Red Pitaya's ADC performed the signal acquisition at a 125 MHz sampling frequency, facilitating THD analysis via FFT. The optimization algorithm was implemented with 15 particles across 200 iterations. In the multi-objective optimization framework, significant emphasis was placed on THD value (80% weight) compared to power monitoring (20% weight). To ensure the reliability of the optimization outcomes and mitigate the effects of random

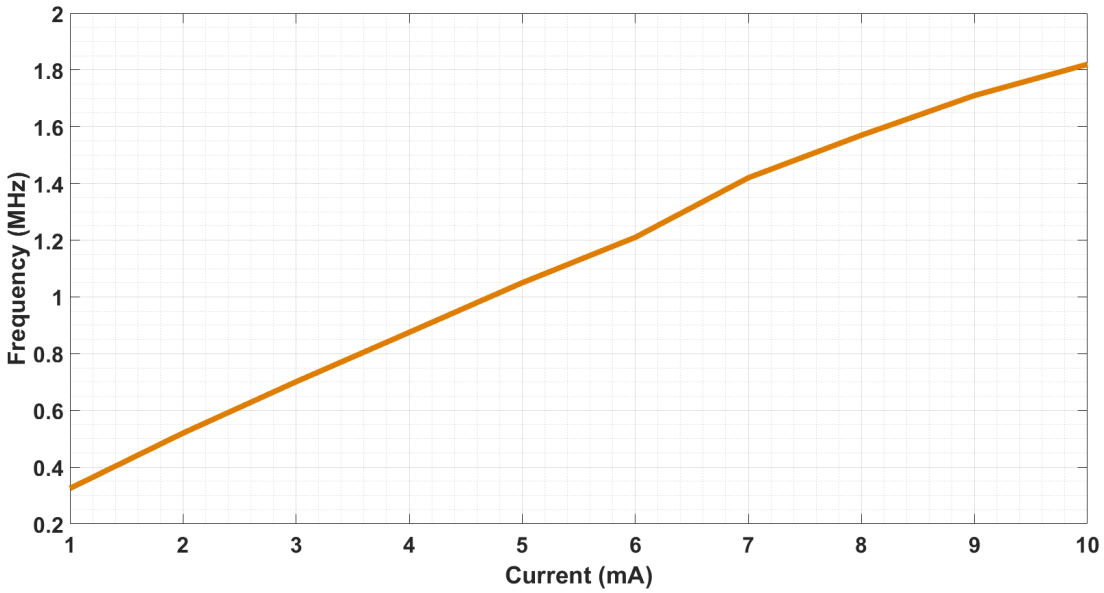

Figure 5.14: Linearity performance of the power monitoring module showing the relationship between the frequency and the CFIA current.

variability, the experiment was replicated across 10 separate runs on the designated chip labeled as number 1. Additionally, Figure 5.15 depicts the average error convergence trend observed in the optimization algorithm. The CFIA was configured to operate at unity gain for worst-case stability conditions.

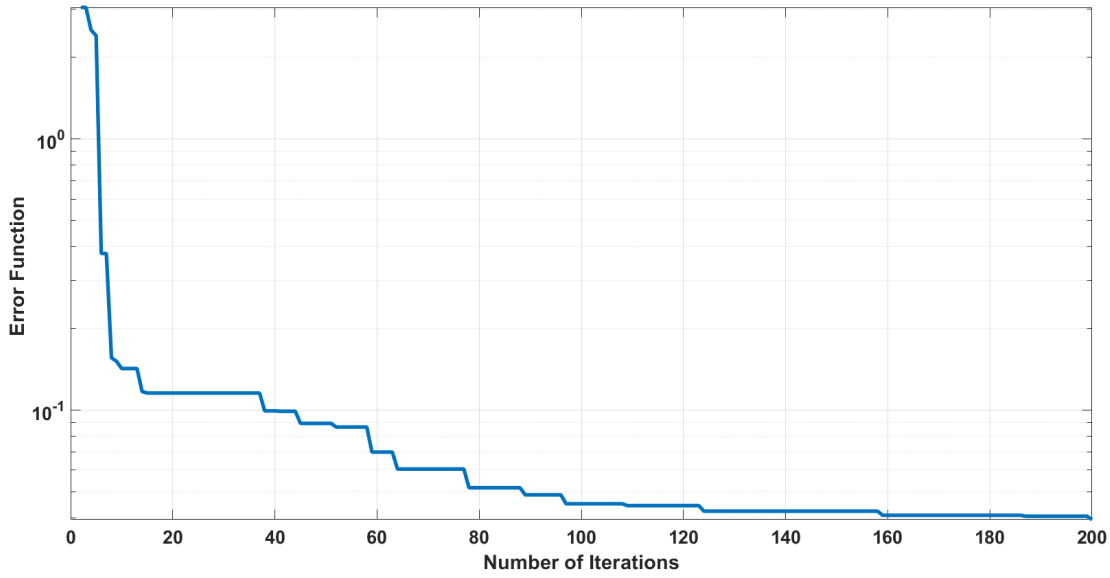

Figure 5.15: Mean value of the error convergence curve of the CFIA optimization.

The THD value of the test stimuli is first calculated with no chip in the loop, where the DAC output of the Red Pitaya is directly connected to its ADC input. Figure 5.16 displays the frequency spectrum of the input test stimuli in this configuration. For

comparison, the chip is then included in the loop, with the DAC output of the Red Pitaya fed into the chip and the chip output connected to the ADC of the Red Pitaya. Figure 5.17 shows the FFT graph indicating the CFIA output frequency response for a solution found by the algorithm with the chip in the loop.

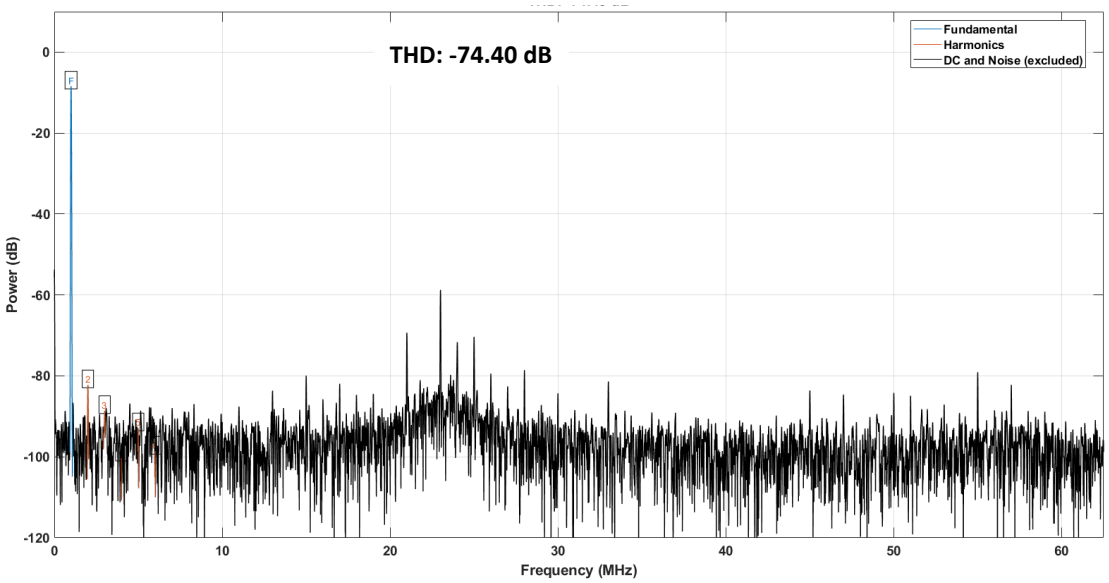

Figure 5.16: FFT output of the test stimuli used for optimizing the CFIA, with the DAC output of the Red Pitaya directly connected to its ADC input.

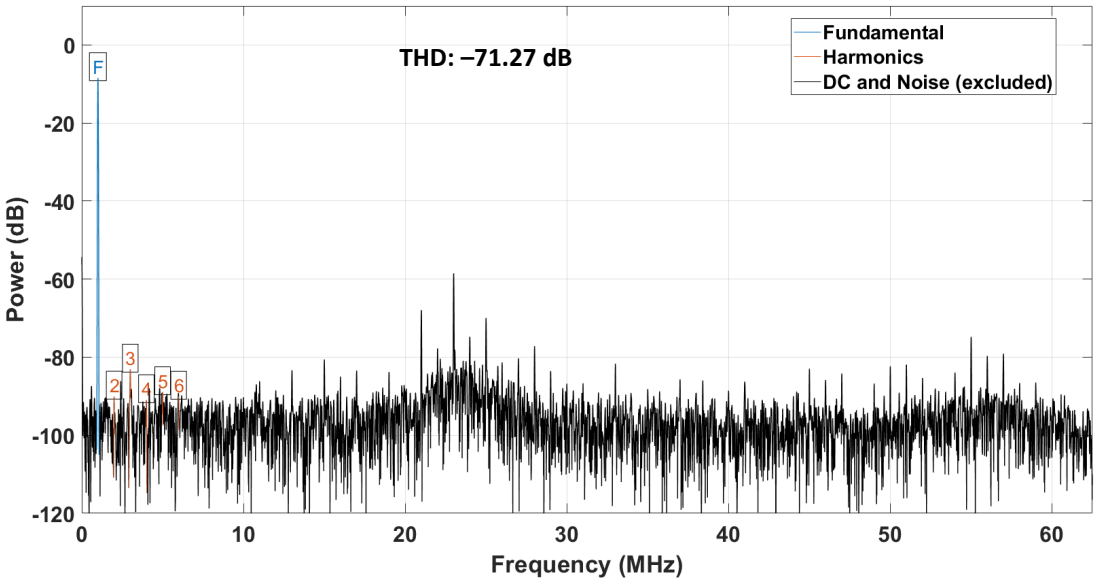

Figure 5.17: FFT output of the stable CFIA solution found by the optimization, with the DAC output of the Red Pitaya fed into the chip and the chip output connected to the ADC of the Red Pitaya.

Following the optimization cycle, the achieved average obtained THD value is -72 dB, with an associated power consumption of 55 mW. This is graphically depicted via the

error bar graph in Figure 5.18 (a), which summarizes the results from 10 separate runs. Additionally, Figure 5.18 (b) provides a detailed view of the optimization performance metrics, focusing on a single optimization cycle conducted on 15 individual chips. The findings indicate that the CFIA has been optimized to its fullest within the limits of the test signal used. Consequently, it is theorized that an enhancement in the THD value of the test stimuli would likely lead to a corresponding improvement in the CFIA's THD performance.

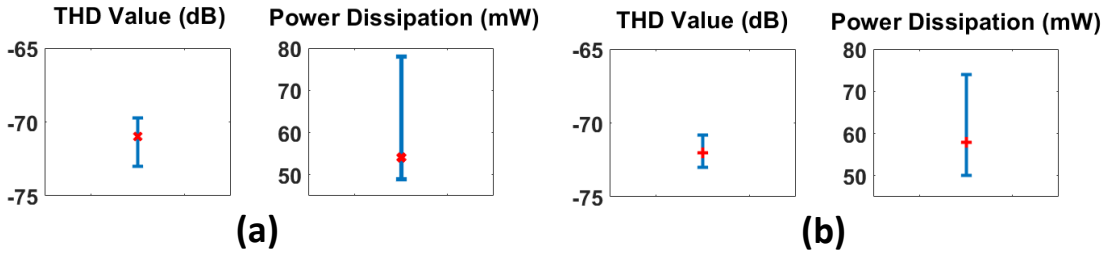

Figure 5.18: Box plots of the ERPSO algorithm (a) over 10 independent runs on a single chip. (b) single run for 15 independent chips.

Figure 5.19 showcases the sinusoidal output response, which indicates an absence of oscillation in the signal. The measured slew rate, derived from impulse response analysis, is approximately ± 11 V/µs. A step response test was performed to further assess the system's stability. The results, illustrated in Figure 5.20, reveal that both the rising and falling edges of the response have a phase margin exceeding 60 degrees. Additionally, Figure 5.21 presents the DC characteristics, highlighting the dynamic input range at unity gain. This broad differential range is particularly beneficial for interfacing with high-output differential sensors like tunnel magnetoresistance (TMR). The AC performance of the system under various gain settings is detailed in Figure 5.22. Notably, the gain observed in the graph was found to be 6 dB lower than expected. The observed disparity in the gain, as shown in the Bode plot (Figure 5.22), does not present a significant concern and can be attributed to the specific setup used for the measurement. This setup involved acquiring a single-ended output during the Bode plot analysis.

The CFIA circuit, incorporating a class-AB complementary output stage, demonstrates an output common-mode range closely approaching the supply rails, as shown in Figure 5.23. This test used a small sinusoidal signal with a 250 mVp-p amplitude and 1 kHz frequency, while the CFIA gain was set at 16. It is important to recognize that the limitation observed in the output signal is primarily due to the characteristics of the

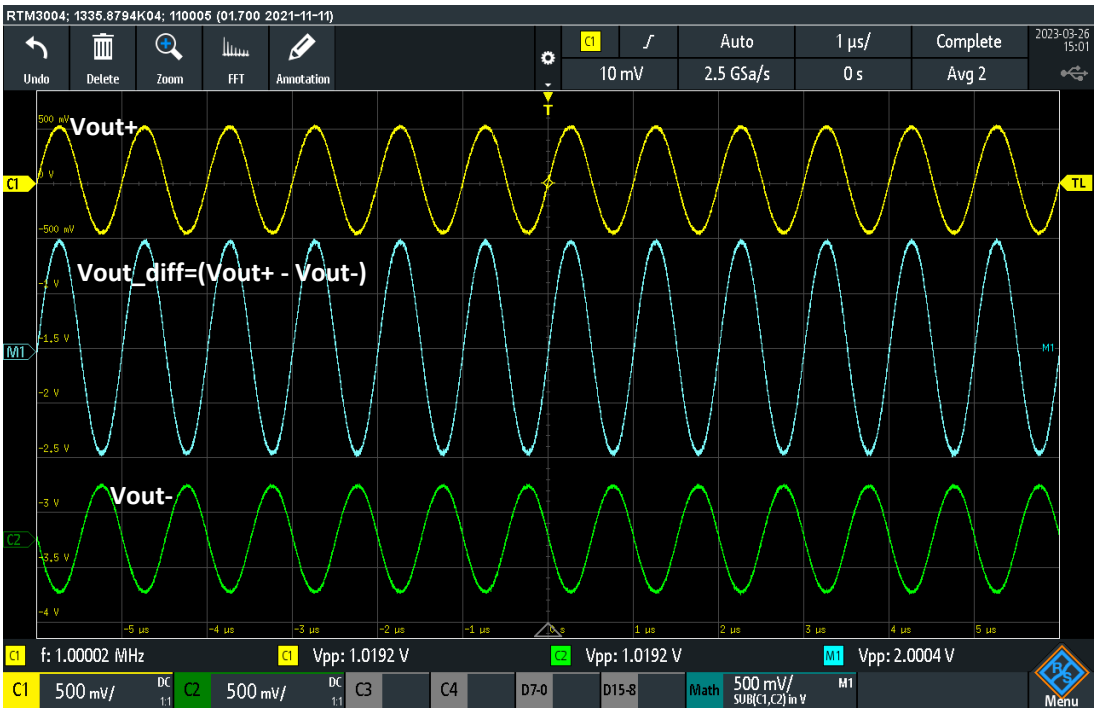

Figure 5.19: Large signal sinusoidal output response of the CFIA after the optimization.

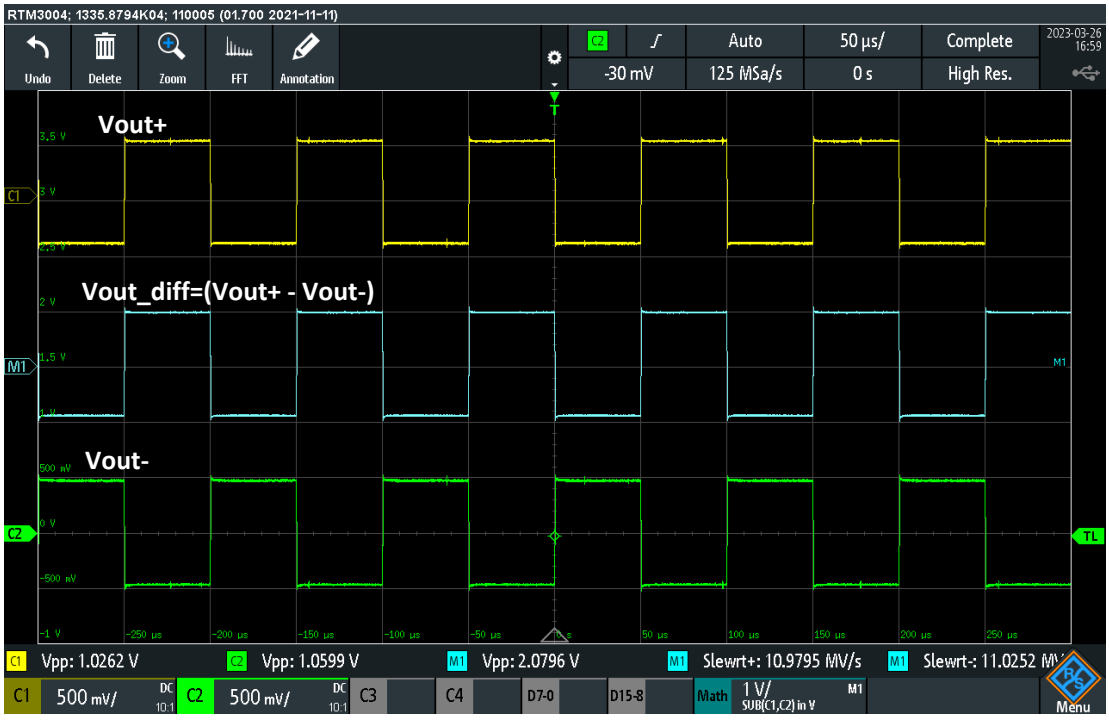

Figure 5.20: Large signal step response of the CFIA after the optimization.

output stage rather than the input features of the system.

Incorporating a class AB complementary output stage, the CFIA circuit features an output common mode range that approaches the supply rails, as depicted in Figure 5.23. During this test, a small sinusoidal signal with an amplitude of 250 mVp-p and a

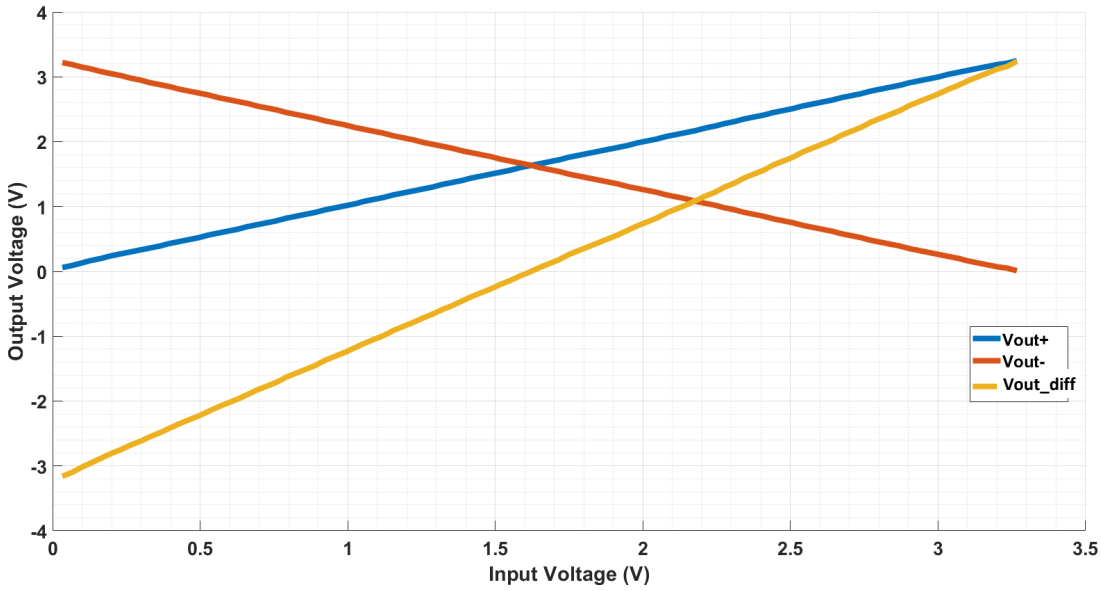

Figure 5.21: Output DC characteristics of the stable CFIA with unity gain configuration after the optimization.

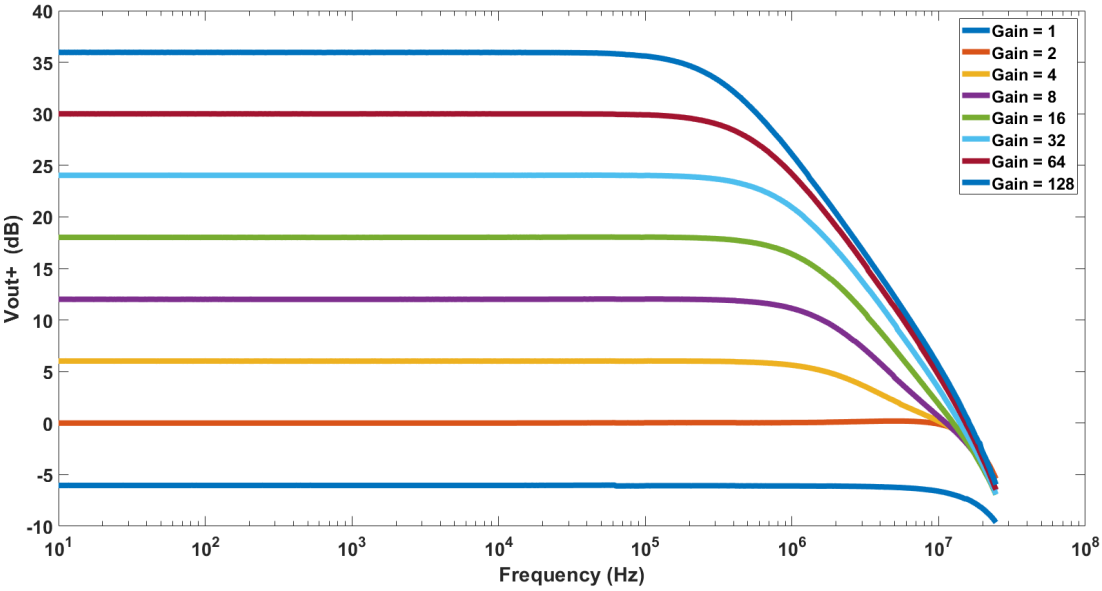

Figure 5.22: Small signal AC response of the optimized CFIA with different gain setting.

frequency of 1 kHz was utilized, while the CFIA gain was established at 16. It should be noted that the output signal constraint is attributable to the output stage rather than the input characteristics.

Table 5.2 offers a comparative analysis of CFIA performance between intrinsic and extrinsic evolution. The intrinsic differential DC gain is indirectly predicted from the closed-loop gain error, given that isolating the feedback network from the amplifier core is impractical. Notably, the table reveals discrepancies between extrinsic and intrinsic

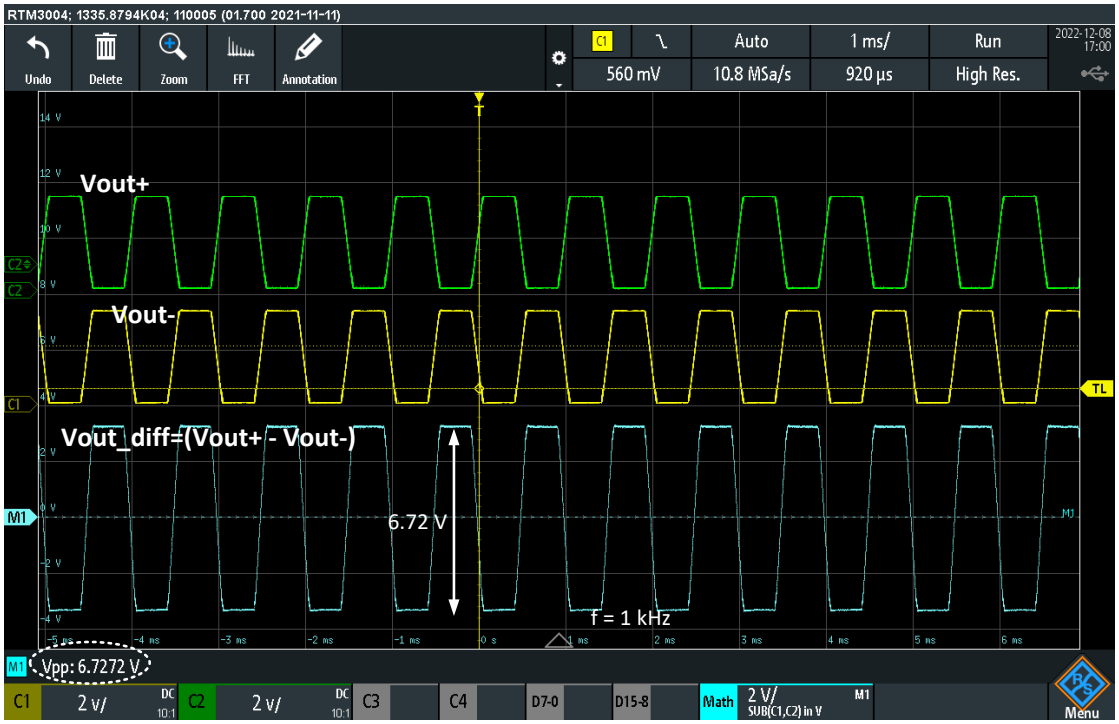

Figure 5.23: The output dynamic range of the CFIA showing the rail-to-rail properties of the class AB output stage.

results attributed to post-manufacturing shifts. One potential cause for this could be the inductive effects of bonding wires and package leads, potentially inducing oscillatory conditions in the CFIA, especially considering this is the first prototype chip developed using XFAB technology.

The fourth column in Table 5.2 displays the CFIA's performance using the default extrinsic optimization configuration. Due to the inherent instability and oscillatory behavior under this configuration, precise characterization of its performance is infeasible. However, the proposed optimization approach effectively identified an optimal configuration, resulting in satisfactory CFIA performance.

The divergence between the simulated and measured power can be attributed to the variation in configuration patterns. This variation arises as the algorithm seeks a stable solution by adjusting the first non-dominant pole of the CFIA driver stage. Specifically, it aims to move this non-dominant pole away from the unity gain frequency point, a process that involves employing higher currents. The CFIA's output stage is designed using fixed-size transistors. Consequently, adjusting their associated poles necessitates increased transconductance (g_m), achievable only by applying a higher current. Additionally, the algorithm tries to enhance the value of the compensation capacitor. This

Table 5.2: CFIA characteristics based on extrinsic and intrinsic optimization solutions for chips 1, 3, 4, 5, 6, 7, 8, 9, 10, and 11 ($V_{DD} = 3.3\,V$, $V_{CM} = 1.65\,V$, $T_{simulation} = 27\,^{\circ}C$, $T_{measurement} = 22\,^{\circ}C$).

CFIA Design Parameter	**Schematic Level**	**Post-Layout Level**	**Chip Level Before Optimization**	**Chip Level Mean of 10**
Differential DC gain (A_{VD})	94.80 dB	94.73 dB	N/A	> 80 dB
Gain–bandwidth product (GBW)	47.75 MHz	39.41 MHz	N/A	> 10 MHz*
Phase margin (PM)	73.22°	60.47°	< 0°	> 60°
Slew rate (SR)	±63.38 V/μs	±60.34 V/μs	N/A	±11 V/μs
PMM output frequency (f_{ck})	347.18 kHz	377.48 kHz	700 kHz	3.1 MHz
Static power dissipation (P_D)	4.17 mW	4.16 mW	9.9 mW	53 mW
Input Dynamic Range	Rail-to-rail	Rail-to-rail	N/A	Rail-to-rail
Output Dynamic Range	Rail-to-rail	Rail-to-rail	N/A	Rail-to-rail

* The Bode plot capability of the utilized MSO (Rohde & Schwarz 3004) is limited to 10 MHz due to its signal generator; therefore, the CFIA's gain bandwidth is expected to be higher.

increase contributes to the observed decrease in the measured slew rate. The compensation capacitor's value varies between 0.35 pF and 2.35 pF, with incremental adjustments of 0.25 pF. In the context of the extrinsic evaluation, the average capacitor value recorded is 0.850 pF, in contrast to the intrinsic evaluation, which yields an average value of 2 pF. It is important to mention that this research aims to develop a combined software and hardware framework for reconfigurable electronics. This framework is designed to facilitate the restoration of degraded circuits while ensuring minimal cost associated with measurement equipment to assess the system performance.

The optimization procedure is conducted again without implementing a power monitoring strategy. As a result, the mean power consumption of the CFIA was measured at 80 mW to achieve the same Total Harmonic Distortion (THD) value of -72 dB. This experiment demonstrates that integrating power monitoring into the optimization process increased power efficiency by 34%. Such an improvement is particularly beneficial for applications where power availability is constrained, like sensor nodes powered by battery or energy harvesting. Additionally, reducing current consumption enhances efficiency and extends the device's lifespan by avoiding limitations related to current density in chip interconnections. High current levels can lead to interconnection failure due to

electromigration.

Table 5.3: Extrinsic evaluation of the intrinsically optimized configuration showing the deviation between the simulated and fabricated chip number 1 under the same measurement conditions ($V_{DD} = 3.3\ V$, $V_{CM} = 1.65\ V$, $T = 22\ °C$).

CFIA Design Parameter	**Intrinsic Evaluation**	**Extrinsic Evaluation**
Differential DC gain (A_{VD})	> 80 dB	100 dB
Gain–bandwidth product (GBW)	> 10 MHz	39.5 MHz
Phase margin (PM)	$> 60°$	82°
Slew rate (SR)	± 10.4 V/μs	± 71 V/μs
PMM output frequency (f_{ck})	2.98 MHz	5.72 MHz
Static power dissipation (P_D)	49 mW	79.2 mW
Input Dynamic Range	Rail-to-rail	Rail-to-rail
Output Dynamic Range	Rail-to-rail	Rail-to-rail

A configuration derived from the intrinsic optimization was applied in the extrinsic evaluation phase to assess further the difference between designed and manufactured chips. This approach revealed a clear difference in performance, particularly in power consumption. The specific configuration consumed 15 mA in the intrinsic evaluation and 24 mA in the extrinsic assessment. Table 5.3 details the CFIA's performance with this configuration, allowing for direct comparison with the data in Table 5.2. Notably, the extrinsic evaluation for this measurement was carried out at the typical mean corner of the process module, which inherently differs from the actual fabrication conditions. A Monte Carlo simulation around this solution provides a better comparison. Despite this, the deviation remained outside the intrinsic performance range, as evidenced in Figure 5.24, where power dissipation is recorded.

5.1.2.5 Strategies for Continuous Sensory Measurement During Device Optimization

It is important to acknowledge that during the optimization of the device, there is an interruption in the sensory measurement process. Two strategies can be employed to address this challenge and ensure continuous measurement.

The first strategy involves the deployment of a real-time operating system (RTOS) or a time-triggered embedded system (TTES) on the Red Pitaya board. This is particularly suitable for managing low-frequency sensor signals, such as those from a TMR sensor used to monitor a rotating shaft's speed. The integration of RTOS or TTES enables the simultaneous execution of calibration and measurement processes, effectively interleaving

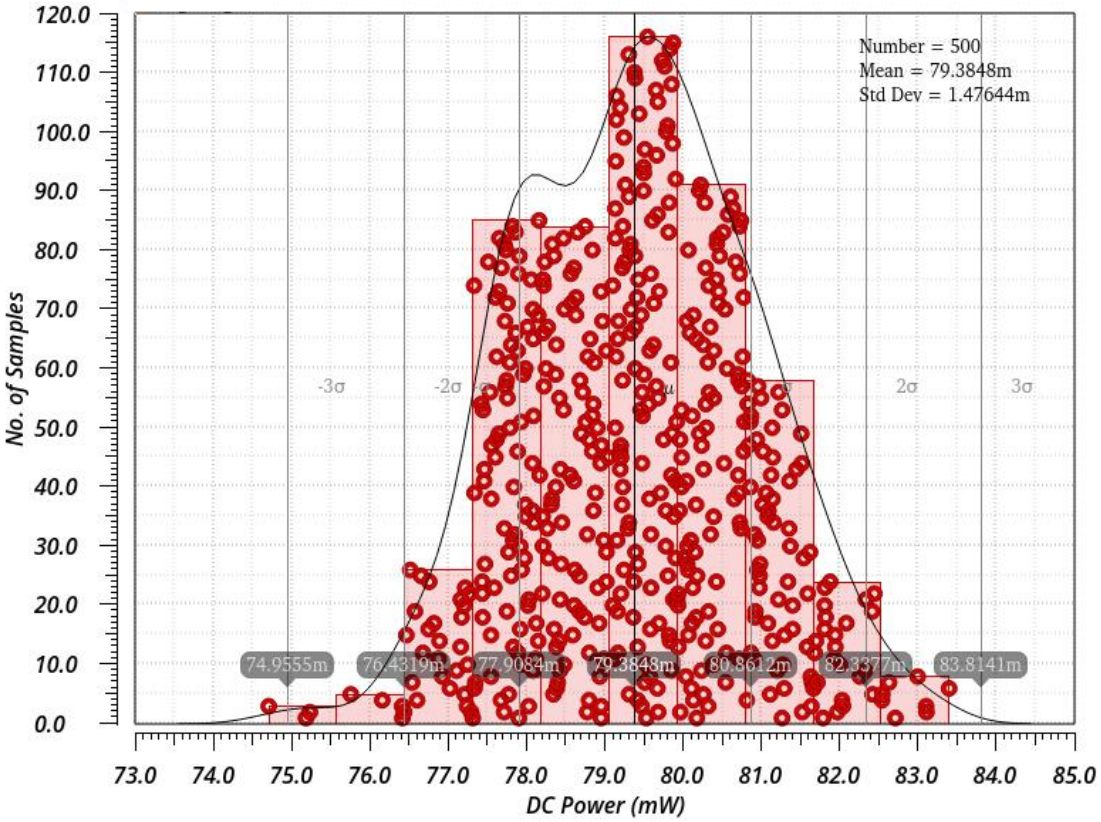

Figure 5.24: MC simulation around the optimization configuration imported from the intrinsic evaluation.

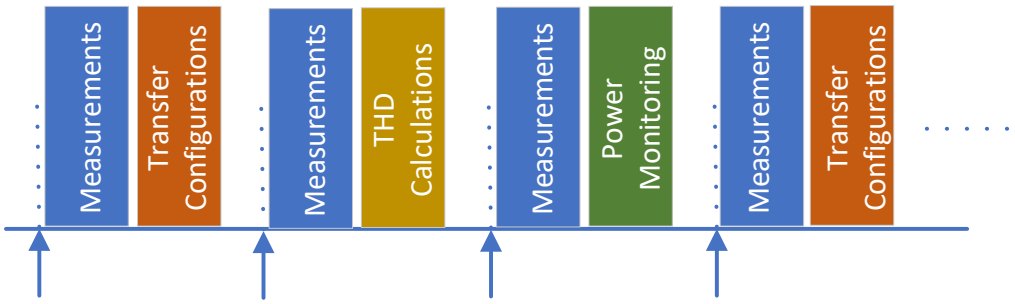

Figure 5.25: Interleaving of optimization and measurement.

them to minimize disruptions. As illustrated in Figure 5.25, this interleaving process includes phases such as 'Measurements', 'Transfer Configurations', 'THD Calculations', and 'Power Monitoring', demonstrating how the system manages to concurrently perform measurement and optimization tasks.

The second strategy is more applicable to high-frequency sensor signals. This approach, known as the ping-pong strategy, operates on the principle of alternating operations between two CFIAs. While one CFIA is being optimized, the other remains active

and fully functional. This dual-system setup ensures that there is always one operational CFIA, thereby facilitating uninterrupted high-frequency signal measurements.

5.1.3 Assessment of CFIA Dynamic Performance Optimization

For the dynamic in-field optimization of self-X sensory electronics, the optimization process is performed by taking into account the varying environmental factors, specifically temperature fluctuations and supply voltage variations [177]. Figure 5.26 depicts the LAB demonstration setup. The Binder MK53 climate chamber is employed for temperature modulation, while the PeakTeck 6181 programmable power supply is utilized for varying the supply voltage. The FPGA boards are situated within the chamber, acknowledging the uncertainty inherent to the optimization system, specifically regarding the test stimuli and ADC as an observer device.

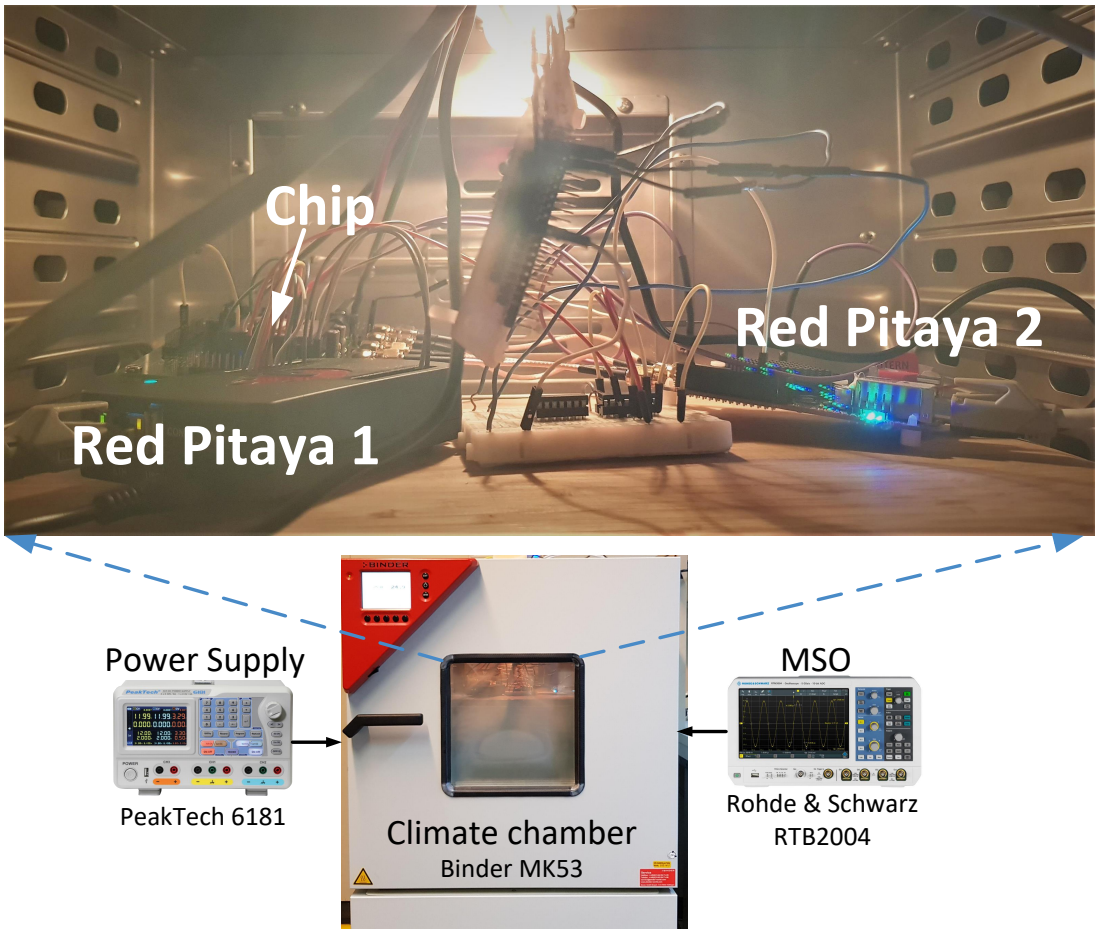

Figure 5.26: The dynamic optimization setup using Binder climate chamber.

This dynamic testing phase utilizes the same stimulus signal previously employed during the static condition optimization. The experiment involves varying the chip

temperature from -20°C to 40°C and adjusting the supply voltage from 3.3 V down to 2.6 V. To validate the optimization results and avoid the lucky shot solutions, each optimization iteration is repeated three times.

The output results of this experiment are graphically shown using the error bar graph in Figure 5.27. Additionally, the optimization convergence curves for this experiment are detailed in Figure 5.28. These graphs provide a clear visual representation of the in-field optimization's effectiveness. It demonstrates the system's capacity to autonomously adjust the CFIA settings to optimize the THD value while simultaneously minimizing power consumption. The results from these dynamic tests confirm the robustness and adaptability of the proposed optimization method under various environmental conditions. Configurations for CFIA dynamic conditions and various gain settings can be found in Appendix A.

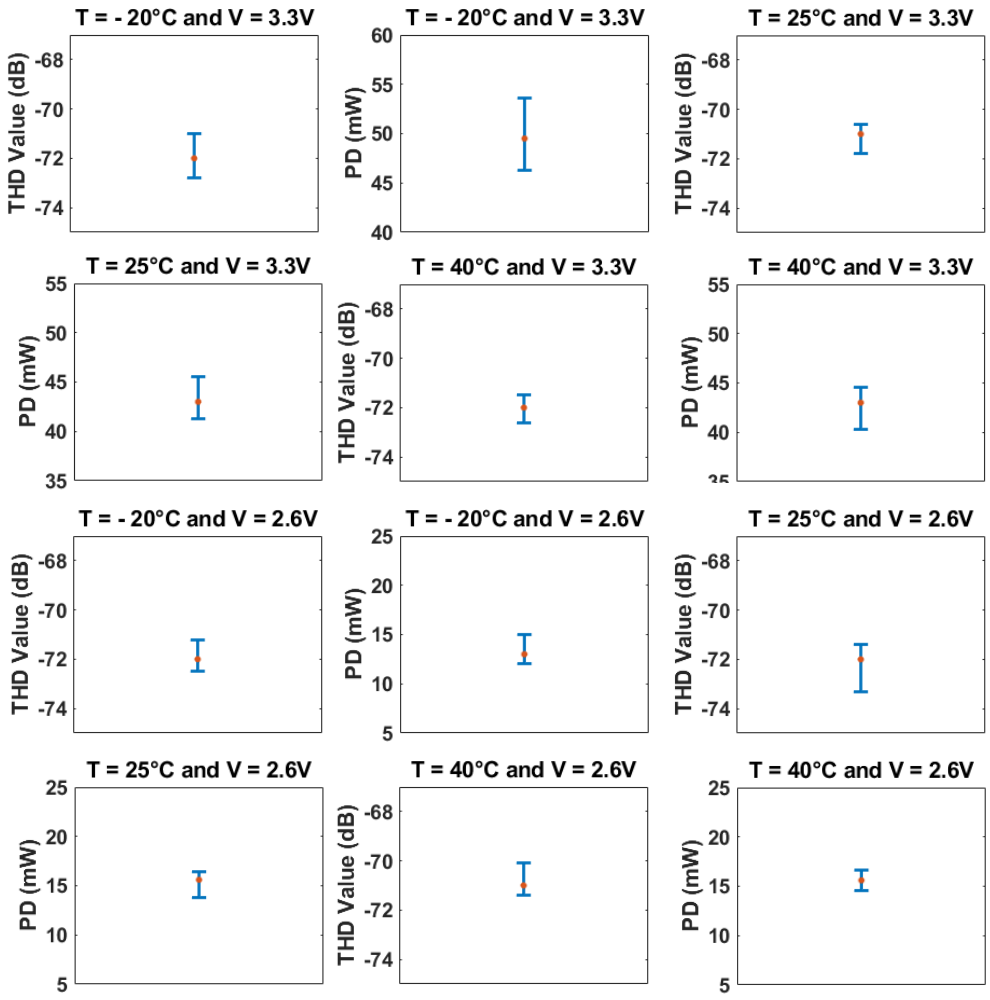

Figure 5.27: Error paragraph for dynamic optimization.

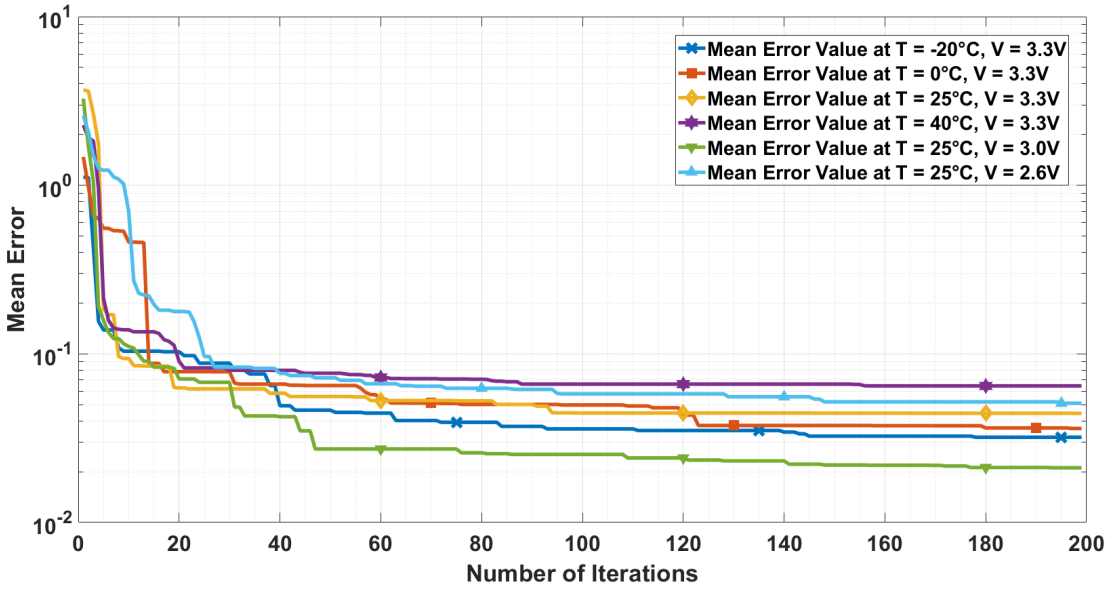

Figure 5.28: Optimization conversion error under dynamic operating condition

5.1.4 Extrinsic Evaluation of Robust Optimization for CFIA

In this subsection, the evaluation of robust optimization for CFIA is conducted extrinsically, focusing solely on simulation-based results due to timing constraints. The remainder of the section presents results derived from hardware implementations and practical experiments.

5.1.4.1 Surrogate-Based Robust Optimization

The effectiveness of the surrogate-based robust optimization approach is extrinsically evaluated on the complex objective space of the reconfigurable CFIAs. The experimental framework employed a sinusoidal test stimulus of 100 kHz frequency and a peak-to-peak amplitude of 2 V. The target THD is set to -75 dB. To mitigate the impact of channel length modulation, all transistors were uniformly sized at a length of 1 µm. The optimization process varied only the width of critical transistor elements.

The surrogate-based robust optimization algorithm is implemented using Python. The framework used to implement this process is shown in Figure 5.29. The robust optimization algorithm, written in Python, passes the solution particle information to the OCeaN (OCN) language in Cadence design tools using File 1, as presented in Figure 5.29. The OCN design tools execute the netlist simulation of the Device Under Test (DUT) and pass back the system output response to the robust optimization algorithm

using File 2. This system response is used as an objective function for the robust optimization. This process continues iteratively until the maximum number of iterations is reached.

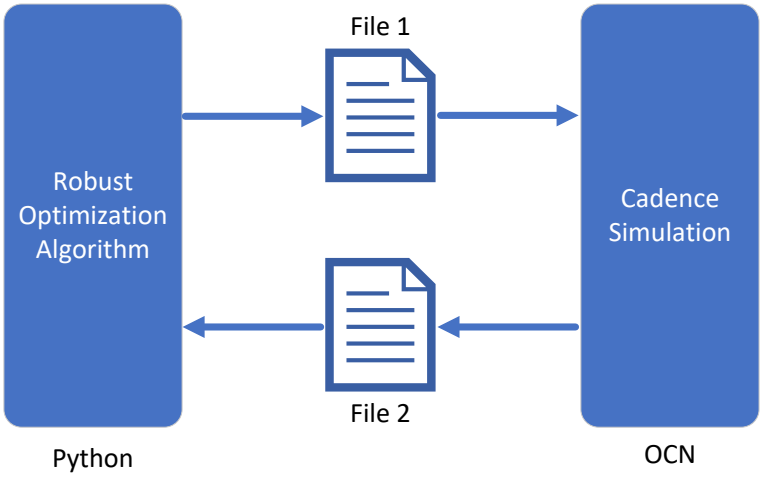

Figure 5.29: Framework for integrating Python-based optimization with OCeaN simulations in Cadence.

Table 5.4 presents the obtained performance characteristics of the CFIA after the optimization process. This table indicates that the THD-based indirect measurement technique successfully optimized the CFIA, meeting the predefined performance benchmarks. Moreover, to ensure reliability and avoid any lucky shots, the experiment is repeated for 15 independent runs. The results, representing a statistical compilation of these runs, are graphically represented through error bar graphs in Figure 5.30. Figure 5.31 compares the noisy and predicted output signals using the Gaussian process regression (GPR)-based robust optimizing with 95% confidence intervals. As seen from the figure, in addition to uncertainty level prediction, the GPR helps forecast the data, which can considerably minimize the transmission power of wireless sensor network applications.

To assess the performance of the surrogate-based robust optimization, the following six different error metrics are employed:

- The Root Mean Square Error (RMSE) is a fundamental metric in regression analysis employed to represent the Average Expected Error (AEE). It is defined by the following equation:

Table 5.4: Performance characteristics of the CFIA after the optimization, V_{DD} = 3.3 V, V_{CM} = 1.65 V.

CFIA design parameter	**Value**
Differential DC gain (A_{VD})	95.12 dB
Gain bandwidth product (GBW)	78.43 MHz
Phase margin (PM)	66.74°
Slew rate (SR)	207.61 V/µs
Differential input linear range (V_{ID})	2.22 V_{P-P}
Total harmonic distortion (THD)	−85.88 dB

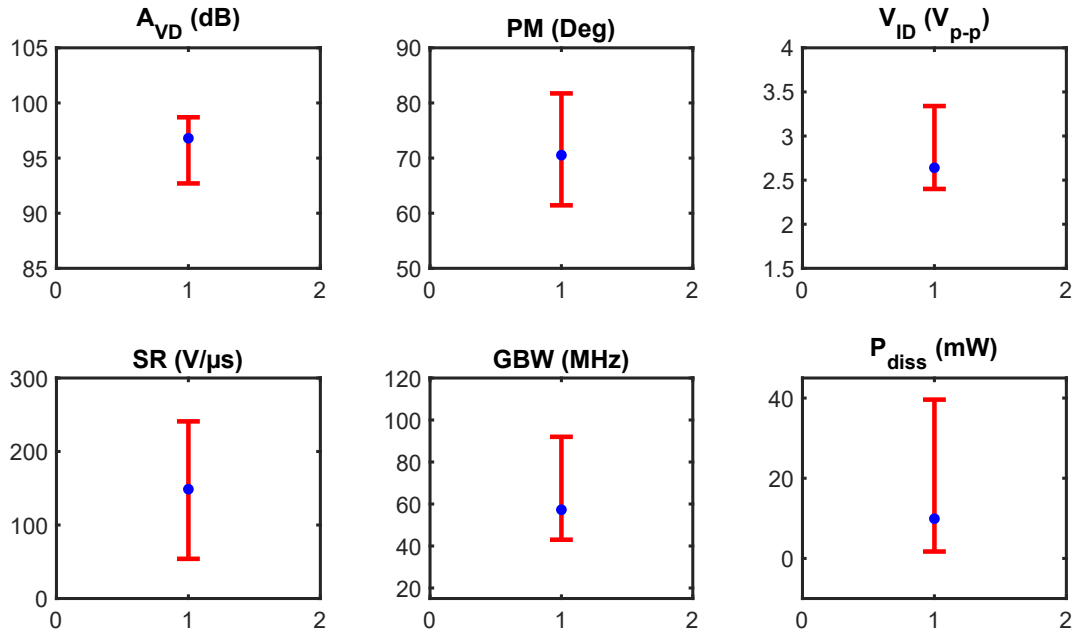

Figure 5.30: Error bar diagram of the six different performance characteristics of the reconfigurable CFIA by using LCRPSO over 15 independent simulation runs.

$$RMSE = \sqrt{\frac{\sum_{i=1}^{N}(y_i - \hat{y}_i)^2}{N}} \tag{5.1}$$

In this equation, y_i denotes the actual value, $\hat{y}_i$ the predicted value, and N the number of samples.

- Pearson's Correlation Coefficient is used to quantify the degree of correlation between actual and predicted values. It is expressed as:

$$p = 100 \cdot \frac{\mathrm{cov}(y, \hat{y})}{\sigma_y \sigma_{\hat{y}}} \tag{5.2}$$

Here, σ_y and $\sigma_{\hat{y}}$ are the standard deviations of the actual and predicted values,

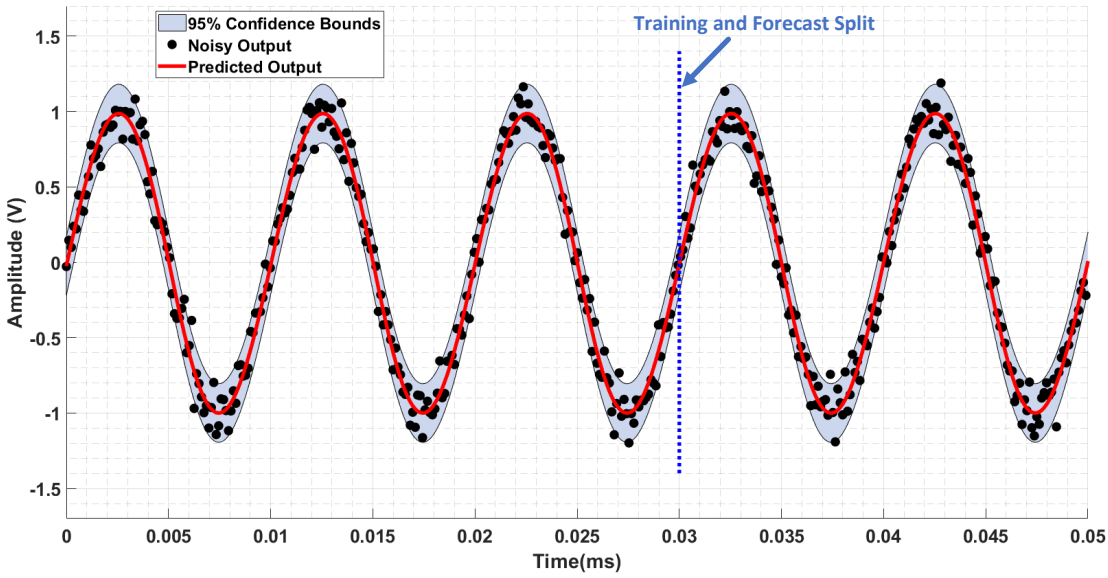

Figure 5.31: The predicted output with the 95% confidence interval and illustration of data forecasting capabilities by the application of GPR block.

respectively.

- The Mean Absolute Error (MAE) measures the absolute discrepancies between predicted and actual values. It is defined as:

$$MAE = \frac{1}{N}\sum_{i=1}^{N}|y_i - \hat{y}_i| \tag{5.3}$$

- The R-Squared Error, also known as the Coefficient of Determination, evaluates how closely data fits the predicted regression model. It is calculated as:

$$R^2 = \frac{\sum_{i=1}^{N}(y_i - \hat{y}_i)^2}{\sum_{i=1}^{N}(y_i - \bar{y})^2} \tag{5.4}$$

where $\bar{y}$ is the mean value of the data.

- Adjusted R-Squared, an extension of the R-Squared metric, adjusts for the number of predictors in the model relative to the number of observations:

$$\bar{R}^2 = 1 - (1 - R^2)\frac{N-1}{N-p-1} \tag{5.5}$$

- The Figure of Merit (FoM), as introduced in [178], correlates the RMSE with the standard deviation of the data, offering a perspective on the expected average error

Table 5.5: Performance evaluation of the GPR by using six various error metrics.

Nr.	**Error metrics**	**Value**
1	Root mean square error	0.286
2	Pearson's correlation	93.67
3	Mean absolute error	0.313
4	R-squared error	0.927
5	Adjusted-R squared error	0.908
6	Figure of merit	0.073

in relation to data variability:

$$FOM = \frac{RMSE}{\sigma_y} \tag{5.6}$$

The effectiveness of the robust optimizer is detailed in Table 5.5. Metrics such as MAE, FoM, and RMSE are indicative of the Average Expected Error (AEE); a lower value in these metrics signifies greater accuracy of the regression model. Conversely, values of R^2, p and $\bar{R}^2$ represent the degree of correlation between the predicted and actual values. A value nearing unity (or 100 in the case of p) denotes a more accurate prediction. As observed in Table 5.5, the highest recorded value for AEE metrics is 0.313. Regarding the correlation metrics, the lowest value recorded is 0.908, indicating a strong correlation between the estimated and ground truth.

5.1.4.2 Archive-Based Robust Optimization

In this experiment, firstly, an investigation into the efficacy of archive-based robust optimization was conducted using three benchmark (BM) functions derived from existing literature [111]. The experiment was executed with 30 particles over 150 iterations, maintaining all other initial parameters as outlined in the preceding chapter. Figure 5.32 displays the results: the first column indicates the specific BM function, and the second column illustrates the corresponding convergence curves. These curves demonstrate a variation in performance across the BM functions, with BM3 achieving convergence in fewer than 50 iterations, in contrast to the over 50 iterations required by the remaining functions. The convergence process was protracted, attributed to the inherent uncertainty in the system. Notably, the uncertainty level was progressively reduced by the archive-based robust optimization from 10% to approximately 1.8%, a margin that could be further narrowed by increasing the iteration count.

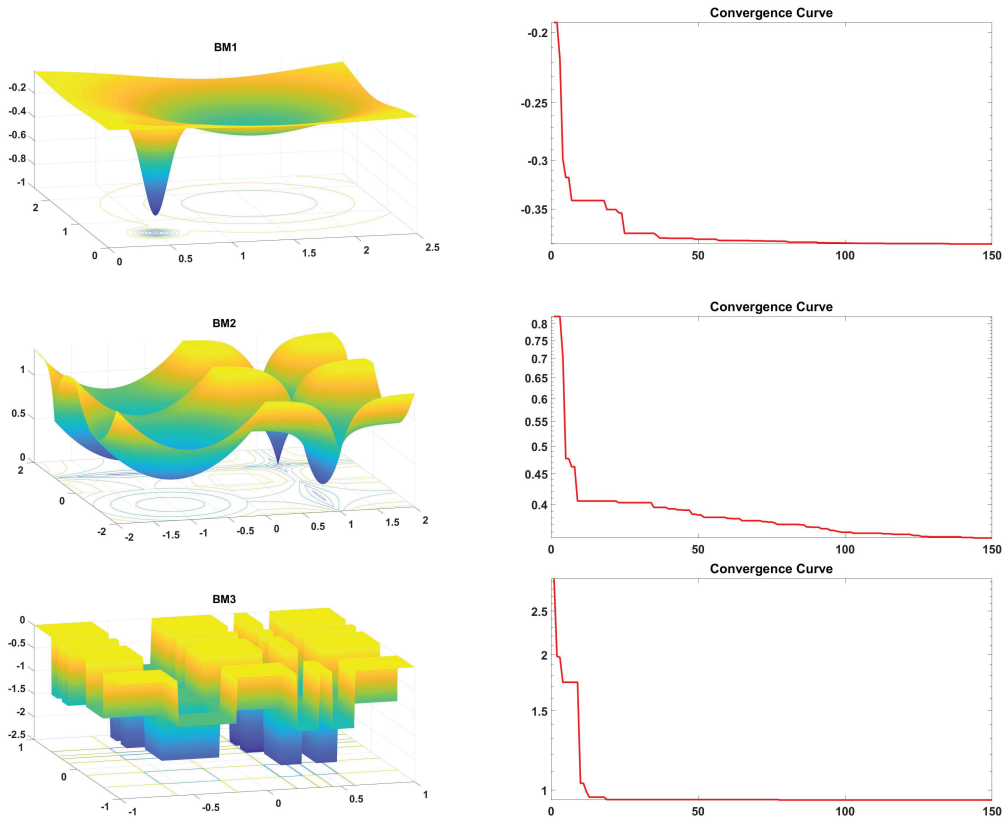

Figure 5.32: Behaviour of archive-based robust optimization on BM1, BM2, BM3.

Subsequently, the archive-based robust optimization was applied to the CFIA for extrinsic evaluation. This analysis focused on two primary objectives: THD and power consumption. An agglomerative method was utilized for multi-objective optimization. This evaluation utilized a sinusoidal waveform of 100 kHz and a peak-to-peak amplitude of 2 V as the test stimulus, with the aim of maintaining the THD below -75 dB. For consistency and to mitigate channel length modulation effects, all transistors were maintained at a uniform length of 1 µm, with the optimization algorithm adjusting only the transistor widths. The optimization algorithm was implemented in Python, with circuit simulations conducted using the Ocean Script language in Cadence design tools. Table 5.6 delineates the performance characteristics of the reconfigurable CFIA following the optimization. The optimization's efficacy is evident from the improved THD values, indicating the successful tuning of the CFIA to its desired performance metrics. This approach enabled the reduction of output root mean square error from 4.24% to 0.56%, leveraging the archive method's strength.

Additionally, to demonstrate the algorithm's capability to suppress measurement un-

Table 5.6: Performance characteristics of the CFIA after the optimization, V_{DD} = 3.3 V, V_{CM} = 1.65 V.

CFIA design parameter	**Value**
Differential DC gain (A_{VD})	91.79 dB
Gain bandwidth product (GBW)	81.13 MHz
Phase margin (PM)	65.94°
Slew rate (SR)	201.18 V/µs
Differential input linear range (V_{ID})	2.18 V_{P-P}
Total harmonic distortion (THD)	−86.07 dB

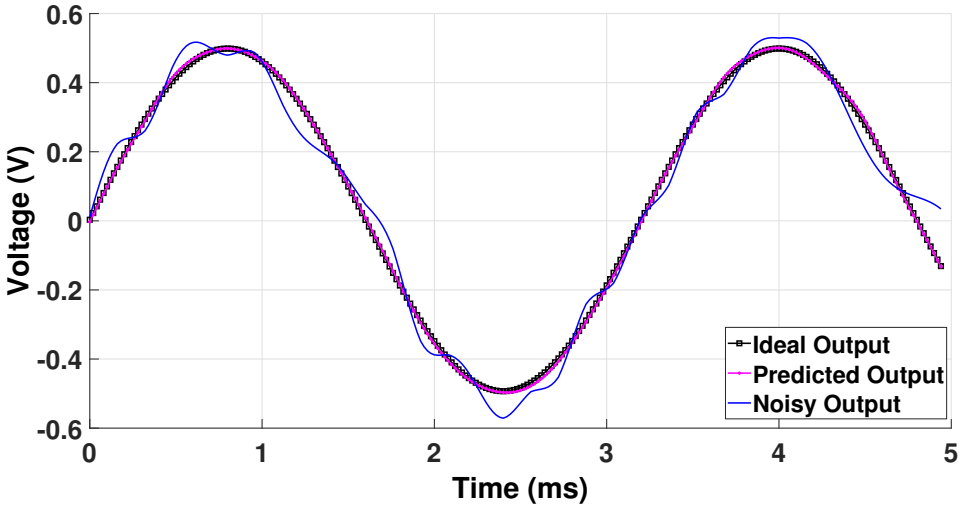

Figure 5.33: Comparison of the ideal, predicted (using robust optimization), and noisy output.

certainty, the voltage response of the CFIA in a unity configuration was examined using robust particles. Figure 5.33 compares the ideal output signal with both the predicted output of the CFIA and the noisy output resulting from observer uncertainty, achieved with a reduced setup of five particles and 80 iterations. The algorithm demonstrated its ability to recalibrate the system in the presence of uncertainty, thereby enhancing the reliability of the output.

5.2 Evaluation of Filter Optimization using Non-Intrusive Sensors

This section delves into the experimental exploration of filter optimization, utilizing a low-cost indirect measurement method with non-intrusive sensors. The setup for this experiment mirrors that used in the CFIA experiments, maintaining consistency in the experimental approach. It is important to clarify that the filter's performance evaluation

and verification are conducted on hardware, while the optimization using non-intrusive sensors is performed through simulations due to time constraints.

The exploration begins with a detailed presentation of experimental results from shadow register verification, a critical step in validating the reliability of measurements. Following this foundational analysis, the focus shifts to assessing the filter's performance under its default configuration, thereby establishing a baseline for subsequent optimizations.

A key aspect of this investigation is the examination of the filter's reconfigurability, particularly in terms of its cutoff frequency. The study demonstrates how the filter's cutoff frequency can be finely tuned by adjusting various configuration bits. This tunability is crucial in adapting the filter to different operational requirements. The impact of these adjustments is further illuminated by correlating the filter's performance with the readings from low-cost, non-intrusive sensors, showcasing the direct relationship between the filter's settings and sensor outputs.

The section then progresses to scrutinize the filter's behaviour under dynamic conditions, particularly focusing on the deviation of its cutoff frequency. The filter's resilience is tested, and strategies for recovering its performance through reconfiguration are discussed. These insights are derived from comprehensive measurements on the fabricated chip, demonstrating the filter's capabilities in real-world scenarios.

This section concludes with an in-depth overview of the self-X indirect measurement system, employing a low-cost indirect measurement method with non-intrusive sensors. The section offers an in-depth examination of the filter's reconfigurability, particularly in terms of its cutoff frequency, and assesses its performance under default and optimized conditions. The findings from this section underscore the feasibility and effectiveness of using non-intrusive sensors in conjunction with advanced optimization techniques to achieve desired performance characteristics in smart sensory electronics.

Due to time constraints, this comprehensive system is evaluated extrinsically. Nonetheless, these findings strongly indicate the system's intrinsic capabilities, suggesting that similar outcomes would likely be observed with a hardware implementation. The analysis effectively validates the functionality of each component, reinforcing the efficiency and coherence of the entire setup as an integrated system.

5.2.1 Filter Measurement Results

5.2.1.1 Initial Test of Filter

The following section details the filter testing process, as illustrated in the block diagram in Figure 5.34. The initial phase of the test involves an in-depth verification of the filter's shadow register, as presented in Figure 5.35. It is essential to note the filter's memory does not have external pins for direct access. As a result, data is relayed serially from the adjacent memory block of the CFIA. This testing step is essential to confirm the accurate transfer of the configuration bit patterns.

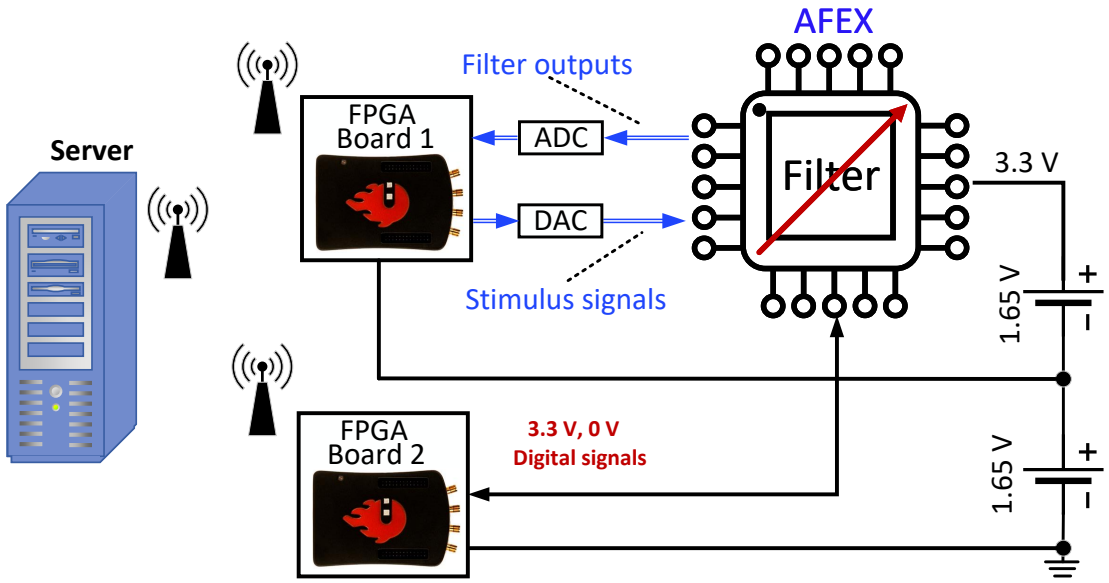

Figure 5.34: Detailed block diagram for the LAB filter testing procedure.

In the following test, the filter is configured using data derived from post-layout extrinsic evaluation, setting its cut-off frequency to 2.6 MHz. A sinusoidal signal with a frequency of 1 kHz and an amplitude of 1 Vp-p is applied to the filter under standard operating conditions (ambient laboratory temperature of 24°C and a supply voltage, V_{DD}, of 3.3 V). The resultant output, shown in Figure 5.36, indicates that the output amplitude maintains unity gain within the filter's pass band. Furthermore, the output demonstrates a phase shift of 179.49°, signifying good matching in the output differential stage.

The filter, featuring two amplifier stages, each consuming 13 mA, has a total current draw of approximately 26 mA at 24°C. Practical experiments have shown that utilizing the filter's programmable current source can effectively reduce the total current

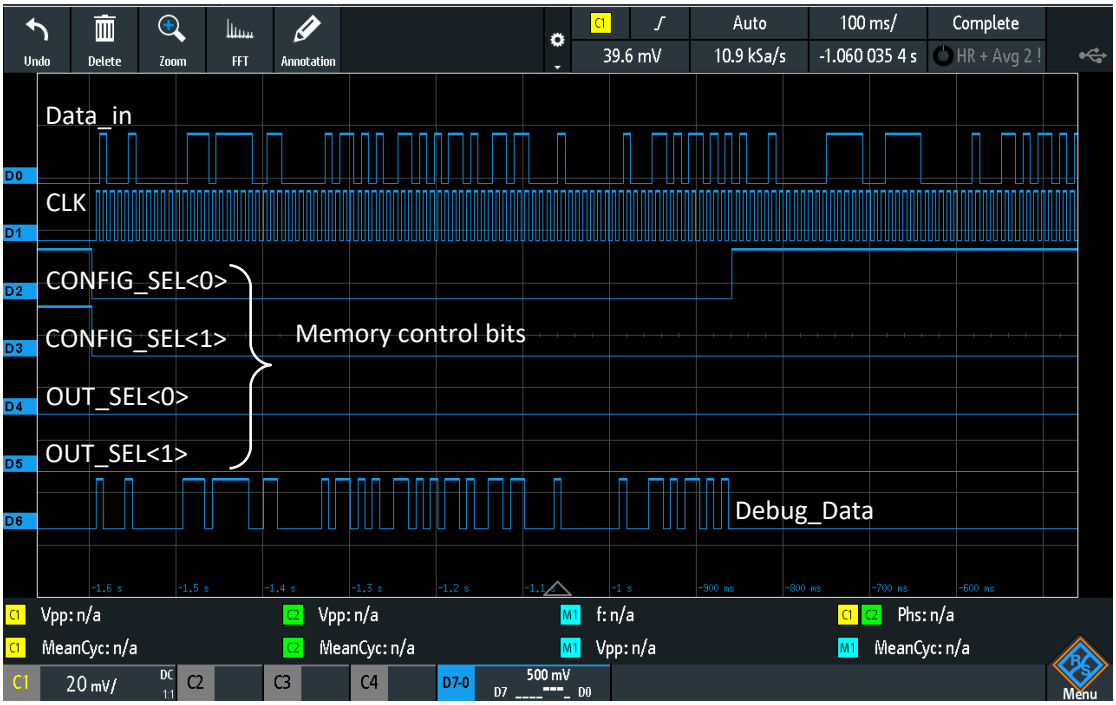

Figure 5.35: Verification test for the filter shadow register memory.

consumption to 11 mA without affecting the filter's operational functionality.

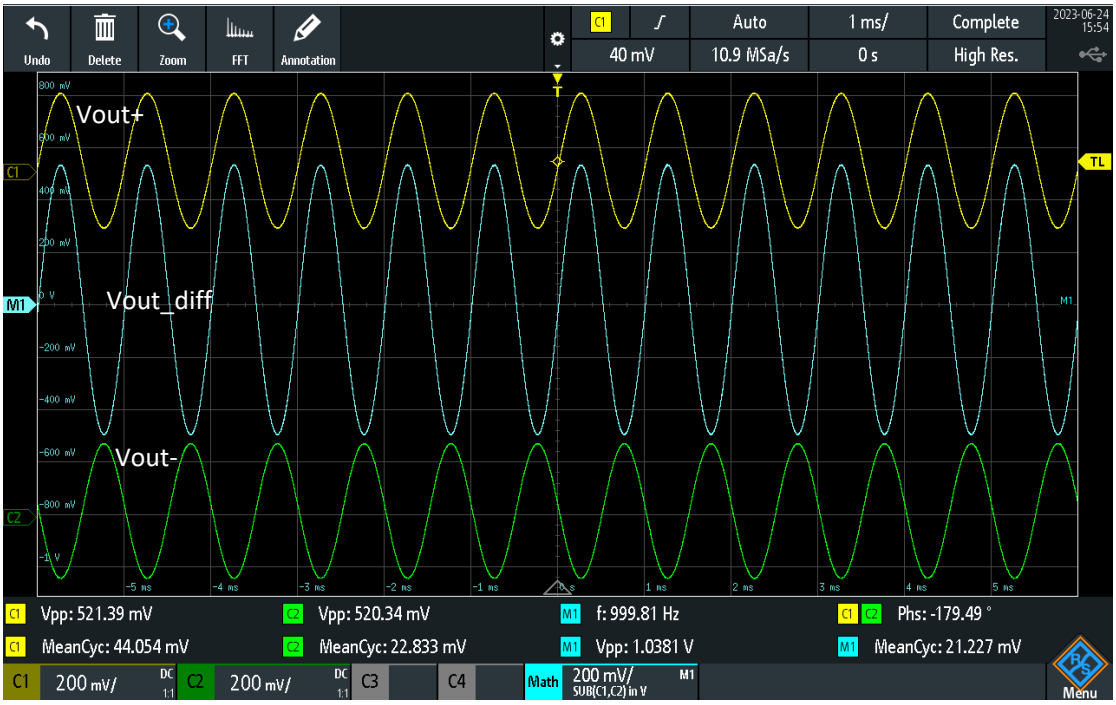

Figure 5.36: sinusoidal transient response of the filter

The small-signal AC response is assessed using a sinusoidal signal of 100 mV amplitude. As depicted in Figure 5.37, the results demonstrate a roll-off of less than -80 dB. This aligns with the post-layout simulation predictions, suggesting an effective filter

order of less than four. The observed low-frequency gain of -6 dB, resulting from using a single output during measurements, corresponds to the filter's 0 dB linear differential (unity) gain.

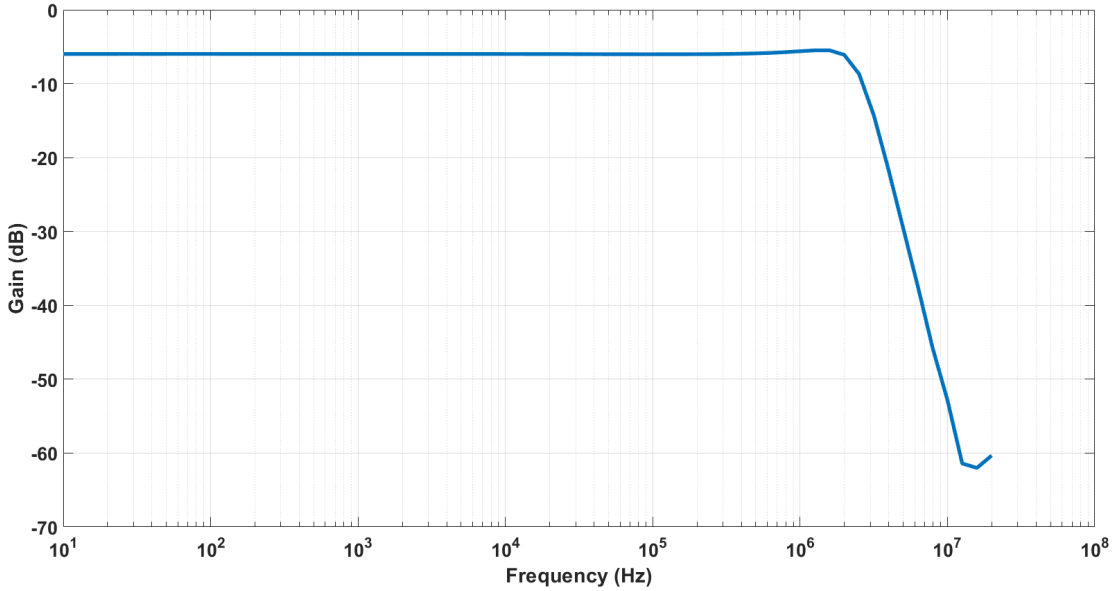

Figure 5.37: Small-signal AC response of the filter using one of the extrinsic patterns at typical operation condition: T= 22°C and V_{DD}= 3.3 V.

The impulse response is examined by applying a square signal to assess the filter's stability under unity-gain conditions. While stability can be predicted from the small signal AC response peaking, experimental validation is conducted by exciting the filter with a sharp-edged pulse. As shown in Figure 5.38, the results affirm the filter's stability and validate its Butterworth performance through a smooth transition into the settling region.

As previously introduced, there are three non-intrusive sensors, two non-intrusive sensors NIS1 and NIS2, operate using the same filter configuration, and the third temperature sensor does not require any configuration bits. Tested at T=24°C, their outputs, presented in Figures 5.39, 5.40, and 5.41, reveal the expected quasi-digital form. Using the Red Pitaya board, the frequency-modulated signal allows straightforward conversion to digital equivalent weight (F/D). Moreover, all sensors have the respective enabled signal for power optimization.

The relationship between the filter bandwidth and the outputs of the non-intrusive sensors (NISs) is explored under various filter configuration settings. Table 5.7 demonstrates a proportional yet nonlinear correlation between the frequencies of the NISs and

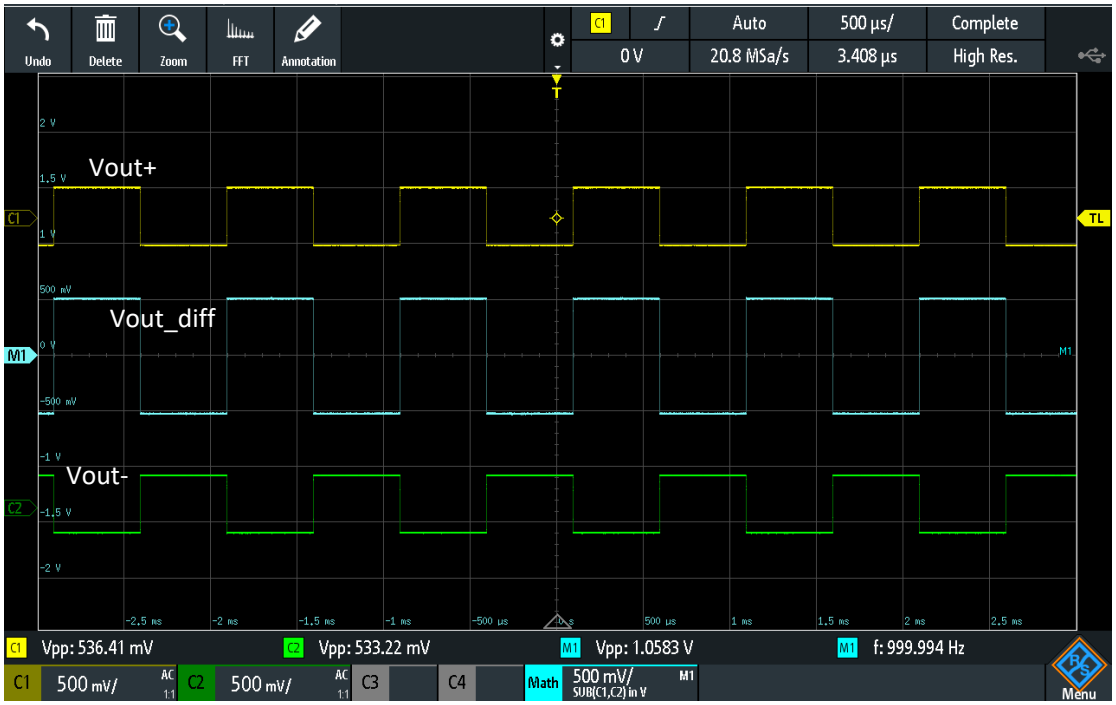

Figure 5.38: Implulse response of the filter confirming the stability using one of the extrinsic patterns at typical operation condition: T = 22°C and V_{DD}= 3.3 V.

Figure 5.39: The output from non-intrusive sensor1 using one of the extrinsic patterns at typical operation condition: T = 24°C and V_{DD}= 3.3 V.

the filter bandwidth. To model this nonlinearity, a regression model can be easily utilized to indirectly estimate the filter's cut-off frequency. It can be observed that when the frequency fell below 1 kHz, Sensor1 reached a saturation point in its measurements,

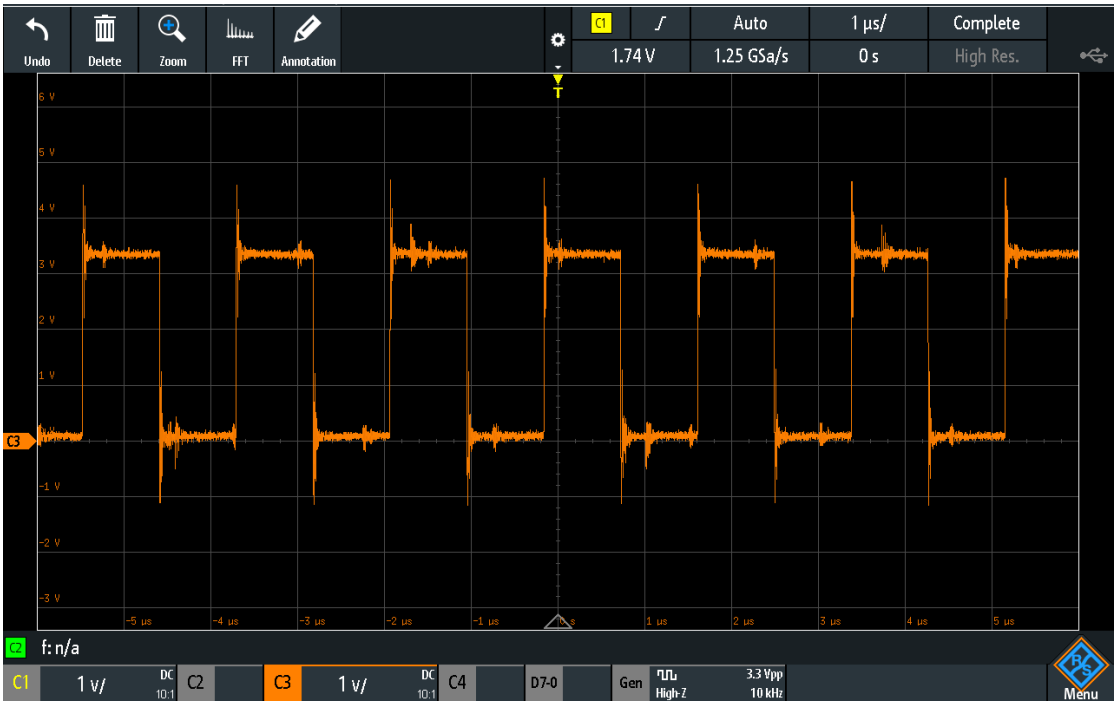

Figure 5.40: The output from non-intrusive sensor2 using one of the extrinsic patterns at typical operation condition: T = 24°C and V_{DD}= 3.3 V.

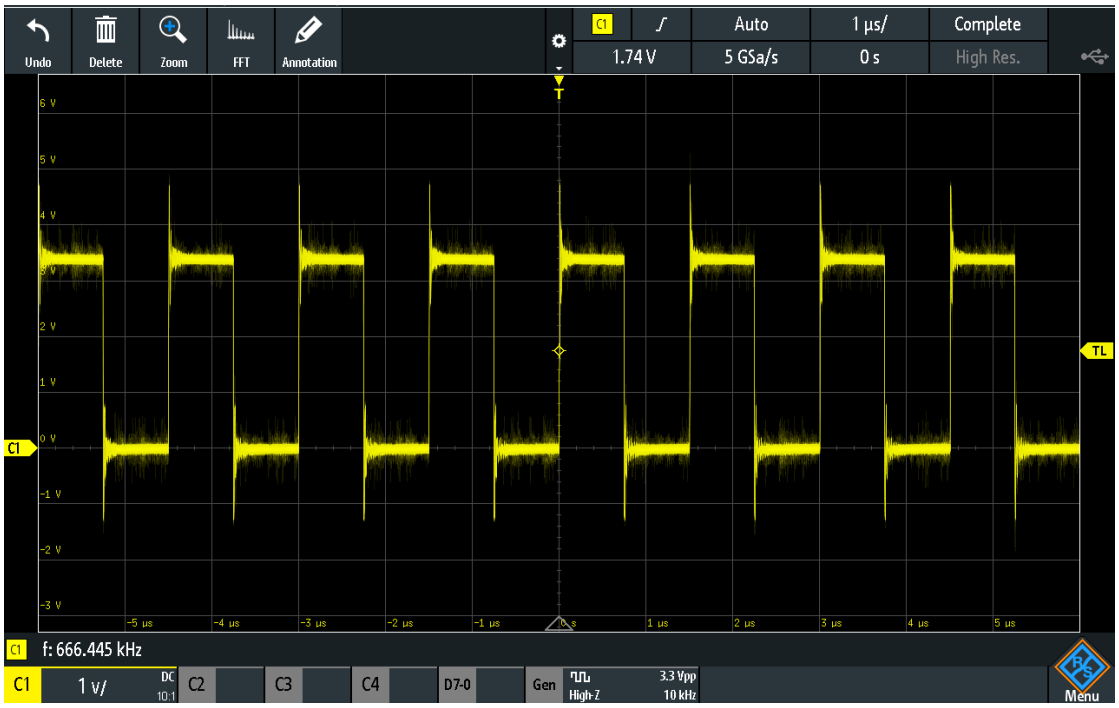

Figure 5.41: The temperature sensor output at T = 24°C and V_{DD}= 3.3 V.

in contrast to Sensor2, which continued to display proportional variations. Furthermore, the integrated on-chip temperature sensor played a crucial role in validating the regression model, facilitating the indirect prediction of the filter frequency in dynamic operational conditions.

Table 5.7: Filter bandwidth and non-intrusive sensors outputs T = 24°C and V_{DD}= 3.3 V.

Filter Bandwidth	**Sensor1**	**Sensor2**
10 MHz	24.6 MHz	6.37 MHz
6.7 MHz	7.51 MHz	5.44 MHz
2.6 MHz	5.03 MHz	4.49 MHz
234 kHz	761.3 kHz	1.66 MHz
140 kHz	515.26 kHz	1.29 MHz
37.2 kHz	185.5 kHz	562.5 kHz
1.7 kHz	26.62 kHz	80.5 kHz
427 Hz	33.71 kHz	66.7 kHz
276 Hz	33.03 kHz	30.91 kHz

5.2.1.2 Filter Dynamic Performance

This experiment evaluated the effect of temperature variations on the filter's AC performance. Initially, the filter is configured at an ambient temperature of 24°C, with the aim of establishing specific cut-off frequencies at various points: 67 Hz (minimum), 1 kHz, 10 kHz, 100 kHz, 1 MHz, 5 MHz, and 10 MHz. The experiment proceeded by placing the filter assembly within a climate chamber, as illustrated in Figure 5.42, and gradually changing the temperature from −20°C to 40°C.

Figure 5.43 shows that the filter bandwidth is sensitive to temperature-induced variations. However, the filter's inherent reconfigurability or tunability allows for recalibration by manually adjusting the MOS resistors, thereby updating the configuration pattern that controls the MOS pole resistors. The recalibration results, presented in Figure 5.44, shows that the cut-off frequencies realign to their intended values. However, at 67 Hz and T = 40°C, the measurement could not be conducted due to equipment limitations. As a result, the corresponding fields in Table 5.8 are marked as 'N.A.' to reflect this constraint. This suggests that the filter's adjustable range at T = 40°C spans from approximately 100 Hz to 10 MHz. Additionally, the spectral range was limited to 25 MHz due to constraints imposed by the digital storage oscilloscope (DSO) used in these tests.

Table 5.8 summarizes the filter's bandwidth before and after these adjustments, indicating a maximum discrepancy of 3% within the successfully recalibrated range. The configurations for dynamic filter conditions and various cutoff frequency settings are documented in Appendix A.

Table 5.8: The filter cut-off frequency under dynamic temperature test comparing the results before and after tuning

Cutoff Frequency	**Cutoff Frequency Deviations**		**Recentered Cutoff Frequency**		**Error Before Tuning**		**Error After Tuning**	
	-20 °C	40 °C	-20 °C	40 °C	-20 °C	40 °C	-20 °C	40 °C
67 Hz	28 Hz	N.A.	66 Hz	N.A.	58%	33%	1.5%	N.A.
1 kHz	478 Hz	1.48 kHz	0.97 kHz	1 kHz	52%	48%	3.0%	0.0%
10 kHz	5.6 kHz	10.7 kHz	9.81 kHz	9.87 kHz	44%	7%	1.9%	1.3%
100 kHz	87 kHz	116 kHz	98 kHz	100 kHz	13%	16%	2.0%	0.0%
1 MHz	800 kHz	1.1 MHz	1 MHz	1.01 MHz	20%	10%	0.0%	1.0%
5 MHz	5.9 MHz	4.85 MHz	5.01 MHz	5.01 MHz	18%	3%	0.0%	0.0%
10 MHz	11.8 MHz	9.8 MHz	10.2 MHz	9.8 MHz	18%	2.0%	2.0%	2.0%

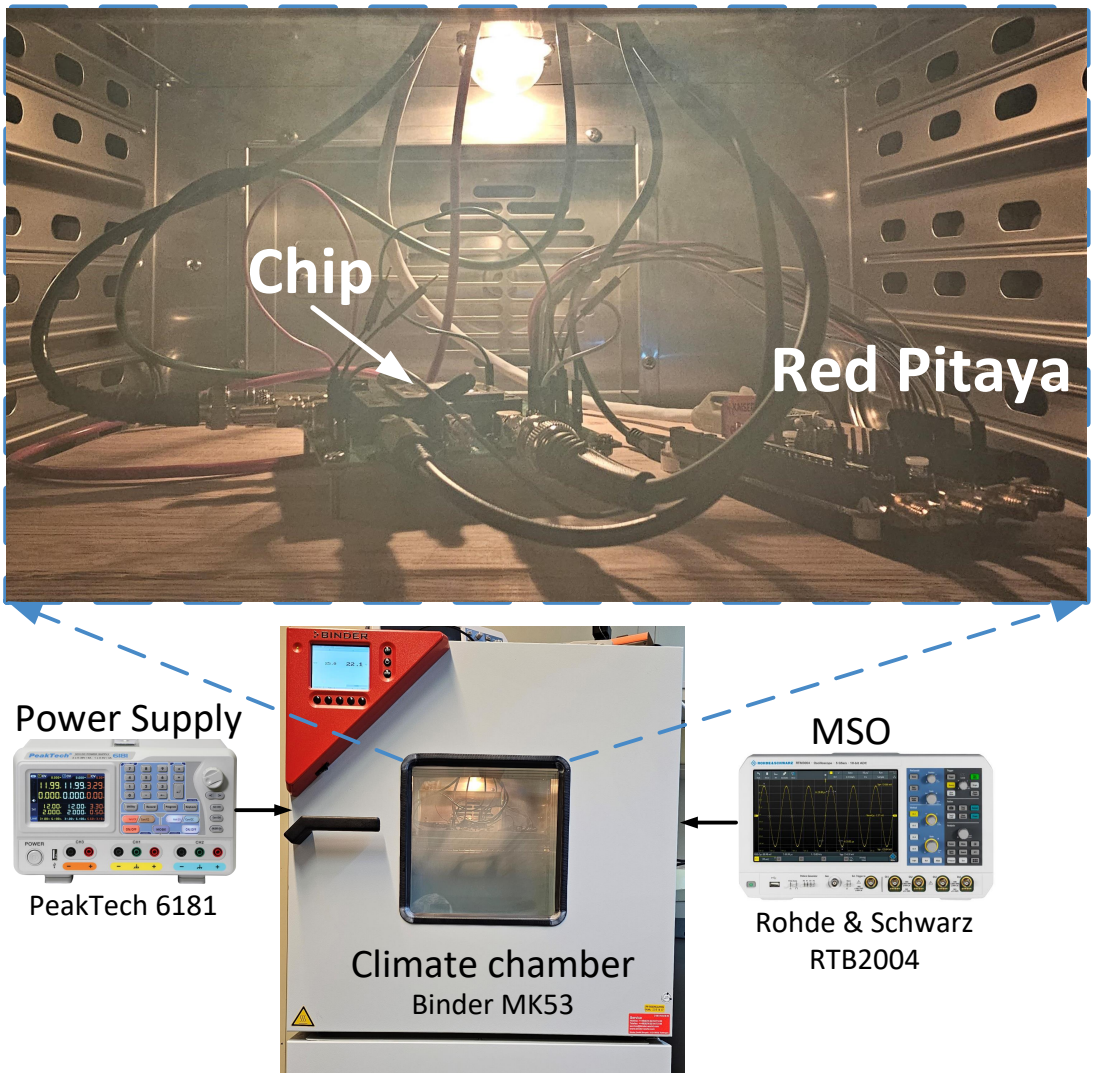

Figure 5.42: Dynamic test of the filter using the climate chamber

Furthermore, the temperature sensor is tested for the temperature range from −20°C to 70°C, with a stepsize of 5 degrees. As depicted in Figure 5.45, the frequency response varied proportionally with temperature changes while maintaining a consistent duty cycle of approximately 50%.

5.2.2 Extrinsic Evaluation of the Non-Intrusive Sensors based Indirect Measurement Method

This experiment employs a fully differential fourth-order tunable continuous-time active low-pass filter, based on the Sallen–Key structure with a Butterworth approximation, as the device under test (DUT) [172]. As explained before, to simplify the machine learning (ML) regression task and reduce the search space complexity, the DUT and

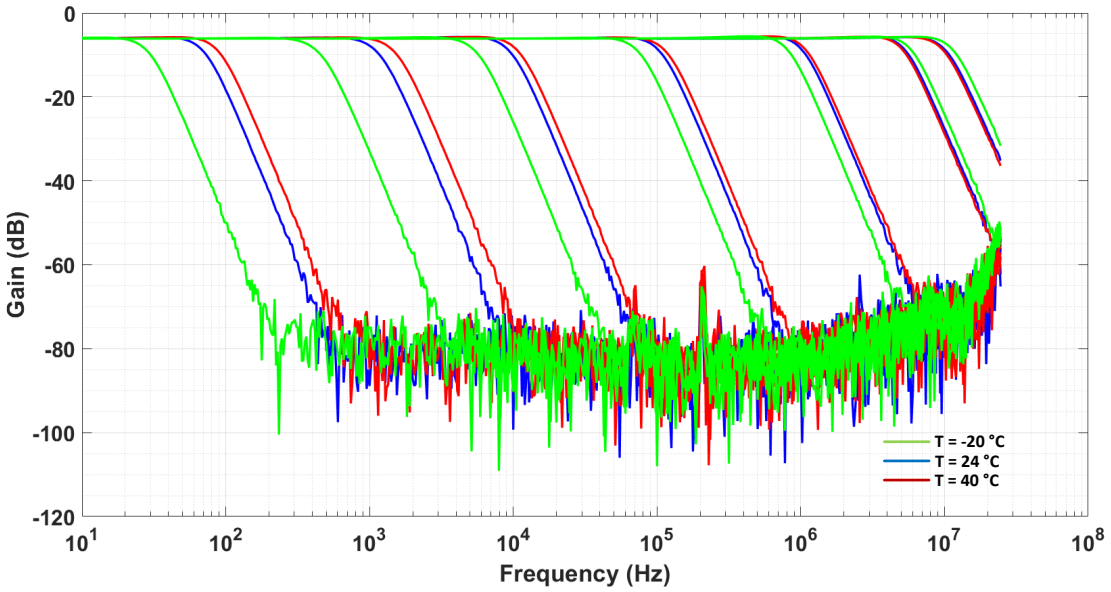

Figure 5.43: The filter small-signal AC response performance under dynamic temperature change at different cut-off frequencies

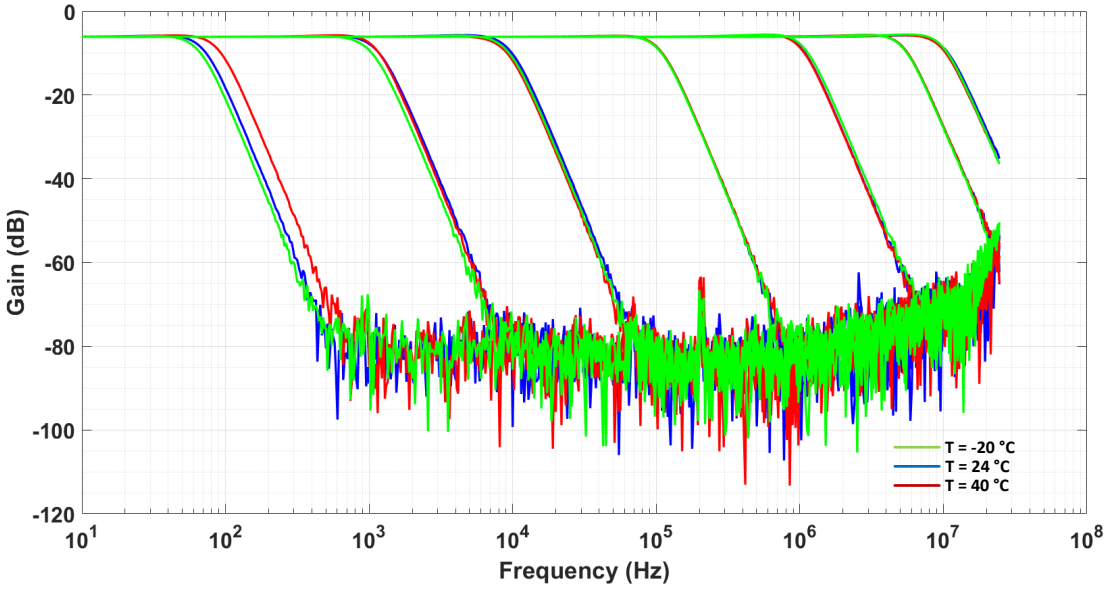

Figure 5.44: The filter small-signal AC response performance under dynamic temperature after bandwidth recovery

non-intrusive sensors share similar tuning knob (TK) values. A digitized MOS resistor, serving as a TK, is utilized to set the filter's cutoff frequency. These TK values are copied to the main DUT after the completion of the optimization process. The low pass filter's cutoff frequency is selected as the performance characteristic to be optimized. Random forest regressor (RFR) is used to create an accurate regression model between the non-intrusive sensor's outputs, TK values, and DUT performance. This RFR comprises 1000 estimators and uses mean squared error as its criterion. For this specific experiment,

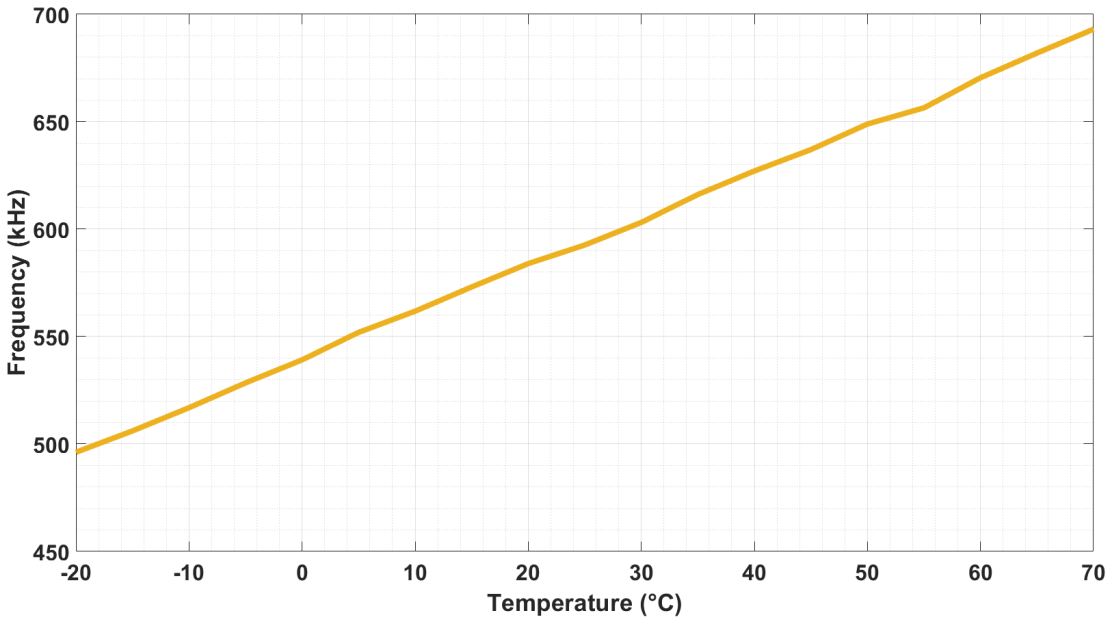

Figure 5.45: Temperature sensor test at V_{DD}= 3.3 V using the climate chamber

all ERPSO performance parameters are maintained at default values, as previously explained, with the adjustment to include 10 particles and 100 iterations. The effectiveness of the RFR is visually depicted in Figure 5.46, using 20% of the testing data set from the schematic data set.

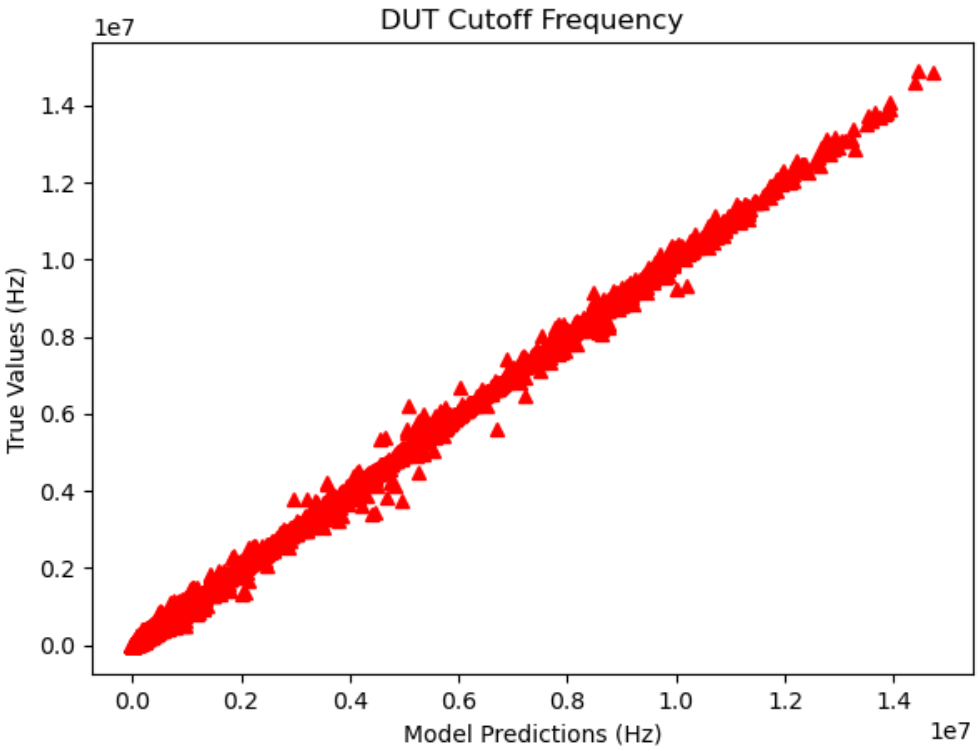

Figure 5.46: Scatter plot illustrating the correlation between predicted and actual values from the schematic dataset.

Six different performance metrics are employed to evaluate the prediction accuracy of the methodology. The results, summarized in Table 5.9, indicate the highest mean square error of 0.09. In terms of correlation metrics, the lowest value recorded is 0.92, signifying a strong correlation between estimated and actual values.

Table 5.9: Performance evaluation of the regression model for the schematic dataset of the LPF using various error metrics.

Nr.	**Error metrics**	**Value**
1	Root mean square error	0.08
2	Pearson's correlation	94.51
3	Mean absolute error	0.09
4	R-squared error	0.93
5	Adjusted-R squared error	0.92
6	Figure of merit	0.05

Furthermore, the experiment was conducted five times with different cutoff frequencies for the filter to ensure robustness and avoid the lucky shot. The average results of these individual runs are summarized in Table 5.10. Notably, the maximum optimization error was approximately 9% at 1 kHz, suggesting potential for further minimization by increasing the training data set around this frequency range.

Table 5.10: Averaged optimization results of the DUT characteristics for five individual runs.

DUT Characteristic	**Targeted**	**Achieved**
3 dB cut-off frequency	5 MHz	4.95 MHz
	1 MHz	1.03 MHz
	100 kHz	94.37 kHz
	10 kHz	9.56 kHz
	1 kHz	1.09 kHz

5.2.3 Enhancing Regression Model Robustness to Compensate for Fabrication Deviations

This section explores the approach of addressing deviations caused by chip layout to simulate the effects that might occur in fabricated chips. By tackling these layout-induced deviations, the study demonstrates the potential applicability of the methodology to real-world fabricated chips. The process begins with the application of a regression model, originally trained on schematic simulations of the Low Pass Filter (LPF), to a dataset derived from layout simulations. This step is crucial to understand how layout variations

might reflect in a fabricated environment. Figure 5.47 illustrates the results of this application, showing a correlation between the schematic and layout simulations. However, due to the deviations inherent in the layout simulation, the regression model trained on the schematic dataset is not directly transferable. This is evident in Table 5.11, where the deviation impact is quantified, showing an increase in the AEE metric to 0.48 and a decrease in the correlation metric to 0.61.

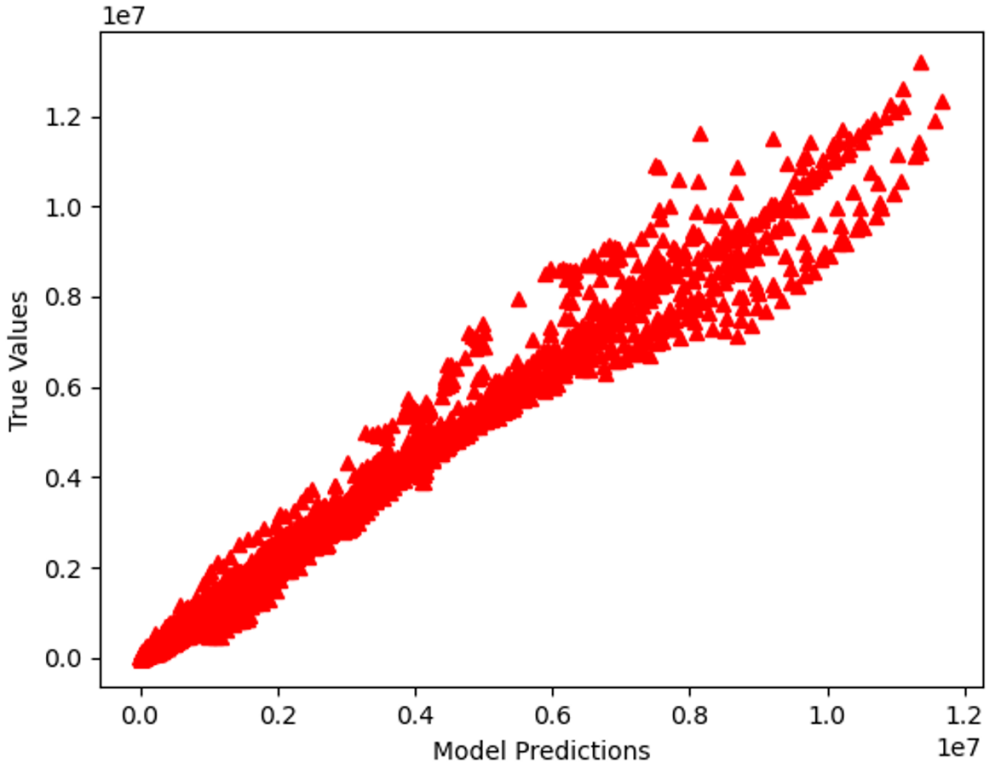

Figure 5.47: Scatter plot depicting the deviation between predicted and actual values in the layout simulation dataset.

Table 5.11: Performance evaluation of the regression model for the layout simulation dataset of the LPF using various error metrics.

Nr.	**Error metrics**	**Value**
1	Root mean square error	0.48
2	Pearson's correlation	64.12
3	Mean absolute error	0.41
4	R-squared error	0.64
5	Adjusted-R squared error	0.61
6	Figure of merit	0.37

A reinforcement learning approach is employed to adapt the regression model to these layout-induced deviations. This technique involves using a new, limited dataset that reflects the deviations from the layout simulation, thereby updating the regression

model initially trained on the schematic data. In this experiment, the layout simulation dataset comprises 15% of the size of the schematic dataset used for the initial training. The results post-application, shown in Figure 5.48, indicate a significant improvement in model accuracy. Table 5.12 confirms this, with performance metrics showing marked improvement, including a decrease in the highest AEE metric to 0.13 and an increase in the lowest correlation metric to 0.91.

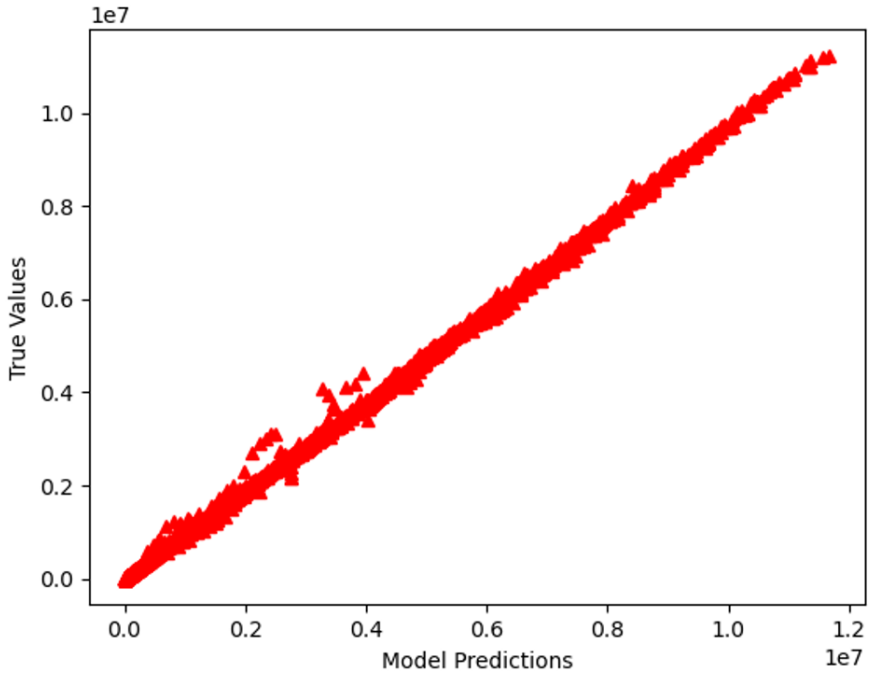

Figure 5.48: Scatter plot showing improved correlation in the layout simulation dataset post-deviation adjustment using reinforcement learning.

Table 5.12: Performance evaluation of the regression model for the layout simulation dataset of the LPF after reinforcement learning.

Nr.	**Error metrics**	**Value**
1	Root mean square error	0.13
2	Pearson's correlation	94.02
3	Mean absolute error	0.11
4	R-squared error	0.93
5	Adjusted-R squared error	0.91
6	Figure of merit	0.07

This concept effectively addresses deviations caused by layout simulation and can be seamlessly extended to manage deviations arising from the fabrication process. The adapted regression model demonstrates the potential to predict the performance of a

fabricated chip, requiring only minimal real measurements for model validation. Considering the time and resource constraints often associated with extensive measurement campaigns on fabricated chips, this approach offers a significant advantage.

Although the implementation on a physically fabricated chip has not been conducted due to timing constraints, the results observed in the above subsection with the measurement results of filter and non-intrusive sensors indicate expected and favourable outcomes. Therefore, it is reasonable to anticipate that similar results could be achieved at the chip level. This projection is based on the consistent behaviour exhibited by the non-intrusive sensors and the filter under study, suggesting a high likelihood of comparable performance in actual chip fabrication scenarios.

Chapter 6

Sensory System Application

This chapter focuses on the practical application and analysis of a sophisticated sensor system, particularly emphasizing the integration and optimization of the system components. The experimental configuration is outlined, and analytical results derived from the experiments are presented. Central to this study is the deployment of a reconfigurable analog front-end with self-X properties for the tunnel magneto-resistance (TMR) sensor, provided by Sensitec, specifically for angular encoding applications. This is coupled with sophisticated data acquisition and processing techniques to highlight the sensor system's effectiveness and adaptability in practical applications.

A pivotal element of this study is the application of configuration bits obtained from algorithm solutions developed in the preceding chapter. Under the umbrella of the Self-X optimization method, this approach highlights the harmonious integration of theoretical and algorithmic progress with their practical implementation in sensor systems. The configurations derived from these solutions are instrumental in fine-tuning the sensor system for optimal performance.

6.1 Experimental Configuration

This section outlines the experimental setup utilized for the study. The experiment incorporates the TMR sensor manufactured by Sensitec, which operates on a 3.3 V DC voltage. It features dual-balanced, fully differential bridge circuits. These circuits generate two differential signals, each offset by 90° and a common mode voltage centred around 1.65 V. Figure 6.1 [179] depicts the LAB functional setup.

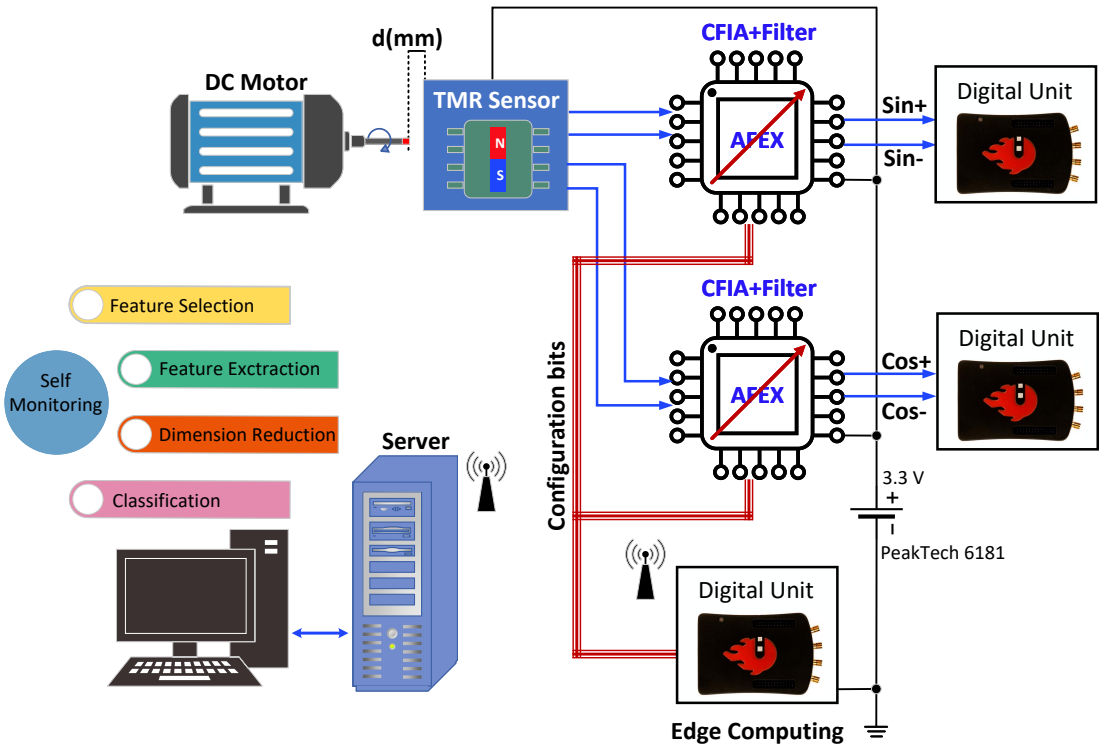

Figure 6.1: The functional setup of the proposed interface with TMR sensor.

For data acquisition, the configuration includes two FPGA Red Pitaya boards, processing the amplified and filtered signals from the sensor through custom AFEX chips, utilizing the onboard 14-bit RF ADCs of the Red Pitayas. Additionally, a third FPGA board is dedicated to configuring the AFEX chips. A key aspect of this configuration is the use of configuration bits derived from one of the algorithm solutions identified by the Self-X optimization approach, as presented in the previous chapter.

Although a configuration utilizing only two FPGAs for both signal acquisition and system configuration is feasible, this setup aligns the ground level of the FPGAs to the common mode voltage of the bridge. The AFEX chips, in contrast, are referenced to 0V. An alternative approach involving a DC-level shifter permits using just two FPGA boards. The server unit oversees the execution of the self-X algorithm for angle computation and anomaly detection. Another doctoral candidate in our research group is investigating the application of self-x concepts to sensor systems at multiple levels [179]. In this context, the angular decoder is employed as a comprehensive case study giving the opportunity to join Self-X work from sensor, sensor electronics to abstract software layer [180]. The TMR sensor is placed on the front of the DC motor's rotary shaft. Details on the TMR readout circuit are provided in Figure 6.2.

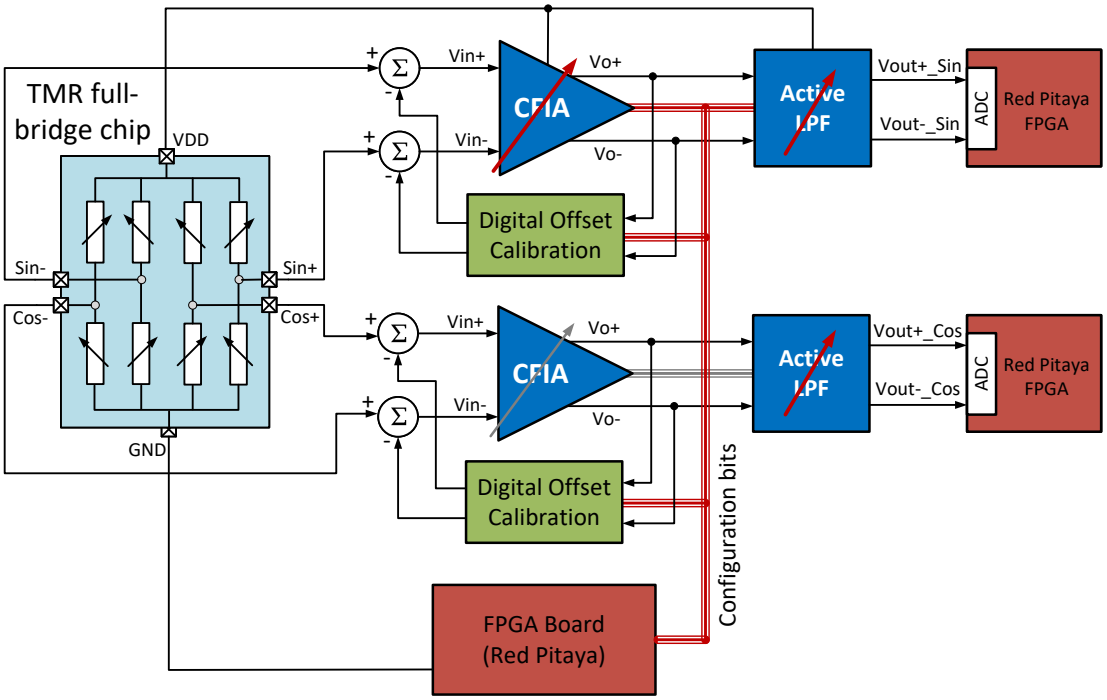

Figure 6.2: The schematic diagram of the proposed TMR readout circuit.

The CFIA offset voltage autozeroing feature is a viable method for compensating the sensor bridge's offset voltage. In addition to the automatic circuit, the offset voltage trimming pattern can be externally configured using the Self-X algorithm. These offset compensation patterns are then transferred to the shadow register. The total number of configuration bits employed to program the CFIA and filter is 88, including those for offset correction. This extensive customization capability enhances the precision and adaptability of the experiment. The laboratory setup, demonstrating the complete TMR sensor assembly, is depicted in Figure 6.3.

6.2 Measurement Results

The experiments were conducted with the filter cutoff frequency set at 1 kHz. This value is ten times higher than the highest frequency expected from the DC motor at maximum speed, ensuring no signal attenuation in the TMR outputs. Initially, the TMR sensor is positioned 4 mm from the motor shaft. The in-amp gain is set at unity to observe the TMR signal without amplification. Figure 6.4 shows that the differential outputs were approximately 0.5 Vp-p with a phase shift of 90°, indicating sine and cosine signals. Given the ADC's full-scale voltage of 2 Vp-p, the gain was adjusted to 4 at this distance,

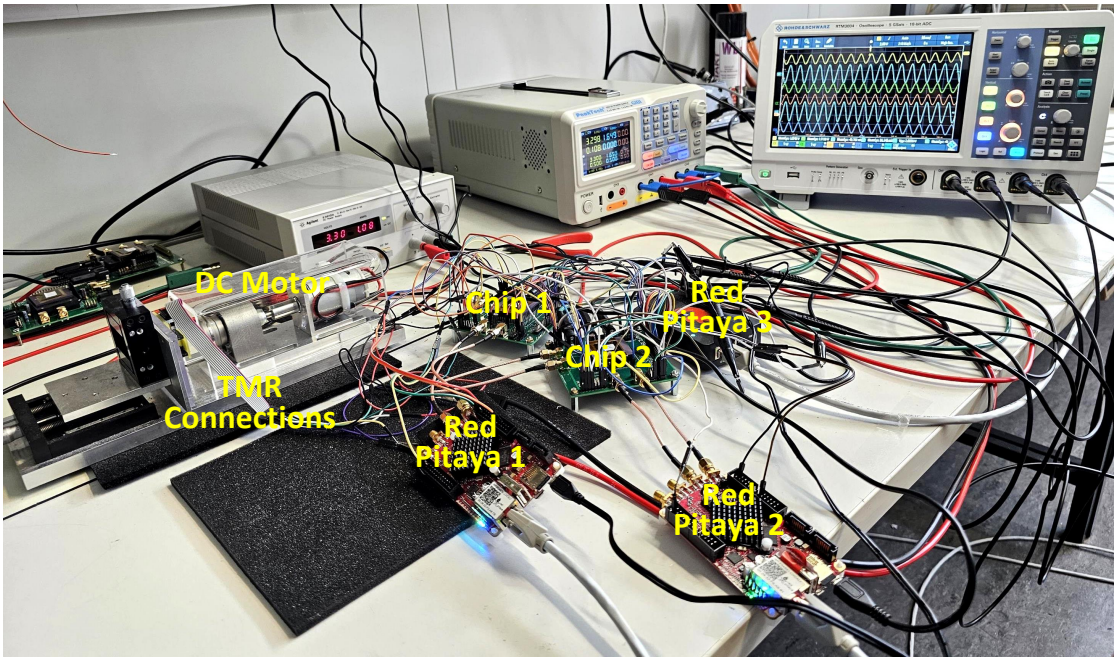

Figure 6.3: LAB setup for TMR interface using the proposed AFEX chip.

with results shown in Figure 6.5.

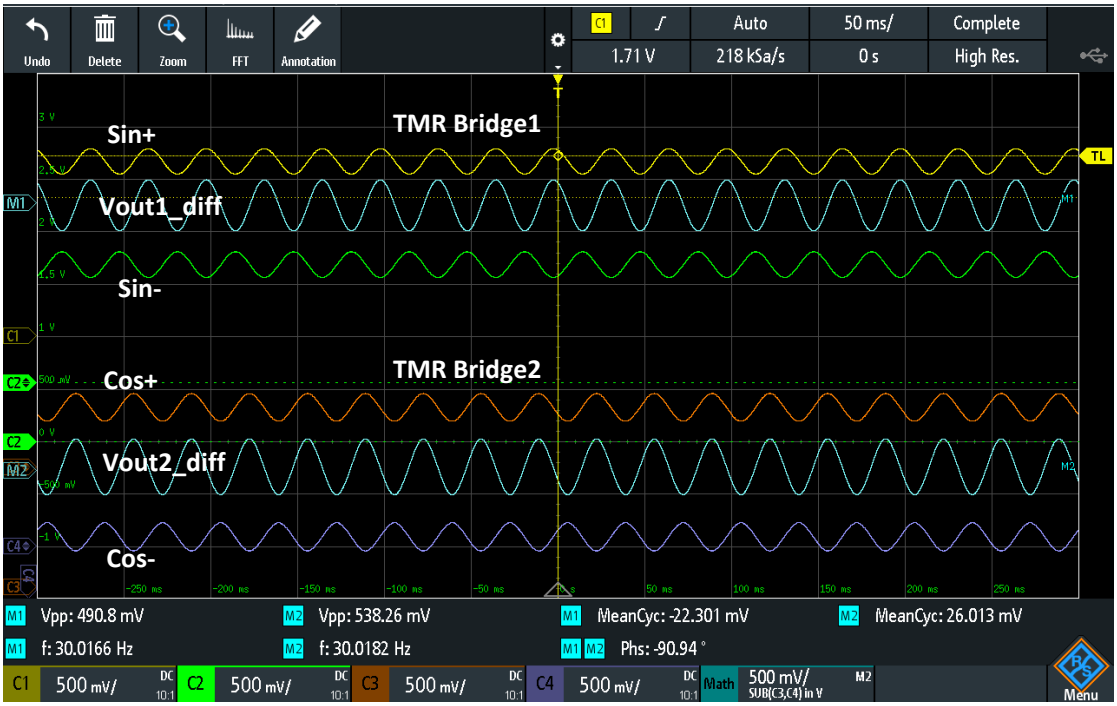

Figure 6.4: TMR sensor outputs at the in-amp gain of unity and distance of 4 mm.

However, it is observed that the offset voltage, which represents the combined effect of the sensor and the in-amp, is also amplified by a factor of 4. It is evident from the mean cycle measurement. With the amplifier configured for unity gain, it was inferred that the contribution of the filter's offset voltage was negligible. An autozeroing scheme

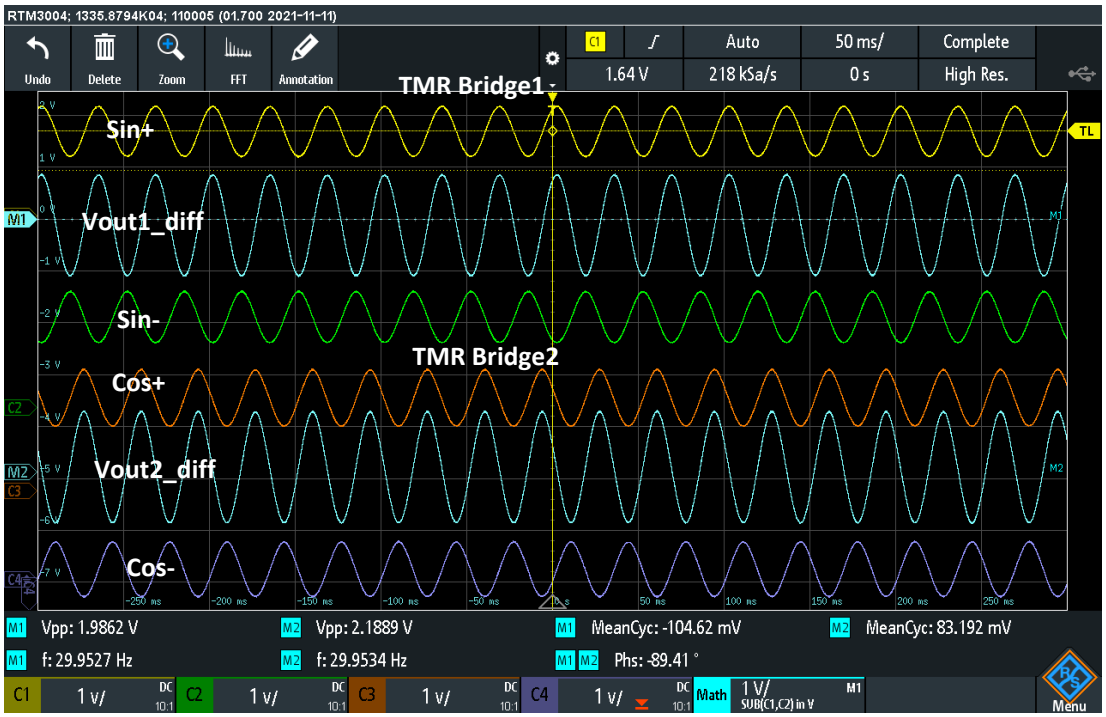

Figure 6.5: TMR sensor outputs at the in-amp gain of 4 and distance of 4 mm.

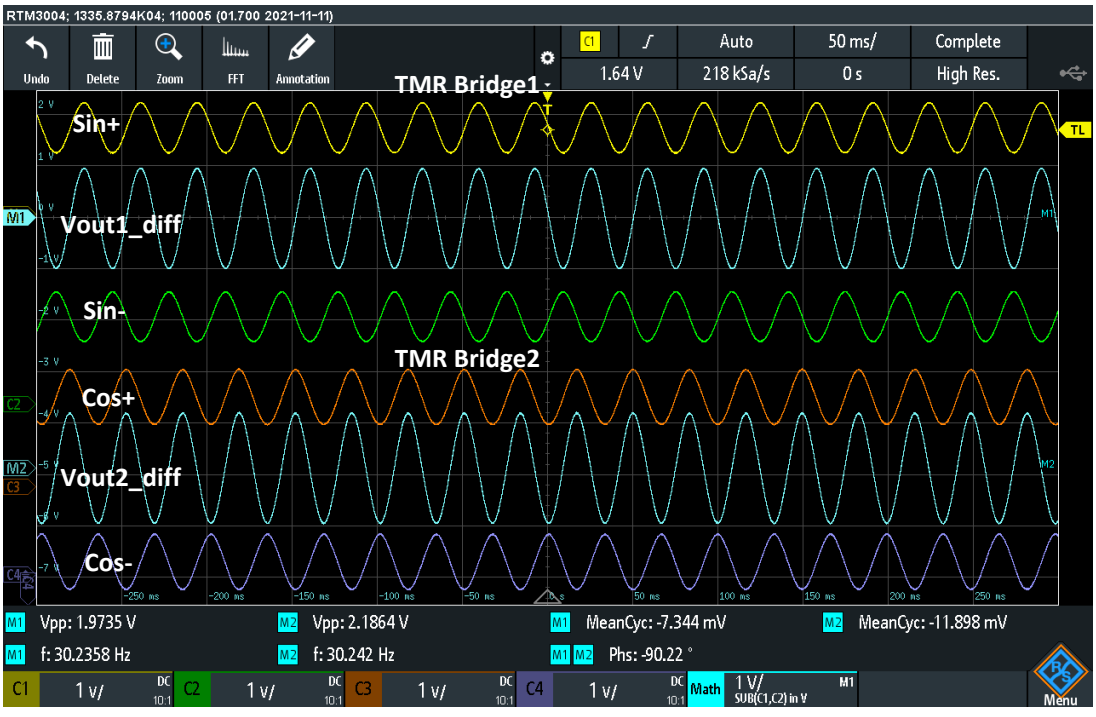

Figure 6.6: TMR sensor outputs at the in-amp gain of 4, distance of 4 mm and with offset autozeroing.

was implemented to counteract the amplified offset voltage, and the results, depicted in Figure 6.6, show a reduction in offset voltage to below 10 mV.

To further illustrate the impact of offset voltage, the sensor's distance from the motor

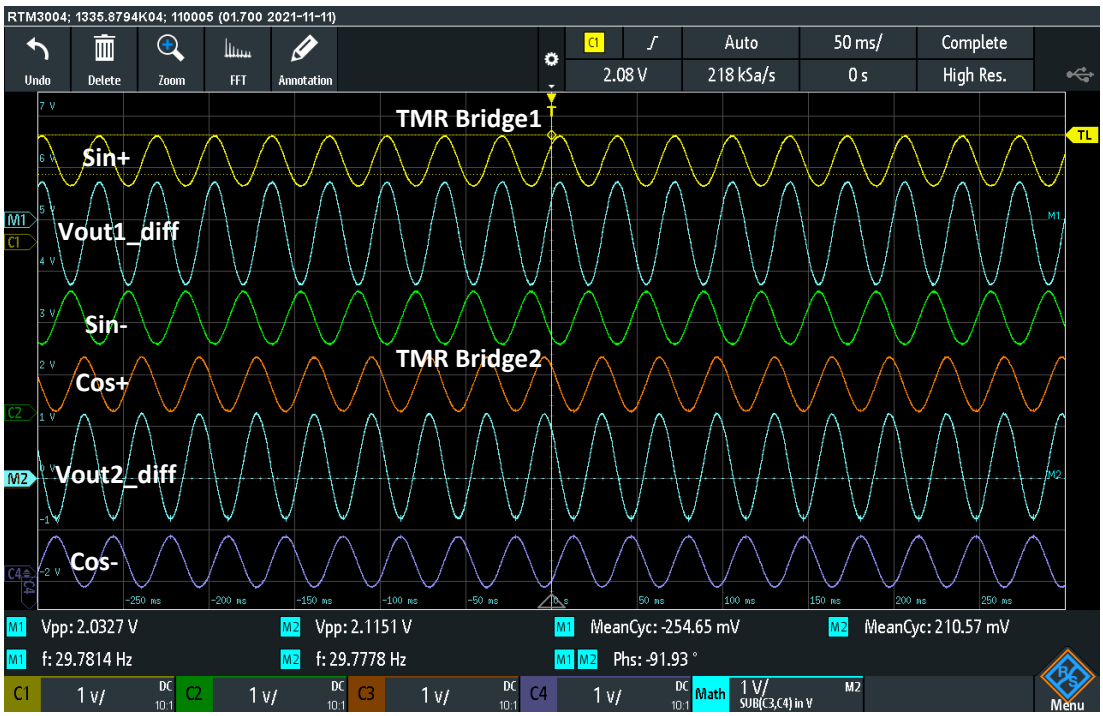

Figure 6.7: TMR sensor outputs at the in-amp gain of 32, distance of 11 mm.

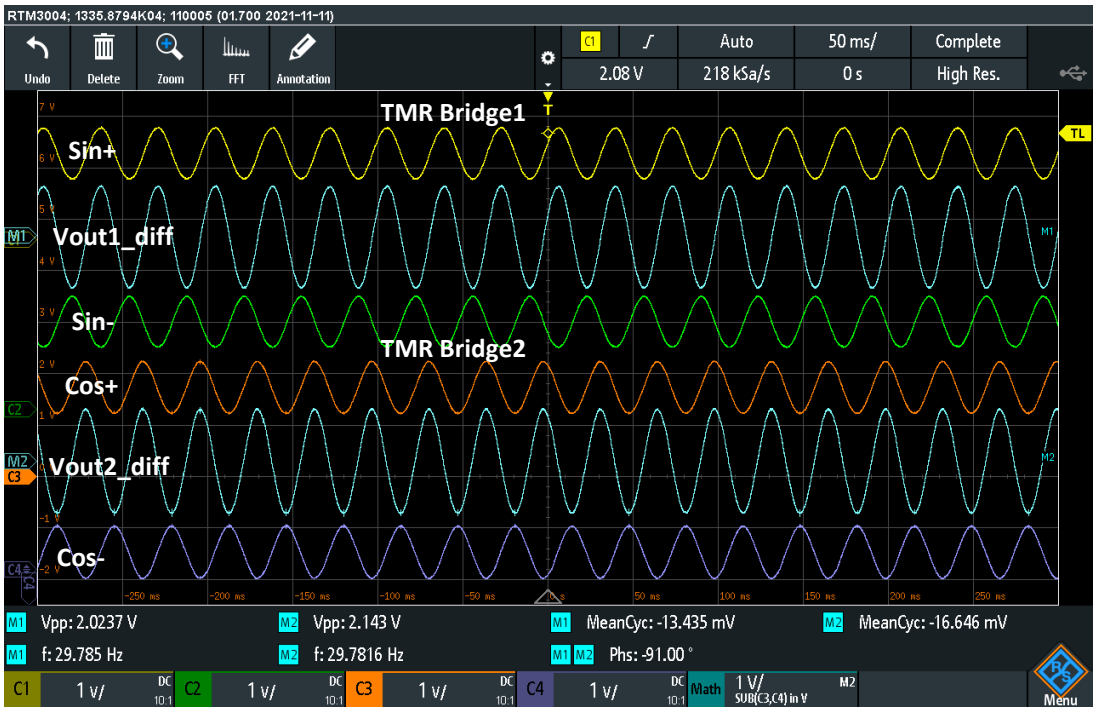

Figure 6.8: TMR sensor outputs at the in-amp gain of 32, distance of 11 mm and with offset autozeroing.

shaft was increased to 11 mm, necessitating an adjustment of the gain to 32. This setup revealed an offset voltage of approximately 250 mV, as shown in Figure 6.7. Following the application of the autozeroing scheme, the offset voltage was effectively reduced to

around 16 mV, as evidenced in Figure 6.8.

It is important to note that the offset voltage limits the resolution of readings by consuming the ADC's full-scale voltage capacity and significantly affects the accuracy of angle computation. This relationship is encapsulated in the following equation [179]:

$$\theta = \arctan\left(\frac{2A_{sin}\sin(\alpha+\varphi)+\text{offset}sin}{2Acos\cos(\alpha)+\text{offset}_{cos}}\right) \tag{6.1}$$

In this equation, θ represents the measured rotational angle, α is the magnet's rotational angle relative to the sensor, $2A_{\text{sin}}$ and $2A_{cos}$ denote the peak sine and cosine amplitudes, respectively, φ is the phase error between the sin and cos signals and offset sin and offset *cos* represent the respective offset errors in the sine and cosine amplitudes.

In summary, the sensor requirements and challenges have been evaluated in relation to the capabilities of the analog front end, including the CFIA and filter. The study successfully demonstrated that the tuning adjustments available are sufficient to manage perturbations effectively. This validation underscores the robustness of the design decisions made, ensuring that the sensor system can meet operational requirements across different conditions, leveraging the configuration insights derived from the optimization algorithm.

Chapter 7

Conclusions

This research aims to enhance the autonomy and optimization capabilities of smart sensory electronic systems (SSES) through the integration of artificial intelligence (AI) at the lowest levels of automated test equipment (ATE). By adopting a cost-effective approach, it has successfully demonstrated the potential of AI and machine learning to enable self-X properties in SSES for their in-field performance optimization.

To achieve this, the study implemented power-efficient chip performance optimization using low-cost indirect measurement methods, employing XFAB 0.35 μm CMOS technology. The comprehensive approach included developing electronic design automation (EDA) methodologies and extrinsic optimization techniques, seamlessly integrated into dedicated hardware for assessment and optimization. The optimization algorithm is implemented at the hardware level using Red Pitaya FPGA boards, which utilize DACs and ADCs to assess and acquire data from the analog front during the optimization process. The chip that serves as the hardware platform for intrinsic evolution is designed by another doctoral candidate within our research group [35]. This chip acts as a foundational component for achieving self-X properties and provides a robust architectural base for the in-field performance optimization approach presented in this research.

7.1 Key Findings

7.1.1 Goal 1: Cost-Effective Indirect Measurements for In-field Optimization

The research introduced a cost-effective and power-efficient approach for intrinsic performance optimization of the configurable current-feedback instrumentation amplifier (CFIA). Initial testing, conducted prior to the intrinsic optimization process based on post-layout simulations using the configuration obtained from extrinsic optimization, revealed degraded performance and unexpected instability within the CFIA circuit. Subsequently, the in-field optimization based on total harmonic distortion (THD) and power monitoring approaches successfully discovered the optimal configuration for the linear operation of the CFIA circuit using the optimization algorithm, highlighting the significant benefits of implementing sensory electronic circuits with self-X properties for yield optimization. The THD optimization approach proved effective in reducing the total number of assessment units required to optimize the performance of the CFIA or any other amplifier. This is primarily due to the statistical correlation of various performance characteristics of the amplifier on the measured THD value. Additionally, even non-stable circuit conditions correlated to lower THD values. To ensure stability, a pulse test is conducted at the end of the optimization process, making most of the optimization process conducted using a single sinusoidal signal stimulus an efficient method for improving amplifier performance.

The power monitoring technique assisted the optimization algorithm in identifying the power-efficient solution from the explored search space. This significantly improved the power efficiency of the solution, ultimately leading to prolonged device lifetime and better energy utilization. The CFIA is optimized for a 1 MHz signal frequency and a 2 $V_{p\text{-}p}$ dynamic input range. The achieved average optimized THD is equal to -72 dB, relative to signal stimuli with a THD of -74.49 dB. This optimization result achieved a 34% increase in power efficiency compared to the optimization process without the power monitoring module.

In the initial experiment, optimization is carried out under static conditions, specifically at room temperature. Then, in the next step, in-field dynamic optimization of sensory interface systems, specifically focusing on a fully differential CFIA, is conducted.

The intrinsic optimization is performed on-chip, with changes in temperature ranging from $-20°C$ to $40°C$, and by reducing the supply voltage by 25% from the nominal value of 3.3 volts. The practical evaluation demonstrates the capability to tackle all sources of variation, i.e., process, voltage, and temperature (PVT). The results show satisfactory THD measurements at various temperatures, with the measured THD being -71.93 dB at $25°C$, -69.95 dB at $-20°C$, and -74.01 dB at $40°C$.

7.1.2 Goal 2: Implementation of AI Agent

Given the complexity of search and objective spaces in smart sensory electronics, a novel experience replay particle swarm optimization (ERPSO) algorithm is developed to act as an AI agent for optimizing the CFIA. The ERPSO algorithm, embedded on Red Pitaya FPGA boards, facilitates autonomous extrinsic in-field optimization of the CFIA by expanding the selection process of the classical PSO with an experience replay buffer (ERB). The FPGA boards handle the serial data-transfer protocol for configuring the CFIA, generate test stimuli, acquire CFIA responses, calculate total harmonic distortion (THD) using FFT, determine the signal frequency for the power-monitoring module, implement the ERPSO algorithm, and transmit data to a server. This implementation enables the AI agent to autonomously search for and optimize the CFIA's performance for PVT variations directly in its operational environment.

7.1.3 Goal 3: Optimization in the Presence of Observer Imperfections

In the next step, the evaluation of robust optimization for CFIA using surrogate-based and archive-based robust optimization methodologies is conducted extrinsically, focusing solely on simulation-based results due to timing constraints. These robust optimizations demonstrate their capabilities through benchmark functions and direct application to the CFIA, focusing on optimizing THD and power consumption. The results from this optimization method indicate a successful reduction in average expected error (AEE) error and improvement in correlation metrics, which helps in the improvement of THD values, illustrating the method's proficiency in fine-tuning the CFIA to achieve desired performance levels while effectively managing uncertainties. Further experimental validation is needed to confirm these results in practical settings and ensure their applicability to diverse analog circuit designs.

7.1.4 Goal 4: Non-Intrusive Sensor-Based Low-Cost Measurements for Filter Performance Optimization

In the next phase, a comprehensive evaluation of a low-cost, non-intrusive sensor-based indirect measurement method is proposed for optimizing filter performance, specifically focusing on the cutoff frequencies for smart sensory electronics. The filter is a crucial component of the readout sensory electronics chain, and its optimization is vital for enhancing overall system performance. Due to timing constraints, the filter's performance verification is conducted intrinsically, while its performance optimization using non-intrusive sensors is performed extrinsically. Filter performance verification begins with a shadow register verification, ensuring the accuracy of configuration bit patterns for filter tuning. The filter is configured using data derived from post-layout extrinsic evaluation, setting its cut-off frequency to 2.6 MHz. The sinusoidal response of the filter, with an output phase shift of 179.49 degrees and maintaining unity gain within its passband, demonstrates a roll-off of less than -80 dB. This aligns with the post-layout simulation predictions, suggesting an effective filter order of less than four. Further, the study thoroughly evaluates the filter's dynamic performance under temperature variations, illustrating its robustness. The filter's ability to recalibrate, maintaining a maximum discrepancy of only 3% from intended cutoff frequencies post-adjustment, emphasizes its resilience and the efficacy of the optimization strategy. This recalibration is performed within the temperature range of -20°C to 40°C, highlighting the filter's operational stability across a dynamic environment.

To further enhance the filter optimization process, non-intrusive sensors for indirect measurement are integrated. These sensors provide a low-cost, effective way to correlate filter settings with sensor outputs, enabling the development of a regression model to estimate the filter's cutoff frequency indirectly. This model is crucial for navigating the non-linear relationship between the filter's bandwidth and sensor outputs.

Although the optimization is conducted extrinsically due to timing constraints, deviations caused by chip layout simulate the effects that might occur in fabricated chips. By addressing these layout-induced deviations through a reinforcement learning approach, the study demonstrates the adaptability and potential applicability of the optimization method to fabricated chips.

7.1.5 Goal 5: Generic and Easily Integrable Architectural Design

The practical application of a reconfigurable analog front-end with self-X properties for the TMR sensor, provided by Sensitec, specifically for angular encoding applications, demonstrates that the architecture is designed for seamless integration with higher system hierarchies. This generic architecture is adaptable to a wide range of sensors and applications, offering significant flexibility, with TMR being just one example.

In this study, the autonomous chip performance optimization process is initially achieved. However, when connected with the TMR sensor setup, the configuration bits derived from the optimization algorithm are used for the analog front end. The data acquisition from the TMR sensor is performed manually, and this acquired data being transferred to a higher hierarchical system for further processing.

Although the process was not entirely autonomous due to time constraints, the system's ability to generate and transfer data highlights its generic nature and ease of integration with upper-level systems. This approach underscores the integration of theoretical and algorithmic progress with practical implementation in sensory systems, demonstrating the architecture's flexibility.

7.2 Future Work

The research presented has laid a robust foundation for the optimization and enhancement of smart sensory electronic systems through the integration of AI and machine learning. However, several avenues remain unexplored and present exciting opportunities for future investigation. The following areas have been identified as key directions for extending the current work:

1. **Interleaved Measurement and Calibration Processes:** The exploration of uninterrupted optimization processes represents a promising avenue for future research. One potential strategy involves deploying a real-time operating system (RTOS) or a time-triggered embedded system (TTES) on the Red Pitaya board. This is particularly suitable for managing low-frequency sensor signals, such as those from a TMR sensor used to monitor a rotating shaft's speed. The integration of RTOS or TTES enables the simultaneous execution of calibration and measurement processes, effectively interleaving them to minimize disruptions. This

interleaving process includes phases such as 'Measurements', 'Transfer Configurations', 'THD Calculations', and 'Power Monitoring', demonstrating how the system manages to concurrently perform measurement and optimization tasks.

2. **ERPSO Algorithm Optimization:** Further refining the implementation of the ERPSO algorithm on Red Pitaya FPGA boards to enhance the efficiency and effectiveness of autonomous extrinsic in-field optimization of CFIA.

3. **Verification of Observer Uncertainty Intrinsically:** Experimentally validating the robust optimization methods for CFIA on hardware to confirm their effectiveness in managing uncertainties and ensuring their applicability to diverse analog circuit designs.

4. **Verification of Non-Intrusive Sensors on Hardware Level:** Intrinsically evaluating non-intrusive sensor-based indirect measurement techniques for smart sensory electronic systems. The non-intrusive nature of these sensors facilitates uninterrupted calibration of the measurement system, offering a pathway to enhance system continuity and efficiency. Additionally, the application and validation of reinforcement learning methods to address deviations between simulation predictions and actual chip performance will be explored. This approach has the potential to significantly reduce the need for extensive physical measurements, thus saving time and resources.

5. **Complete Autonomous Implementation of Analog Front End with TMR Sensor:** Achieving full autonomy in the implementation of the analog front end in conjunction with the TMR sensor, ensuring seamless data acquisition, processing, and integration with higher hierarchical systems.

By addressing these areas, future research can build on the foundational work presented in this study, advancing the capabilities and applications of smart sensory electronic systems.

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Appendix A

Configuration Patterns

Closed-loop gain (A_{CL})	**Temperature**	**Configuration Pattern (binary)**
1	24 °C	000100000000000110001111110101010000100001000011111111
	-20 °C	000100000000000111110110101001000010000100000100011100
	40 °C	000100000000000111010010110111000011001000000100011011 0
2	24 °C	001100000000000110001111110101010000100001000011111111
	-20 °C	001100000000000111110110101001000010000100000100011100
	40 °C	001100000000000110001111110101010000100001000011111111
4	24 °C	010100000000000110001111110101010000100001000011111111
	-20 °C	010100000000000111110110101001000010000100000100011100
	40 °C	010100000000000111010010110111000011001000000100011011 0
8	24 °C	011100000000000110001111110101010000100001000011111111
	-20 °C	011100000000000111110110101001000010000100000100011100
	40 °C	011100000000000111010010110111000011001000000100011011 0
16	24 °C	100100000000000110001111110101010000100001000011111111
	-20 °C	100100000000000111110110101001000010000100000100011100
	40 °C	100100000000000111010010110111000011001000000100011011 0
32	24 °C	101100000000000110001111110101010000100001000011111111
	-20 °C	101100000000000111110110101001000010000100000100011100
	40 °C	101100000000000111010010110111000011001000000100011011 0
64	24 °C	110100000000000110001111110101010000100001000011111111
	-20 °C	111100000000000111110110101001000010000100000100011100
	40 °C	110100000000000111010010110111000011001000000100011011 0
128	24 °C	111100000000000110001111110101010000100001000011111111
	-20 °C	111100000000000111110110101001000010000100000100011100
	40 °C	111100000000000111010010110111000011001000000100011011 0

Table A.1: CFIA best configuration patterns across different temperatures

Cutoff-frequency (f_c)	**Temperature**	**Configuration Pattern (binary)**
67 Hz	24 °C	0100010010000011111000000000001
	-20 °C	0100010010000011111000000000011
	40 °C	0100010010000011111000000000001
1 kHz	24 °C	0100010000000011111000000000001
	-20 °C	0100010000000011111000000000011
	40 °C	0100010010000011111000000011111
10 kHz	24 °C	0100010000000010001000000000001
	-20 °C	0100010000000010001000000000010
	40 °C	0100010000000010010000000000010
100 kHz	24 °C	0100010000010011100000110001
	-20 °C	0100010000010011100001101000
	40 °C	0100010000010011100000100111
1 MHz	24 °C	0100010001100011000001110001
	-20 °C	0100010001100011000010110001
	40 °C	0100010001100011000001100000
5 MHz	24 °C	0100010001110000011111000100
	-20 °C	0100010001110000010001110000
	40 °C	0100010001110000001001001111
10 MHz	24 °C	0100010001111110001111111111
	-20 °C	0100010001111110001111111111010
	40 °C	0100010001111110001111111111111

Table A.2: Filter best configuration patterns across different temperatures

Appendix B

Curriculum Vitae

Qummar Zaman

Education

- **PhD in Electrical Engineering**, RPTU, Kaiserslautern, Germany (2018 – 2025)
- **MSc in Electrical Engineering**, University of Engineering & Technology (UET), Taxila, Pakistan (2012 – 2014)
- **BS in Electronics Engineering**, International Islamic University, Islamabad, Pakistan (2008 – 2012)
- **Higher Secondary School Certificate (Pre-Engineering)**, FBISE, Pakistan (2006 – 2008)
- **Secondary School Certificate (Science)**, FBISE, Pakistan (2004 – 2006)

Areas of Interest

- Analog & Mixed-Signal IC Design
- Sensory System Development
- Smart Sensory Electronics

- Automatic Test Equipment for ICs
- Machine Learning and AI for Sensory Electronics

Research Publications (Selected)

1. Zaman, Q., & König, A. (2019). Self-x integrated sensor circuits immune to measurement noise in the presence of input perturbation by using robust optimization. *tm-Technisches Messen, 86(s1)*.

2. Zaman, Q., Alraho, S., & König, A. (2021). Efficient transient testing procedure using a novel experience replay particle swarm optimizer for THD-based robust design and optimization of self-X sensory electronics in Industry 4.0. *Journal of Sensors and Sensor Systems, 10(2)*, 193-206.

3. Zaman, Q., Alraho, S., & König, A. (2023). Low-Cost Indirect Measurements for Power-Efficient In-Field Optimization of Configurable Analog Front-Ends with Self-X Properties: A Hardware Implementation. *Chips 2.2*, 102-130.

4. Alraho, S., Zaman, Q., & König, A. (2023). In-field dynamic performance optimization of sensory readout electronics with Self-X properties using a low-cost and power-efficient indirect measurement method. *tm-Technisches Messen, 90(s1)*, 132-137.

5. Abd, H., Zaman, Q., Alraho, S., & König, A. (2024). Neuromorphic Spiking Sensory System with Self-X Capabilities. *IEEE Access*.