Contributions to the Design and Application of Integrated Multi-Sensor and Actuator Electronics with Self-X Properties for Robust Integrated Intelligent Systems

Beiträge zur Gestaltung und Anwendung von integrierten Multi-Sensor- und Aktuator-Elektroniksystemen mit Selbst-X-Eigenschaften für robuste integrierte intelligente Systeme

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Abstract

The swift progress in smart sensor technologies, Internet of Things, Industrial Internet of Things, and Cyber-Physical Systems has led to evolving the sensor standards to enable Industry 4.0, the industrial domain where adaptability, efficiency, and reliability are essential. The sensor applications of the new industry era necessitate increasingly adaptable sensor electronics and signal processing capabilities based on machine learning (ML) and artificial intelligence (AI) with other cutting-edge technologies.

This thesis presents a literature review of the design and applications of evolvable hardware and reconfigurable/programmable electronics that can be tailored for smart sensory electronics (SSEs) in Industry 4.0. Through an interdisciplinary approach that weaves together elements from bio-inspired systems, evolvable hardware, and advanced signal processing techniques, this work introduces a suite of design methodologies and implementations for analog front-end (AFEX) systems endowed with self-X capabilities, namely self-optimization, self-configuration, and self-calibration.

Central work to the AFEX is the circuit improvement and implementation of the fully-differential current-feedback instrumentation amplifier (CFIA) that demonstrates high performance in terms of input dynamic range, power efficiency, and adaptability and also integrates advanced features like input-offset voltage autozeroing.

A major limitation of hardware in-field optimization is the chip area due to the configurable elements and the assessment unit implementation; both together increase the cost and almost present the optimization approach as possible but not a practical or attractive industrial solution. In this work, the application of indirect measurement for devices under optimization is implemented using simple non-intrusive sensors (NISs) and THD-based power-efficient indirect measurement techniques. Several design metrics are extracted simultaneously in fewer tests that don't require the addition of new hardware, except for the utilization of the existing sensor's data acquisition resources. To reduce the chip cost, it is proposed to configure the sensitive elements only in the circuit.

In addition to the CFIA, the thesis proposes an innovative design of a fourth-order fully-differential anti-aliasing and anti-imaging filter, a crucial device for maintaining signal integrity for various signal processing properties ranging from low to high-frequency sensor applications. The key features of the proposed filter are the wide tunable band-

width range, fine-step frequency resolution per decade, and a high dynamic signal range approached by the application of a programmable and linearized MOS resistor. Furthermore, to account for the complexity of the bandwidth tuning, an indirect measurement approach based on SSIs is proposed with the help of AI and neural networks.

The practical realization of these designs is fabricated on a chip using the CMOS 0.35 µm technology from XFAB. The conducted LAB experiments under various operating conditions demonstrate not only the feasibility of the proposed solutions but also their potential to enhance the performance and energy efficiency, maximize yield, and improve the reliability of SSE in harsh industrial environments. Furthermore, by enabling sensors to autonomously adapt under varying conditions, it reduced the need for manual recalibration, thereby supporting the autonomous operation of industrial systems.

An experimental demonstration using a Tunnel Magnetoresistance (TMR) sensor in the last chapter, showcases the practical application and benefits of the proposed in-field optimization. This demonstration not only serves as a proof of concept but also illustrates the potential of the proposed design approach in real-world industrial scenarios.

Kurzfassung

Der rasche Fortschritt in den Bereichen intelligente Sensortechnologien, Internet der Dinge, industrielles Internet der Dinge und cyber-physische Systeme hat dazu geführt, dass die Sensorstandards weiterentwickelt wurden, um Industrie 4.0 zu ermöglichen, den industriellen Bereich, in dem Anpassungsfähigkeit, Effizienz und Zuverlässigkeit von entscheidender Bedeutung sind. Die Sensoranwendungen der neuen Industrieära erfordern zunehmend anpassungsfähige Sensorelektronik und Signalverarbeitungsfähigkeiten, die auf maschinellem Lernen (ML) und künstlicher Intelligenz (KI) sowie anderen Spitzentechnologien basieren.

In dieser Arbeit wird eine Literaturübersicht über das Design und die Anwendungen von evolvierbarer Hardware und rekonfigurierbarer/programmierbarer Elektronik vorgestellt, die für intelligente sensorische Elektronik (SSEs) in der Industrie 4.0 maßgeschneidert werden können. Durch einen interdisziplinären Ansatz, der Elemente aus bioinspirierten Systemen, evolvierbarer Hardware und fortschrittlichen Signalverarbeitungstechniken miteinander verwebt, stellt diese Arbeit eine Reihe von Designmethoden und Implementierungen für analoge Front-End-Systeme (AFEX) vor, die mit Self-X-Fähigkeiten ausgestattet sind, nämlich Selbstoptimierung, Selbstkonfiguration und Selbstkalibrierung.

Das Kernstück des AFEX ist die Schaltungsverbesserung und Implementierung des volldifferenziellen stromrückgekoppelten Instrumentenverstärkers (CFIA), der eine hohe Leistung in Bezug auf Eingangsdynamik, Leistungseffizienz und Anpassungsfähigkeit aufweist und auch fortschrittliche Funktionen wie die automatische Nullstellung der Eingangsoffsetspannung integriert.

Eine wesentliche Einschränkung der Hardware-Infield-Optimierung ist die Chipfläche aufgrund der konfigurierbaren Elemente und der Implementierung der Bewertungseinheit; beides zusammen erhöht die Kosten und macht den Optimierungsansatz zwar möglich, aber nicht zu einer praktischen oder attraktiven industriellen Lösung. In dieser Arbeit haben wir die Anwendung der indirekten Messung für zu optimierende Bauelemente unter Verwendung einfacher nicht-intrusiver Sensoren (NISs) und THD-basierter leistungseffizienter indirekter Messverfahren implementiert. Mehrere Designmetriken werden gleichzeitig in weniger Tests extrahiert, die keine neue Hardware erfordern, mit

Ausnahme der Nutzung der Datenerfassungsressourcen des vorhandenen Sensors. Um die Chipkosten zu senken, haben wir vorgeschlagen, die empfindlichen Elemente nur in der Schaltung zu konfigurieren.

Zusätzlich zum CFIA wird in dieser Arbeit ein innovatives Design eines volldifferentiellen Anti-Aliasing- und Anti-Imaging-Filters vierter Ordnung vorgeschlagen, das für die Aufrechterhaltung der Signalintegrität bei verschiedenen Signalverarbeitungseigenschaften von Nieder- bis Hochfrequenzsensoranwendungen von entscheidender Bedeutung ist. Die Hauptmerkmale des vorgeschlagenen Filters sind der große abstimmbare Bandbreitenbereich, die feinschrittige Frequenzauflösung pro Dekade und ein hoher dynamischer Signalbereich, der durch die Anwendung eines programmierbaren und linearisierten MOS-Widerstands erreicht wird. Um der Komplexität der Bandbreitenabstimmung Rechnung zu tragen, wird außerdem ein indirekter Messansatz auf der Grundlage von SSI mit Hilfe von KI und neuronalen Netzen vorgeschlagen.

Die praktische Umsetzung dieser Entwürfe wird auf einem Chip mit der CMOS 0,35 µm Technologie von XFAB hergestellt. Die durchgeführten LAB-Experimente unter verschiedenen Betriebsbedingungen zeigen nicht nur die Machbarkeit der vorgeschlagenen Lösungen, sondern auch ihr Potenzial, die Leistung und Energieeffizienz zu steigern, den Ertrag zu maximieren und die Zuverlässigkeit von SSE in rauen Industrieumgebungen zu verbessern. Durch die Möglichkeit der autonomen Anpassung der Sensoren an sich ändernde Bedingungen wird außerdem die Notwendigkeit einer manuellen Neukalibrierung verringert, wodurch der autonome Betrieb von Industriesystemen unterstützt wird.

Eine experimentelle Demonstration unter Verwendung eines Tunnelmagnetowiderstandssensors (TMR) im letzten Kapitel zeigt die praktische Anwendung und die Vorteile der vorgeschlagenen Feld-Optimierung. Diese Demonstration dient nicht nur als Konzeptnachweis, sondern veranschaulicht auch das Potenzial des vorgeschlagenen Designansatzes in realen industriellen Szenarien.

Erklärung

Hiermit versichere ich, dass ich die vorliegende Arbeit selbst angefertigt und verfasst habe und alle benutzen Hilfsmittel in der Arbeit angegeben habe.

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Senan Mahmood Aube Alraho

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List of Abbreviations

AAF Anti-Aliasing Filter

ADC Analog-to-Digital Converter

AFE Analog Front-End

AFEX Amplitude and Spike-Domain Analog Front-End Circuits with Self-X Properties

AI Artificial Intelligence

AMA Association for Sensors and Measurement

ANN Artificial Neural Network

ASIC Application-Specific Integrated Circuit

ATE Automatic Test Equipment

BGR Bandgap Reference

BIST Built-In Self-Test

CAB Configurable Analog Block

CFIA Current-Feedback Instrumentation Amplifier

CMOS Complementary Metal Oxide Semiconductor

CMRR Common-Mode Rejection Ratio

CPGA Ceramic Pin Grid Array

CPS Cyber-Physical Systems

CUT Circuit Under Test

DAC Digital-to-Analog Converter

DSS Digital Signal Synthesizer

DUT Device Under Test

EDA Electronic Design Automation

EEPROM Electrically Erasable Programmable Read-Only Memory

EHW Evolvable Hardware

EIS Electrical Impedance Spectroscopy

ERPSO Experience Replay Particle Swarm Optimization

FB-DDF Fully-Balanced Differential-Difference Amplifier

FFT Fast Fourier Transform

FPAA Field Programmable Analog Array

FPGA Field-Programmable Gate Array

FPMA Field Programmable Medium-granular Mixed-signal Array

FPTA Field Programmable Transistor Array

GA Genetic Algorithm

GBW Gain-Bandwidth Product

GND Ground

GOPA Generic Operational Amplifier

ICMR Input Common-Mode Voltage Range

IoT Internet of Things

JPL Jet Propulsion Laboratory

LAB Laboratory

LNA Low-Noise Amplifier

LPF Low-Pass Filter

MC Monte Carlo

ML Machine Learning

MOS Metal-Oxide Semiconductor

MOSFET-C Metal-Oxide-Semiconductor Field-Effect Transistor Capacitor

MPC Multi-Project Chip

MSB Most Significant Bit

MSO Mixed-Signal Oscilloscope

NAMUR User Association of Automation Technology in Process Industries

NIS Non-Intrusive Sensors

OTP One-Time Programmable

PANDA Programmable ANalog Device Array

PCB Printed Circuit Board

PGA Programmable Gain Amplifier

PLL Phase-Locked Loop

PMM Power Monitoring Module

PMU Power Management Unit

PPAC Power, Performance, Area, and Cost

PSRR Power Supply Rejection Ratio

PVT Process-Voltage-Temperature

Q Quality Factor

RAA Reconfigurable Analog Array

RDK Rapid Development Kit

RH Reconfigurable Hardware

SC Switched-Capacitor

SIPO Serial-In Parallel-Out

SiP System-in-Package

SoC System-on-Chip

SPI Serial Peripheral Interface

SR Slew Rate

SSE Smart Sensory Electronics

SRAA Self-Reconfigurable Analog Array

THD Total Harmonic Distortion

TMR Tunnel Magneto-Resistance

TSC Temperature-Sensing Core

USIX Universal Sensor Interface with Self-X Properties

VBE Base-Emitter Voltage

VCM Common-Mode Voltage

VDD Supply Voltage

Chapter 1

Introduction

1.1 Sensor Electronics for Industry 4.0

Continuous and rapid advancements in micro/nano heterogeneous integration and packaging technologies, including Systems-on-Chip (SoC) and System-in-Package (SiP) [1,2], have driven significant progress in integrated computing systems. Simultaneously, the emergence of innovative sensory concepts and new standards or reference elements based on emerging quantum technologies, such as NIST-on-a-Chip [3, 4] has enabled the development of systems that are becoming increasingly sophisticated, accurate, reliable, and cost-effective. Coupled with advanced information processing technology, commonly known as Artificial Intelligence (AI), has enabled the development of intelligent systems for a broad range of applications, including the Internet of Things (IoT), industrial IoT (I(I)oT), and Cyber-Physical Systems (CPS).

The convergence of machine learning (ML) and AI with other cutting-edge technologies, including cloud computing, big data analytics, CPS, and (I(I)oTs), drive the fourth industrial revolution (Industry 4.0) [5–8] and current applications in automation [9], autonomous driving [10], wearable electronics, and healthcare assistance systems [11]. The constant evolution of technology, especially in the context of industrial transformation, primarily relies on acquiring, analyzing, and interpreting data from smart sensors and I(I)oT devices [12]. As a result, it is essential to develop accurate, flexible, and long-term dependable sensory electronics [13,14], that can efficiently collect, process, and transmit data to the central processing unit [15].

The signal interface chain of a typical smart sensor is shown in Figure 1.1 [16–21].

The analog front-end interfaces the analog sensor with the analog-to-digital converter (ADC). This interface performs two essential roles: signal conditioning for the sensor and anti-aliasing filtering.

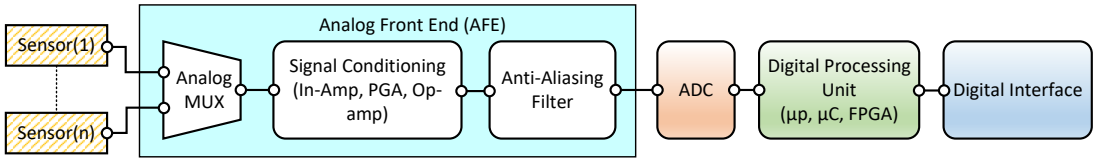

Figure 1.1: Block diagram of the typical smart sensor signal interface chain.

Sensor signal conditioning incorporates various functions, including buffering, common-mode voltage level shifting, and amplification. The instrumentation amplifier (in-amp), owing to its excellent ability to interface sensor signals from noisy environments, is the preferred device for signal conditioning [22].

The small sensor signal level may undergo further amplification via an additional gain stage following the in-amp. This stage utilizes programmable gain amplifiers (PGAs) based on operational amplifier (op-amp) circuits that align the signal with the full-scale voltage of the ADC. The anti-aliasing filter reduces the signal noise to the level required for the ADC resolution. Further amplification can be achieved if an active filter is employed. Moreover, the fully-differential active filter can serve as an ADC driver for handling its high input stage load and aligning the filtered signal to the common-mode voltage of the ADC.

The ADC unit converts the conditioned analog signal into a digital domain and interfaces it with the digital processing unit, such as a microcontroller (µC) in its simplest form. This digital processing unit further processes the captured sensor signal, performing tasks such as offset correction, linearization, digital filtering, and introducing user programmability to the entire chain and the peripheral interface. Although not depicted in the figure, a power unit exists to supply energy to all blocks and provide reference voltages and currents. It can also deliver the excitation signal to the sensor unit (either voltage or current). A power management unit (PMU) is also necessary to safely and efficiently power the entire sensor chain, especially when power resources are limited, as with energy harvesters [23, 24].

The sensor output is susceptible to various error sources originating from the interface electronics, beginning at the amplifier stage. These include the input offset,

gain, and nonlinearity errors. These errors supplement the offset and nonlinearity errors inherent to the sensor element. The deviations observed in the sensor conditioning are typically attributed to mismatches between the devices and components within the integrated circuit (IC). Under circumstances where a high gain is required to process low output sensor signals, these errors represent a potential risk of being significantly amplified [25]. Nonetheless, the performance and long-term reliability of smart sensory electronics (SSEs) face continuous challenges due to static and dynamic variations, including irreversible dynamic effects owing to aging effect [26].

Static aberrations, especially in advanced-node complementary metal oxide semiconductors (CMOS), arise from both local (random/stochastic) and global (systematic) mismatches between chip devices. The primary origins of these discrepancies can be traced back to several manufacturing process imperfections. These include the limitation in lithography resolution that leads to discrepancies in the actual device size, the effect of the gate oxide thickness profile on the threshold voltage of transistors, variations due to the doping gradient, and differences in carriers' mobility, among others [27, 28]. Furthermore, the mechanical stress inflicted on the chip during the die molding process prompted by the packaging and assembly phases of the ICs exacerbates static discrepancies [29, 30].

Dynamic variations, in particular the reversible type, arise from environmental fluctuations and alterations in the power supply voltage, in addition to the thermal drift caused by the self-heating and temperature gradient owing to the non-uniform power dissipation distribution in the ICs [31], which is more pronounced in densely packed transistors in advanced node technology and SoCs [32]. Both reversible dynamic and static process variations are well-modelled by foundry process design kits (PDK). Hence, it can be predicted by simulating the circuit with electronic design automation (EDA) tools across various process corners and altering the voltage and temperature, a concept known as process-voltage-temperature (PVT) verification. However, the aging effect due to the progressive deterioration of device characteristics over time on the circuit performance and long-term reliability is still challenging in accurately modelling and predicting the circuit performance during the design and simulation [33–35]. However, assessing the aging effect remains indispensable when implementing robust and reliable circuits intended for critical applications under actual operating conditions across the

IC lifecycle [36].

Several techniques can be used to address these issues in the early design phase and later in the product lifecycle using dynamic calibration approaches. Post-layout simulation by nesting the voltage and temperature corners over the process gradients using Monte Carlo (MC) simulation is the most convenient approach in the design phase for investigating the impact of local and global process variations as well as the effect of the interconnection parasitic elements on the yield of the circuit parameters.

Layout matching techniques [37–39], including common centroid or interdigitized configurations, along with the integration of dummy elements, significantly improve device matching properties for mitigating process variations as well as the packaging stress effect and become indispensable in analog layout design. Generally, larger devices are less susceptible to lithography tolerances and can offer enhanced matching performance in terms of the cost of chip area [28]. The geometry of the interconnections must be appropriately dimensioned to correspond with the current density of the connecting layer to prevent electromigration, which can potentially compromise the device reliability [40].

During the design phase, efficient design automation activities, encompassing circuit and layout synthesis, can be carried out to automate or optimize circuit performance. Examples of these tools include MUNEDA's WiCkeD [41, 42], and ABSYNTH [43]. These optimizations aim to extrinsically explore robust solutions for circuit element sizing that improve the circuit's performance yield across PVT variations while considering both the power consumption and design area. In other words, the optimization aim is to center the circuit design to achieve the highest manufacturing yield under actual operating conditions while addressing the essential IC design metrics namely power consumption, performance, area, and cost, collectively known as PPAC [44]. Moreover, recently developed IC EDA platforms offer built-in optimization tools. For example, the Cadence Virtuoso suite provides sensitivity analyses that can identify the most critical elements within the circuit and their impact on each design specification. Subsequently, these elements can be optimized using various possibilities available within the software to improve the yield. However, the automatic synthesis of analog IC layout remains a challenge [45], with a lack of maturity compared to digital counterparts [46–48], limiting industry acceptance [49]. Despite its time-consuming nature, manual layout design is still favored in analog circuits [50–52], with partial automation being feasible within

user-predefined constraints. Also, optimizing the design based on the worst-case process corner derived from worst-case simulations or statistical corners from Monte Carlo simulations may not accurately represent the real-world fabrication outcomes. Therefore, a generic design covering all possible corners will oversize the circuit or reduce the power efficiency. For instance, accounting for the worst-case speed corner in the design necessitates an increase in circuit power, which, if the fabricated chip is already at the worst-case power corner, would further exacerbate the power consumption.

In addition, matching techniques are only applied to paired devices of the same type, such as differential-pair transistors, current mirrors, and divider networks. Hence, it can not mitigate the absolute deviation of individual elements. Consequently, considering a simplistic first-order RC integrator or relaxation oscillator with a 20% variation in both the resistor and capacitor feedback yields a cumulative 40% shift in the cutoff or oscillation frequency, which is expected after fabrication. Nonetheless, inherent matching errors constrain the ability to achieve precise matching for large arrays of components [53].

State-of-the-art trimming approaches can be followed at the wafer level or after die packaging to readjust the circuit elements or compensate for mismatches. Laser trimming and Zener zapping are well-established traditional techniques for precisely and permanently adjusting resistor values in integrated circuits at the wafer level (IC) [54]. However, the cost and availability of these techniques for the specific CMOS technology should be considered [55]. Furthermore, wafer-level trimming approaches generally cannot address the shifts induced by the assembly and packaging process.

Fuse trim links [56] and electrically programmable fuses [57, 58] provide one-time programmable fuses as post-packaging trimming alternatives, thereby eliminating the necessity for wafer-level testing at the cost of extra pads or pins. In contrast to the DigiTrim innovation [59], patented by Analog Devices which offers a one-time programmable fuses procedure with no extra pads by utilizing the same input pins of the operational amplifier (op-amp) for programming the fuses to trim the offset voltage. An often-utilized trimming technique in the industry involves preserving the trimming vector of the circuit element network through one-time programmable memory (OTP) [60]. Following execution at either the wafer or packaging stage, the trimming data are permanently stored. However, one-time trimming approaches cannot adapt to dynamic variations,

particularly the aging effect. Alternatively, using EEPROM memory cells (EEcells) paves the way for trim fuses to be repeatedly reprogrammed, thereby enabling multiple programming cycles [61, 62]. Analog Devices also present a similar approach based on the EEPROM [59] by using current or voltage DACs to adjust the current or voltage nodes in the IC with the possibility of reprogrammability and requiring at least one extra pin. This technique is compatible with CMOS technology and does not require special fabrication processes.

The presented procedures are static, slow, and expensive [63]. Therefore, on-chip dynamic/automatic calibration methods have been developed to address static and dynamic deviations in SSEs using compensation techniques during the operational phase. These approaches include conventional techniques such as autozeroing [64] and chopping [65] to correct the op-amp offset and noise, as well as dynamic element matching (DEM) using built-in digital polynomial fitting or deterministic algorithms to calibrate the linear characteristics and noise performance of data converters [66, 67]. More advanced dynamic approaches, including design-for-testability methods, have been introduced to support self-diagnostics and autocorrection in analog circuits [68]. Notably, self-calibration techniques have been established in the field of ADCs [69, 70]. In terms of DC accuracy, the TMS320280x ADC chip family from Texas Instruments provides a software calibration driver [71] that supports the gain and offset error calibration. Gain calibration involves determining the necessary gain coefficient for the integrated PGA on the ADC chip to match the sensor output signal to the full-scale voltage of the ADC [72].

1.2 Self-X Sensory Electronics

In the landscape of everyday objects, highly integrated sensor systems have become a standard feature. However, this scenario differs dramatically when rough industrial environments are considered. The implementation of sensor systems is often hindered by extreme ambient conditions, such as high operating temperatures or humid and chemically aggressive environments. These conditions challenge the reliable operation of sensitive electronic components, rendering standard electronics or process technology and packaging impractical for use [16, 73]. The need for robust and reliable electronics is critical in applications exposed to harsher or noisier environments, such as space technology. Here,

extreme temperature and radiation can significantly degrade circuit characteristics. This emphasizes the necessity for electronics that can endure and function effectively under such demanding circumstances [74–76].

Furthermore, with the advent of Industry 4.0, the need for adaptable systems that can swiftly respond to evolving requirements is paramount for manufacturers. Consequently, electronic systems no longer depend on fixed designs for mass-produced products and have predictable demand. This necessity has shifted towards flexible systems that can be efficiently reconfigured with minimal operational disruption, and capital spending [77].

Recent on-chip dynamic approaches are based on organic computing [78] and evolutionary electronics [79]. Evolvable hardware (EHW) refers to configurable electronic hardware (RH) that can be self-configured using bio-inspired optimization algorithms that run on the evolutionary processing unit (EP) [80]. This approach can be accomplished by employing configurable elements of the circuit and system performance evaluation setup [18, 81–83]. The configurable elements act as design tuning knobs that can be periodically calibrated to restore and regulate the circuit performance, thereby facilitating the adaptation of the design throughout the product life cycle.

Intrinsic optimization [84] finds the optimal configuration pattern during the run time and supports the system with lifelike features based on so-called self-X or self-* attributes (self-calibration, self-adaptive, self-optimization, self-monitoring, self-healing, self-trimming, self-check, self-diagnosis, self-reconfiguration) [85–90] utilizing ML and AI techniques, such as metaheuristic optimization algorithms [91,92]. Hence, the system can adapt to and compensate for static and dynamic (reversible and aging) anomalies or damages that may occur during the electronics service time. The block diagram of the sensory electronics with self-X features is depicted in Figure 1.2, where the assessment unit evaluates the system performance based on the optimization solutions by providing the signals stimuli and measuring the output response under the control of the optimization unit.

The self-X approach offers significant advantages by replacing the need for costly and time-consuming one-by-one discrete calibration of systems. Instead, the self-X solutions can leverage built-in redundancy, reconfiguration, and correction features that utilize learning or optimization techniques at different levels of abstraction. Industry 4.0 highlights the value of self-X properties in automation technology [85], with these

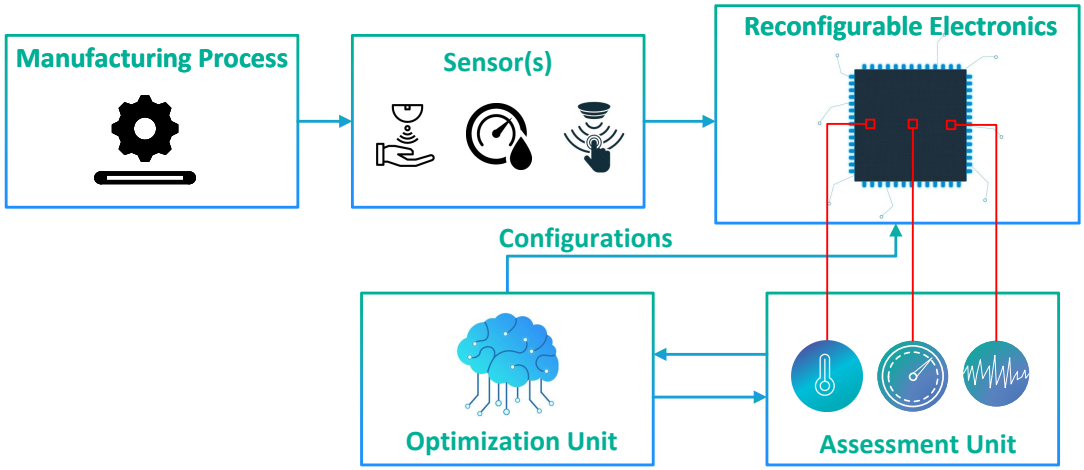

Figure 1.2: Block diagram of the sensory electronics with self-X properties.

features serving as new design principles for efficient and autonomous manufacturing process control [93]. Furthermore, the technology and sensor trend roadmaps published by the Association for Sensors and Measurement (AMA) and the User Association of Automation Technology in Process Industries (NAMUR) have both emphasized the significance of incorporating sensory electronics imbued with self-X properties [13,94]. This integration is vital for ensuring reliability, robustness, and a high degree of flexibility in various applications, particularly in the challenging conditions of Industry 4.0 and other applications in harsh environments [80]. Furthermore, they play a pivotal role in facilitating enhanced control and coordination across the entire product chain [15].

The consistent advancements in CMOS node technology, in line with the 'More Moore' extension, as delineated by The 2015 International Technology Roadmap for Semiconductors (ITRS) [2] and the 2021 Edition of the International Roadmap for Devices and Systems (IRDS™) [95], contribute substantially to the enhancement of PPAC metrics in digital systems. However, analog and mixed-signal circuits, particularly those interfacing with sensor signals [13], often lag in adopting the latest node due to several technical difficulties [96–99]. Analog circuits do not scale down as automatically as digital circuits because their component sizes are governed by specific circuit parameters such as noise, amplification, and bandwidth. Furthermore, achieving satisfactory device matching necessitates larger devices to minimize the influence of process systematic and random errors, a challenge that escalates with the advent of smaller node technologies [100]. Consequently, the area required for analog circuits does not automatically shrink in proportion to the reduced structural dimensions.

As the supply voltage reduces and the threshold voltage fails to decrease at a parallel rate, conventional analog circuit topologies become impractical. This discrepancy also results in a diminished signal dynamic range of the AFE, in contrast to the trends in sensor technology where dynamic ranges are typically increasing. Techniques for compensating the short-channel effect, such as cascoded mirrors for improving circuit matching or boosting the intrinsic gain, may be unfeasible because of limited voltage headroom. In addition, the decrease in the channel length increases the leakage current, which affects the MOS-switch performance. A noteworthy consideration is the necessity for mature modelling to facilitate circuit design and simulation [101], a task that is becoming increasingly intricate because quantum mechanical effects may govern charge transport [102]. Therefore, the industry continues to find value in the 180 nm and 350 nm CMOS nodes technology for implementing analog and mixed-signal sensory electronics [13, 103] owing to their mature process and modelling capabilities. These nodes present a balanced compromise in terms of density, switching speed, power loss, supply voltage, and fabrication costs. To address the issues of modelling accuracy and mismatch effects, the self-X concept can be employed for in-field design performance corrections.

On the other hand, the complexity, cost, and time required for measuring various metrics in the performance evaluation setup are crucial factors for implementing Self-* properties in SSEs [81, 82, 104], whereas in-field optimization [105] requires an on-chip assessment unit, commonly referred to as a built-in self-test unit (BIST) [82, 83, 106]. Two distinct categories of on-chip measurement setups can be classified based on the evaluation criteria for the target performance parameters. The direct performance measurement approach provides heightened accuracy and precision with a trade-off between augmented design complexity and chip area [83]. Conversely, the indirect measurement (IM) method relies on the statistical correlation between various performance characteristics, facilitating the concurrent estimation of multiple system performance parameters through simple test stimuli [82, 83, 107–109].

An alternate cost-effective indirect measurement strategy utilizing non-invasive sensors is highlighted by the authors in [104]. The sensor is electrically isolated from the main circuit and designed such that its operating conditions are strongly correlated with the ICs' characteristics. Hence, the primary circuit characteristics can be reasonably es-

timated and economically measured using multiple non-intrusive sensors, which are best when they have different sensitivities to the main circuit characteristics. However, it is challenging to analytically approximate the performance predictor. Hence, an artificial neural network (ANN) is typically employed as a regressor to approximate the regression task. Nonetheless, the generation and collection of data required for the training phase of the ANN is a considerable challenge. The complexity of this task escalates exponentially in parallel with the complexity of the design under optimization.

1.3 Motivation to this Work

State-of-the-art EHW structures, designed to fabricate high-yield circuits or provide robust and flexible SSEs for Industry 4.0, call for several points of consideration. Reconfigurability is facilitated by the design of a scalable device array within the circuit, which presents the following challenges:

1. A large die area, necessitated by scalable devices and switch selectors, augments fabrication costs and restricts the chip functionality.
2. Requirement for extensive on-chip configuration memory.
3. The overuse of switching resources can impede design performance by introducing additional parasitics to the circuit nodes, particularly when the switches are positioned along the analog signal path.
4. Optimization time.

BIST techniques have been successfully employed in digital systems for decades [110] to avoid the cost and complexity of using automatic test equipment (ATE). However, their implementation in analog and mixed-signal systems poses significant challenges [67]. This is primarily because assessing analog performance and generating the required signal stimuli entails a complex setup.

The third challenge pertains to the optimization procedure for analog components within sensory electronics. Unlike digital EHW, such as Field Programmable Gate Arrays, configuring analog EHW may lead to detrimental outcomes, potentially resulting in circuit failure or diminished long-term reliability. These effects are typically contingent

on the resulting current and current-density limitations of the physical interconnections. Conversely, the power efficiency of analog circuits is a crucial aspect of PPAC metrics, particularly when considering sensor nodes supplied by limited power resources.

1.4 Thesis Goals

The primary goal of this thesis is to tackle the challenges encountered in the realm of in-field chip performance optimization and analog EHW. This research strives to contribute to the evolution of a highly efficient and robust sensor interface analog front-end with self-X features that are practically compatible with Industry 4.0, harsh operating environment, comply with the sensors technology roadmap specifications delineated in AMA vision [13] and NAMUR [94], and cope with the reliability demand outlined by the ongoing project of Intelligent Reliability 4.0 [111]. The self-X system comprises both hardware and software components. This thesis predominantly focuses on the hardware aspect, whereas the software part, including its physical implementation in the EP unit, is being addressed in cooperation with another Ph.D. candidate working on the same project [112]. Within this scope, this thesis aims to concentrate on the following objectives:

- Conceiving and designing key components for a universal sensor interface with self-X properties (USIX 4.0) for industry 4.0.
- Minimize the chip area of the configurable SSE while preserving its flexibility. This necessitates the development of a method that selectively applies reconfigurability to the critical elements within the circuit. These elements significantly influence the SSE performance. Furthermore, it requires less configuration memory and shorter optimization duration owing to the reduced search space complexity of the optimization algorithm.
- Develop a reliable and power-efficient optimization method for reconfigurable analog circuits. This involves the creation of a simple power monitoring module that can enhance the circuit efficiency and improve the long-term reliability of the devices.
- Design fast and wide input signal range sensor signal conditioning circuits to ac-

commodate the advancements in the output dynamic range of the sensor in the amplitude domain. To keep pace with the progression of the supply voltage in CMOS technology, it is necessary to adhere to fully differential circuits. This includes the design of a fully-differential current-feedback instrumentation amplifier and a wide tunable range fully-differential active filter. The use of fully-differential characteristics further enhances linearity when processing high input signals.

- Simplify the complexity of the assessment unit to facilitate the self-X evaluation process through a simple and low-cost performance evaluation setup that can be used for chip in-field optimization. This thesis explores two types of indirect measurements. The first involves predicting various circuit features using a limited number of simple measurements. The second type involves a non-intrusive approximation of the circuit performance using on-chip PVT monitors with the assistance of artificial intelligence. Furthermore, reducing/eliminating the vulnerability of the assessment unit, particularly the observer uncertainty in terms of the circuit and optimization algorithm, shall be addressed.
- Run the optimized design into physical cells and chip fabrication.
- Intrinsic optimization to practically prove the validity of the proposed concepts.

1.5 Thesis Structure

The remainder of the thesis is organized as follows: Chapter 2 offers a literature review on configurable/evolvable electronic circuits. Chapter 3 details the design of the proposed fully-differential instrumentation amplifier, the design of the fully-differential and tunable active filter in conjunction with the design of the non-intrusive sensors, and the completion of the chip design with initial tests. Chapter 4 presents the practical results of intrinsic optimization of the fabricated instrumentation amplifier and filter. The demonstration of the proposed sensor interface with the TMR sensor is provided in Chapter 5. Finally, Chapter 6 concludes this thesis and suggests ideas for potential extensions of this research in the future.

Chapter 2

State of the Art of Evolvable Hardware

2.1 Literature Survey on Bio-Inspired Evolvable Hardware

The foundational concept of Evolvable Hardware (EHW) was initially proposed and identified as Darwin Machines by Hugo de Garis [113, 114] at the beginning of the 1990s. This new design methodology leverages Genetic Programming (GP), employing the Genetic Algorithm (GA) [115] to evolve and grow complex electronic systems that are too complicated to analyze readily or humanly designable. As a practical illustration of this methodology, the authors extrinsically evolved the weights and signs of self-connected Neural Network modules, which perform time-(in) dependent functions for the artificial nervous system. In the given context, the term "extrinsic" is used to indicate that the evolution of the circuit or system module takes place in a simulated environment. On the other hand, "intrinsic" refers to the actual evolution occurring within real hardware, regardless of whether the optimization unit running the algorithm is executed on a host computer, DSP, FPGA, ASIC or integrated on the evolvable chip itself [116].

The advent of electrically erasable programmable logic gate arrays (PLAs) has paved the way for the practical realization of autonomous artificial hardware. As a result, the year 1993 marked a significant milestone with the earliest hardware-based realization of Darwin Machines, which also represented the inception of what is now known as evolvable hardware as reported by the authors in [79]. The GA run on the computer

unit was used on GAL16Z8, a PLA commercial chip from Lattice Semiconductor Inc., was used to intrinsically evolve the system logic architecture and interconnections to achieve the desired performance adapted to environmental changes or hardware faults in real-time operation. The authors developed a basic combinational logic circuit of a 4-to-1 multiplexer using 108-bit strings, also called configuration or architecture bits. Subsequently, the first digital evolvable hardware realization using Field Programmable Gate Array (FPGA) was reported by Thompson in [117, 118], employing the XC6216 FPGA chip from Xilinx. The tentative experiment involved the evolution of a circuit capable of differentiating between two square tone inputs of 1kHz and 10kHz. The GA running on the host computer is used to evolve the FPGA architecture with 1800 configuration bits.

Inspired by the GP and EHW concept presented in the digital domain, authors in [119,120] evolved extrinsically various analog cells, including filters, amplifiers, voltage reference circuits, and more. This led to unique circuit topologies, but on-chip intrinsic evolution was not feasible; instead, the obtained solutions were manufactured and the post-fabrication outcomes waited.

The efficacy of FPGA in fast digital circuit prototyping motivated the researchers in [121] to propose and fabricate the first Field Programmable Analog Array (FPAA) as an analog counterpart to the FPGA. Using 1.3 µm CMOS technology, the FPAA comprises homogeneous Configurable Analog Blocks (CABs) connected through a user programmable network. The configuration bits loaded into an integrated shift register memory dictate the interconnections and specific analog functions executed within each CAB. Macromodels for operations such as addition, threshold operation, and signal multiplication facilitate the simulation of various neural network functions, enabling the realization of diverse neural network topologies.

Researchers from the University of Toronto created two Field-Programmable Analog Arrays (FPAAs) [122]. The first FPAA [123] consisted of fully-differential continuous time (CT) CMOS transconductor-based CABs designed for audio-range signal processing. Each CAB has a transconductance and adjustable feedback capacitors, and can act as a comparator when the compensation capacitor is disabled. The transconductor in this design serves as a flexible network element, functioning as a switch or a programmable resistor. The second FPAA [124] uses the second-generation current con-

veyor (CCII) with customizable resistors and capacitors optimized for video frequency range applications.

In 1995, IMP Inc. launched EPAC 50E10, a commercial FPAA-like product for discrete-time (DT) designs, utilizing the 1.2 analog EECMOS process and switched-capacitor (SC) technology [125]. The device includes an analog input multiplexer, programmable amplifiers, routing bus, and input/output modules. It enables real-time reconfiguration via a 200-bit string, is tailored for low-power, multi-channel signal conditioning, and operates without external parts, providing a 125 kHz analog bandwidth, corresponding to a 1 MHz clock frequency for SC operation.

Zetex Inc., now part of Diodes Inc., introduced the Totally Reconfigurable Analog Circuit (TRAC20), the first universal FPAA, operating up to 4MHz and using continuous time bipolar technology [126]. TRAC20 consists of 20 CABs arranged in two rows of ten. Topological programming is achieved by deactivating CABs and wiring pins externally, with a deactivated CAB disconnecting its inputs and output to serve as the next CAB input. The gain is adjusted using off-chip resistors, while a 60-bit string configures the CABs. The TRAC20 is integrated with a computer-aided design (CAD) tool for configuration and pre-implementation circuit simulation. It can generate a variety of analog circuits, including filters, programmable gain amplifiers (PGAs), voltage-controlled oscillators (VCOs), and phase-locked loops (PLLs), among others. This makes TRAC20 a versatile platform for implementing sensor readout circuitry.

Motorola Inc., introduced MPAA020, a CMOS SC FPAA design, in 1997 [127, 128]. Composed of a homogenous array of identical CABs arranged in four rows, the design can be programmed using 619-bit string. Each CAB, which can execute first-order filtering functions, can connect to immediate or distant neighbours through 'local' or 'global bus' inputs and outputs, enabling programmability of cell functionality and interconnections. This flexibility allows the implementation of a wide range of analog architectures, from simple comparators to complex filters. With 41 op-amps, 100 programmable capacitors, and 6809 electronic switches, MPAA020 can manage various control system tasks. Its linear and nonlinear signal processing abilities support numerous waveform generation functions. Similar to the EPAC family, its clock speed is capped at 1MHz, limiting the bandwidths to 200 KHz.

AN120E04, an FPAA from Anadigm [129], was engineered for low-cost analog sig-

nal conditioning in high-volume applications. Operating at 5V and based on a fully-differential SC architecture for DT systems. The FPAA features a 2x2 matrix of SC CABs integrated into a programmable interconnect network, regulated by the on-chip SRAM configuration memory. These cells accept single-ended or differential analog signals and incorporate programmable anti-aliasing filters, a high-gain, chopper-stabilized amplifier for low-noise, and a DC offset voltage below 100 µV . Furthermore, AN120E04 includes a Successive Approximation Register (SAR), a 256 Byte LUT, a 4-to-1 input multiplexer and capable to interface DC to 2MHz signal bandwidth, making it a versatile platform for prototyping analog sensor signal processing for various applications. Anadigm's third-generation FPAA product, AN231E04 has replaced AN120E04 [130]. The upgraded chip operates at 3.3V and supports advanced analog signal processing and nonlinear operations such as sensor response linearization and arbitrary waveform synthesis. The chip's configuration data is stored in an on-chip SRAM configuration memory loaded by a simple SPI-like interface protocol. This memory is shadowed, allowing an uninterrupted operation while loading a new circuit configuration. The Anadigmdesigner2 software and a development board enable instant prototyping of any circuit captured in the tool [131–134].

The aforementioned FPAA solutions share two key characteristics. First, they use coarse-grained configuration at the block level, providing flexibility for dynamic, user-driven prototyping and the synthesis of various analog and mixed-signal systems [135]. However, circuit function reliability under extreme conditions is not assured, with qualifications only for best-case scenarios in military-grade environments [136]. Second, their control over the system structure is limited, making them program-oriented and capable of only a partial evolution.

The first reported physical implementation of analog EHW was proposed by Higuchi's group in Japan [137] and Stocia's group at the NASA Jet Propulsion Laboratory (JPL) [138], with the aim of executing genetic evolution on real hardware.

Higuchi et al. [137] employed GA to optimize the center frequency of the intermediate band-pass (IF) $G_{m\text{-}C}$ filter used in cellular phones by adjusting the transconductance value of 39 cells. The optimization process is facilitated by incorporating reconfigurable current sources, as illustrated in Figure 2.1, which allows for the genetic selection of individual current values. This feature enables precise fine-tuning of the bandwidth of

the filter, ultimately enhancing its yield. Standard techniques such as PLL, are suitable for tuning the bandwidth if all stages have identical static shifts and change equally with respect to the dynamic effect.

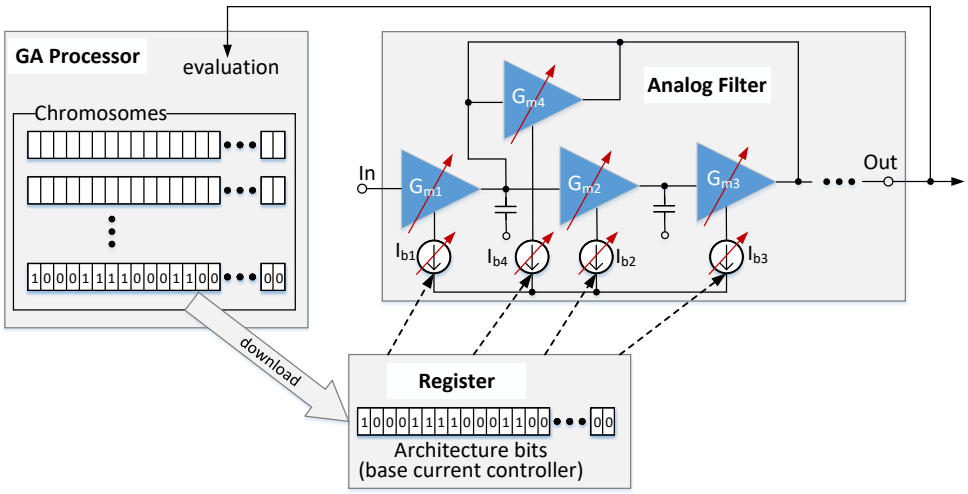

Figure 2.1: Analog EHW chip for IF Filters [139].

The NASA JPL group has proposed an analog EHW at the transistor level, known as the Field Programmable Transistor Array (FPTA) [138]. The first FPTA chip was fabricated using 0.5 µm CMOS technology and contained 64 FPTA cell [139–141]. As illustrated in Figure 2.2, each FPTA module comprises an array of eight fixed-size MOS transistors that can be autonomously interconnected to synthesize various circuit topologies through programmable interconnections managed by the 24 MOS switches. Cascading multiple FPTA modules allows the on-chip evolution or self-reconfiguration of more complex digital, analog, and mixed-signal circuits. However, the absence of basic passive elements, such as capacitors and resistors, in the FPTA structure limits the scope of the evolved circuit solutions. The FPTA can be understood as a fine-grained FPAA architecture [140, 142].

Evolutionary processes at the transistor level enable the creation of unique circuit topologies that diverge from the standard human designs. This approach is beneficial for synthesizing robust [143] and fault-tolerant hardware [144] under harsh operating conditions such as extreme temperatures [145]. As illustrated in Figure 2.3, the GA is run by a host machine. Some GA individuals run on the FPTA simulation model, supporting intrinsic evolution, a concept known as mixtrinsic optimization [146]. However, the potential discrepancy between the simulation and the real chip performance may render

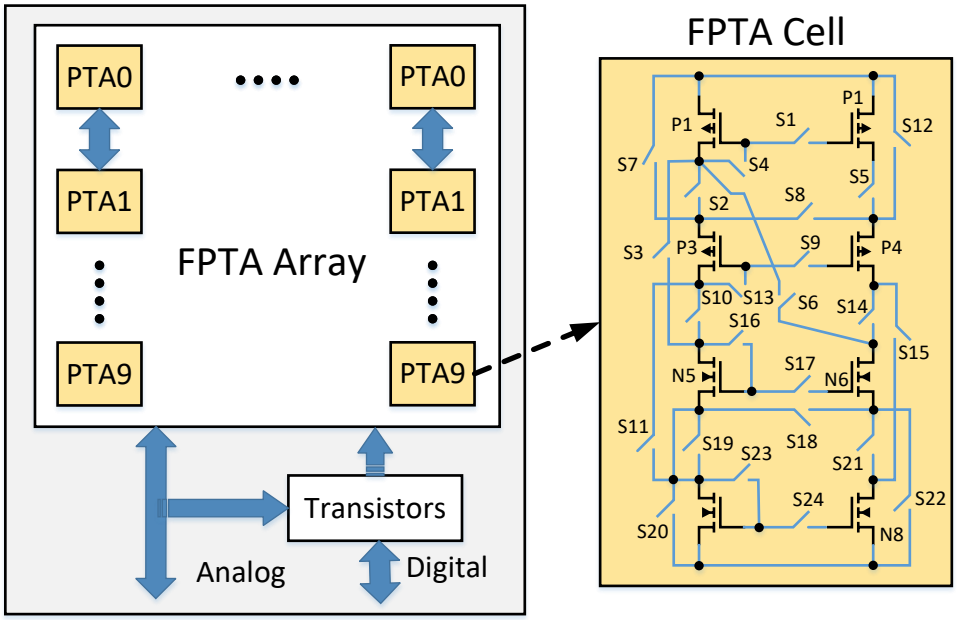

Figure 2.2: FPTA1 module from JPL [139].

reliance on extrinsic simulation disadvantageous, even with mature technology models. Thus, only intrinsic evolution can guarantee valid solutions [140]. Moreover, the time required for running complex analog circuit modules significantly surpasses hardware optimization time, limited only by the chip-optimization unit communication speed, potentially enabling faster performance by several orders of magnitude compared with simulation.

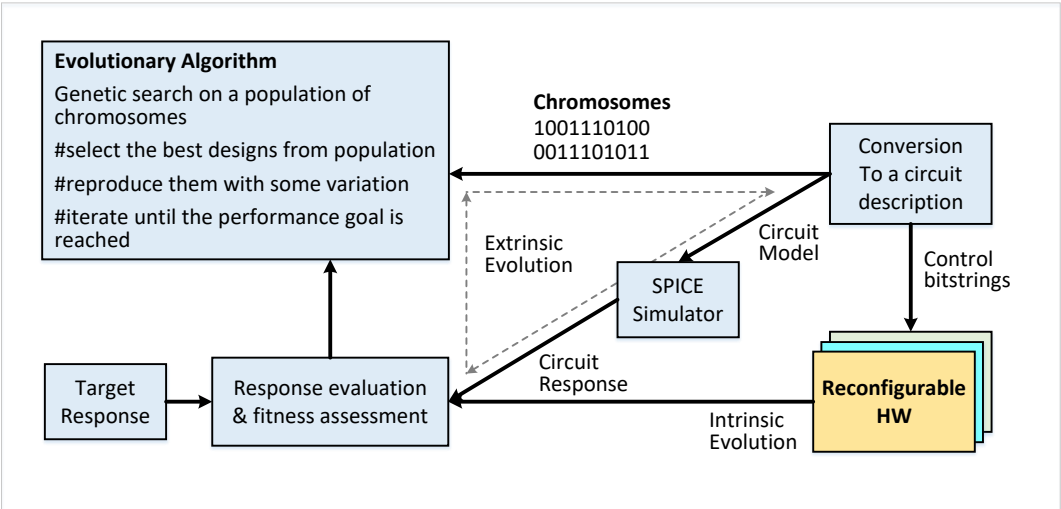

Figure 2.3: Mixtrinsic optimization approach with FPTA [144].

The second-generation FPTA (FPTA2) [147] includes 64 configurable cells with programmable capacitors, resistors, and integrated photodetectors for a vision sensor sys-

tem. Comprised of 14 interconnected transistors and 44 switches, it facilitates complex analog blocks, such as buffered op-amps, filters, computational circuits, and digital circuits. Fabricated using 180 nm CMOS technology, it provides 96 analog/digital inputs and 64 outputs and requires 5000 bits for full chip programming. This presents FPTA2 as the first field-programmable mixed-signal transistor array.

Jet JPL pioneered the Stand-Alone Board Level Evolvable system (SABLES) [148], incorporating a Digital Signal Processing (DSP) unit to execute the GA and provide signal stimuli. SABLES is designed to rapidly prototype self-reconfiguring analog circuits, demonstrating real hardware incorporation in autonomous applications [149]. It is also used to study observer uncertainty related to GA processing and signal stimuli in adaptation loop under harsh conditions. The PC-DSP connection manage communication and post-result analyses, illustrating a significant step toward evolvable System-on-Chip (SoC) integration [150]. SABLES has been successfully validated to automate the FPTA configuration and demonstrate a self-recovery capability for applications at extremely high or low temperatures [151, 152]. Under such conditions, standard on-chip calibration solutions are beyond the control range, particularly when considering critical and long-term missions for space applications [153]. In an upgraded version of SABLES, the authors replaced the DSP unit with an FPGA [80]. Following JPL's footsteps, several research labs, including the University of Sussex [154], Catholic University of Rio [155], and UERJ-Rio de Janeiro State University [156,157], have developed similar board-level evolvable platforms based on discrete components.

However, the fine-grained approach presents several challenges. First, CMOS switch non-idealities, including on/off resistance and parasitic capacitor effects, can impact the performance of the analog circuit, particularly its operating frequency and dynamic performance, making it inferior to ASIC. This issue becomes significant when multiple switches are chosen in series, with the ON resistance of the switch introducing nonlinearity under large signal conditions. Therefore, the frequency response of the FPTA is capped at 100 kHz. Furthermore, series-connected switches develop voltage drops that vary non-linearly with the drawn current and increase the total leakage current drawn from a specific branch [158]. The finite off resistance of the MOS switch prompts the GA to generate new circuit topologies by treating the switch's existing parasitic as a circuit element. Second, evolving a circuit without knowing the estimated circuit size

may necessitate running multiple FPTA modules to find the optimal solution, complicating the algorithm's search space and making it more difficult to find the optimal structural solution. If fewer modules are used, the algorithm may fail to obtain a valid solution. Finally, the fixed size of the MOS transistor in the FPTA severely restricts its adaptability to CMOS analog designs.

The authors in [159] propose an FPAA, built using a tunable continuous-time OTA-C filter with configurable OTAs and capacitors, aimed for high-frequency operations and manufactured using 2 µm CMOS technology. The FPAA features 40 CABs with tuning circuits designed to compensate for PVT variations. Each CAB includes a fully-differential programmable transconductance (g_m) tunable by a factor of 700, a programmable capacitors, and control switches, enabling filter adaptability over a wide frequency range of up to 20 MHz. Compared to Higuchi's FPAA [137], this design offers greater tuning flexibility at the circuit component level, potentially benefiting the development of evolvable analog hardware.

Researchers from Georgia Institute of Technology [160] introduced a new generation of CT FPAA based on the floating gate transistor (FGT) [161], serving as both a crossbar network switch and a computational element in the Computational Analog Block (CAB). FGT's resistance of the FGT, similar to that of a transmission gates, single pass-transistor capacitance, and state memory make it an ideal switch element for a crossbar [162], resulting in a higher bandwidth network with a smaller silicon footprint. The adjustable resistance of the FGT switch allows for a compact, area-efficient FPAA architecture, eliminating the need for space-consuming resistors in the CMOS processes. The proposed FPAA, fabricated using 0.5 µm CMOS technology [158], comprises a 4X4 matrix multiplier, three wide-range operational OTAs, and a capacitive current conveyor per CAB. The team later developed an ultra-low-power SoC-based FPAA chip [163] in 0.35 µm CMOS, integrating a 16-bit open-source MSP430 microprocessor for computation and control. This chip allows rapid reconfiguration of analog and digital computation for various ultra-low-power embedded systems [164].

Concurrently, researchers from Albert-Ludwigs-University presented a novel methodology for CT FPAA topology [165, 166], featuring a configuration of 17 interconnected $G_{m\text{-}C}$ CABs arranged in a hexagonal structure utilizing 0.25 μm CMOS process. These blocks incorporate digitally tunable transconductors, allowing efficient signal routing to

neighbouring cells and enabling self-feedback without using switches in the signal path. Furthermore, each transconductor, in collaboration with the parasitic input capacitance of the connected neighbor cell, forms a $G_{m\text{-}C}$ integrator [167]. This unique configuration offers exceptional capability for artificial evolution and rapid prototyping tools for high-speed and low-power configurable CT filters [168], potentially achieving unity-gain frequencies of up to 200 MHz with an adjustable order. The authors conducted simulations to automatically synthesize a given filter transfer feasible on the array module in Matlab using a GA [169] for online adaptation of process and environment changes [170]. In another study [171], the authors demonstrated intrinsic evolution using GA to autonomously adapt and compensate for changes in the filter characteristics caused by temperature variations.

Researchers from Technische Universität Ilmenau developed an Electrically Programmable Analog Array (EPAA) [172] with granularity distinguished from block to transistor level. With its fully configurable architecture, EPAA can utilize predefined macro-library function blocks or allow transistor-level configuration and support CT and SC techniques. Thus, it is a suitable platform for rapid prototyping of mixed-signal complex SoC systems. The architecture is segmented into four clusters of four cells each. After powering on, the EPAA autonomously downloads the required configuration from EEPROM via a serial system interface. The initial EPAA version was implemented in Alcatel Mietec 0.5um CMOS technology and used in application circuits such as magneto-resistive bridges. EPAA and dedicated software form the Rapid Development Kit (RDK).

Drawing from Higuchi's research and the high-frequency achievements of other coarse FPAA approaches, such as the work in [159], the JPL group revised their concept to facilitate higher levels of configurability and consequently developed the Reconfigurable Analog Array (RAA) [173]. The RAA comprises CABs that are programmable through bias voltages by using DACs at the board level. It can implement adjustable filters and amplifiers with bandwidths of up to 20 MHz [174]. Unlike Higuchi's process variation-centric approach, this new structure focuses on ensuring circuit performance under extreme temperature conditions. The JPL group enhanced the RAA, culminating in the Self-Reconfigurable Analog Array (SRAA) [136]. With temperature compensation capability and an array of elementary cells, including various op-amps, comparators, and

current sources, the SRAA provides ample flexibility for mapping specific circuits, and supplanting traditionally used mission-oriented ASICs. SRAA cells feature adjustable controls for tuning the CABs to offset temperature changes. Notably, the SRAA can operate continuously, while optimal compensation is determined on reference cells. The compensation result is transferred from the shadowing reference cell to the main array. This pioneering field-programmable platform enables online, real-time adaptation while performing its primary function, establishing a hardware-in-the-loop adaptive method.

Jörg Langeheine et al. at Heidelberg University refined the fine-grained FPTA structure initiated by JPL [147], creating an enhanced FPTA [175]. This flexible hardware supports intrinsic evolution, enabling the programming of MOS transistor features such as length, aspect ratio, and connectivity. The initial chip, fabricated using 0.6 µm CMOS technology [176], comprises a 16 x 16 array of programmable transistor cells (either NMOS or PMOS type) as depicted in Figure 2.4 [177, 178]. Each cell functions as a single transistor in the configured circuit and contains 20 transistors, allowing for five distinct lengths and four different widths. A range of lengths is included because the dependency of MOS transistor characteristics on the aspect ratio (W/L) and its actual channel length. This design offers 75 potential aspect ratios, creating a continuous fitness landscape for the evolutionary algorithm and expanding the evolutionary space for developing robust analog and mixed-signal VLSI circuits. The 22-bit data required to configure each cell, including transistor geometry and routing, are stored in RAM units, requiring 6144 bits for the entire chip configuration. The chip includes integrated readout electronics to monitor the temperature, voltage, and current, ensure safety, and facilitate debugging. In addition, metal lines are designed to handle high currents to prevent damage from electromigration, resulting in larger chip areas dominated by routing interconnections [179]. The authors developed an evolutionary system [180], wherein a PC hosts the GA and a PCI interface card enables PC-FPTA communication and fitness measurements. The Heidelberg FPTA chip has recently been used in autonomous robotics [181]. Although the Heidelberg FPTA chip offers flexibility, the accumulated impedance from the series switches restricts the frequency performance to approximately 1 MHz [175, 182]. Another limitation of the chip is its lack of passive circuit elements; it utilizes MOS resistors and capacitors instead, which often lack the linearity of their passive equivalents.

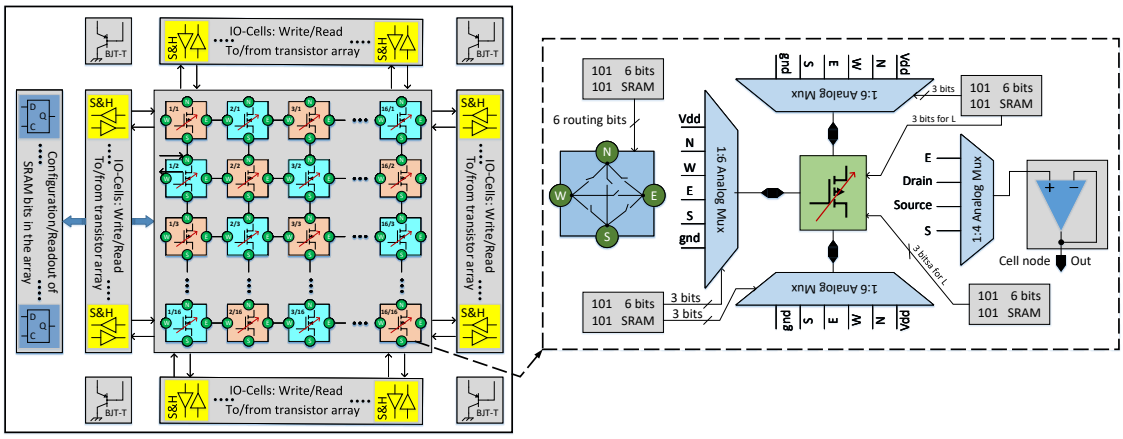

Figure 2.4: FPTA block diagram by Heidelberg group [177].

Regardless of the importance of FPTA-based architectures in evolving robust circuits for harsh conditions, automatic tuning, which operates within a preselected topology, presents a simpler challenge compared to the comprehensive task of automated circuits synthesis from scratch [151]. Therefore, in the industrial electronics community, where amplitude-domain representation is common, the extensive degree of freedom at fine granularity is often seen as impractical due to the excessive resources of switches, memory and routing, increasing the chip area and the fabrication cost while offering inferior dynamic performance compared to ASIC.

The research team from TU Kaiserslautern [183, 184] has made significant progress in studying the granularity level in configurable electronics, examining the beneficial and detrimental aspects of fine (FPTA) and coarse-grained approaches (FPAA). They initiated a hybrid granular level approach in between, the Field Programmable Medium-Granular Mixed-signal Array (FPMA) [185–187], designed explicitly to create generic and dynamically-reconfigurable hardware suitable for rapid prototyping of a wide range of established CT circuits for sensory electronics. The primary goal of the medium-granular approach is to ensure acceptability and compatibility with industrial standards. FPMA comprises heterogeneous arrays of active and passive scalable devices. This design provides a flexible platform for implementing various algorithms, ranging from simple computations to more complex organic/genetic computing. Consequently, it enables the realization of robust and fault-tolerant systems with drift compensation and life-like features such as self-healing, self-adaptation, self-monitoring, self-calibration, and self-repair, collectively referred to self-X properties [78].

In their proposal, simulated employing 0.35 µm CMOS technology, the authors adeptly reduced the switch count by integrating existing design knowledge through predetermined circuit topologies to achieve predictable system behavior, ensuring compliance with industrial standards. This approach guarantees that invaluable insights from experienced designs are transparent and can be thoroughly exploited during optimization. In contrast to fine-grained homogenous FPTAs, where the optimization algorithm starts from scratch or 'primal soup' every time and treats the EHW as a black box, possibly leading to arbitrary structures and not completely predictable underlying behaviors. The researchers fixed the transistor length to 1 µm based on the best simulation-verified performance of analog cells. The transistor aspect ratio is determined by employing a binary-weighted array with dimensions in powers of two of the minimum unit width transistor, as shown in Figure 2.5. These steps led to a significant decrease in the number of configuration switches and enhancing the dynamic performance of the circuit. The benefits also included reduced chip area, decreased memory storage requirements, reduced configuration time, and fewer variables for the optimization algorithm to handle, further expediting the optimization process. Disabling the analog circuit during configuration inherently isolates the analog parts from digital switching interference, allowing for the mutual usage of power pins between the analog and digital components. Additional advancements have been made by organizing the switches into three groups: a low-level group for programming scalable devices, a medium-level group (termed topology switches) to alter the overall amplifier topology apart from the fixed circuit topology, and a top-level switch group for configuring single or multiple amplifier blocks with feedback circuitry to implement more complex analog and mixed circuits, such as instrumentation amplifiers (in-amp), active filters, ADC, etc. The authors demonstrated the proposed FPMA by implementing a configurable folded cascode op-amp and a more intricate Generic Operational Amplifier (GOPA). The GOPA provides adaptability in setting up the topology and programmable elements. Capable of actualizing over 15 well-established amplifier structures and implementing single-ended and differential circuits with programmable compensation techniques. The GOPA ensures complete versatility in both the selection of the structure and sizing of the devices included within these structures.

The authors presented the initial measurement results of the first fabricated FPMA

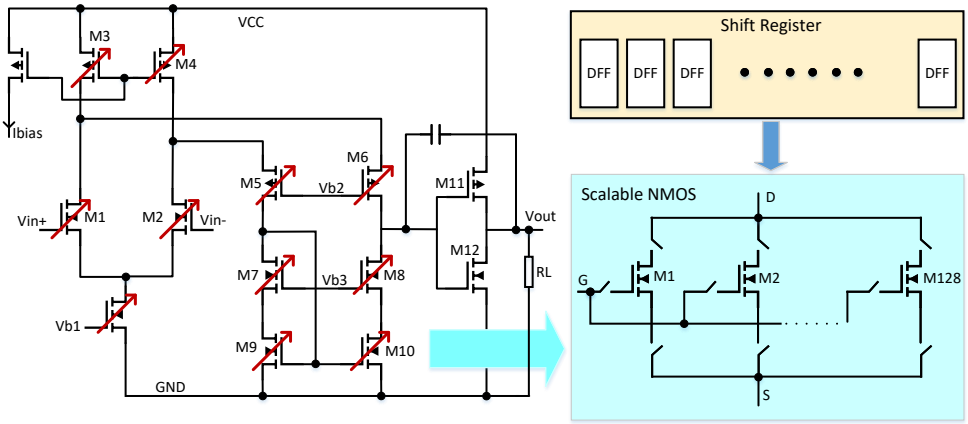

Figure 2.5: Reconfigurable FC-OPA presented by [185] showing the replacement of regular transistors by scalable transistors.

chip in [63]. These results were based on manual configurations imported from the design phase, specifically for testing the folded-cascode op-amp part. In [188], the two-stages Miller op-amp part was tested using extrinsic configurations derived from running the particle swarm optimization algorithm (PSO) [189, 190] on the circuit netlist. Furthermore, in [191], the authors presented their first intrinsic optimization results to examine the system performance in dynamic environments, where the FPMA chip-in-the loop can adapt to temperature changes. The proposed reconfigurable sensor system, depicted in Figure 2.6, comprises three main blocks: the reconfigurable hardware, the optimization unit that employs an evolutionary algorithm, and the assessment unit responsible for generating signal stimuli, measuring, and extracting hardware specifications during the reconfiguration process.

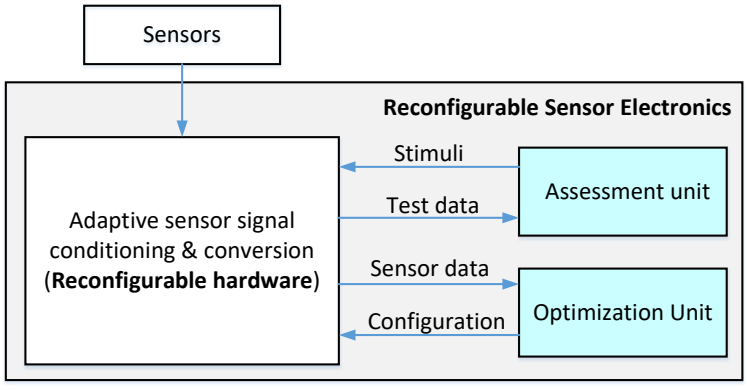

Figure 2.6: Conceptual block diagram of the evolvable sensor system. [191].

Additionally, in [192], the authors introduced a new type of mixtrinsic evolution. This approach simulates a set of specifications that are challenging to measure due to

cost and time requirements. Conversely, specifications that are more sensitive to instance deviations are intrinsically measured , as illustrated in Figure 2.7. It is worth noting that, unlike in [146], their approach employs the term "mixtrinsic multi-objective evolution" to indicate the use of both intrinsic and extrinsic evolution for each individual but for different objectives.

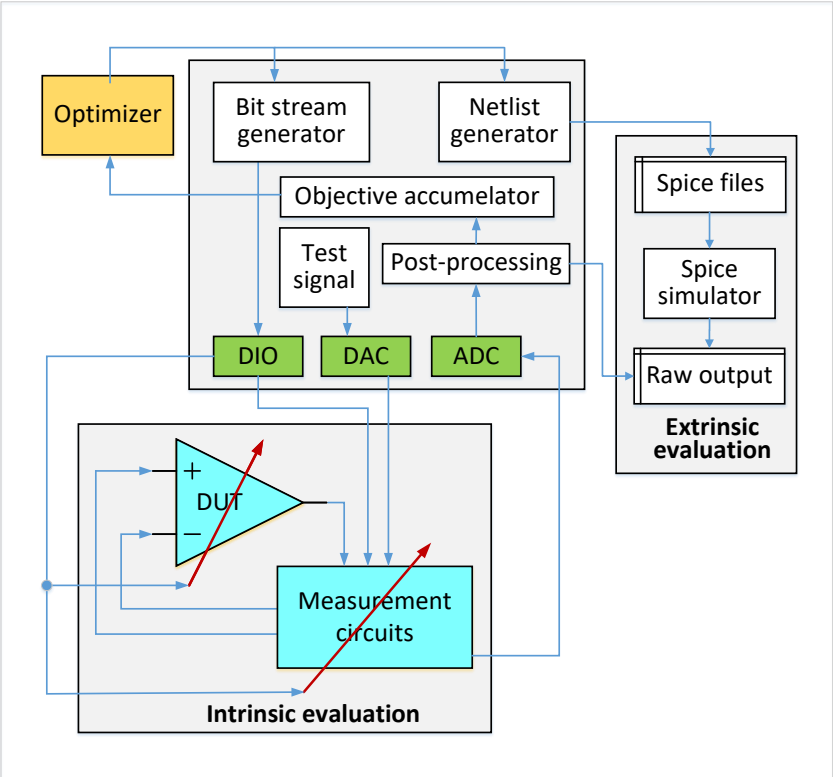

Figure 2.7: New type of mixtrinsic multi-objective optimization environment [192].

A revised version of the authors' work known as FPMA2 [87, 193, 194] was released and underwent several substantial changes. First, they incorporated matched layout techniques to effectively average the substrate-induced noise. Second, they reduced the number of switches per transistor unit in the array by controlling only the gate voltage and removing the switches from the drain and source terminals, thereby decreasing the parasitic node capacitance. Third, they employed charge pumps to boost the gate voltage, thereby reducing the ON resistance of the switch. These modifications collectively led to improved dynamic and noise performances. Furthermore, the use of highly resistive poly (rpolyh) from the technology provider enabled the achievement of higher resistor values, which proved to be essential for realizing feedback circuitry and constructing complex structures such as the instrumentation amplifiers demonstrated in [194]. The flexibility afforded by the FPMA approach motivated them to develop an analog IC

training board. This board facilitates rapid prototyping of analog circuit designs and is specifically designed for educational purposes [195]. Comprehensive information about FPMA1, FPMA2, and the optimization approach can be found in [196, 197].

Moreover, researchers from TU Kaiserslautern [198] expanded the concept of self-X vision to enhance the design of intelligent integrated sensor systems based on intrinsic and extrinsic optimization. They successfully proposed self-X principles at various levels of abstraction of the sensor system, including the lowest hierarchical level and sensor element within the optimization loop, as illustrated in Figure 2.8. This integration aims to minimize errors in the sensor measurements for critical applications. To achieve this implementation, different calibration actuators, such as DAC and power electronics, need to be integrated, depending on the sensor type for controlling the sensor behavioural [199–201] as depicted in Figure 2.9 [202]. Optimization can lower the power consumption of wireless sensor nodes by managing the power of the sensor bridge using a programmable current source under the control of the self-X [203, 204]. Additionally, it is feasible to adjust the output common-mode voltage or sensor bridge offset voltage by regulating the adjustable current source that powers the sensor bridge.

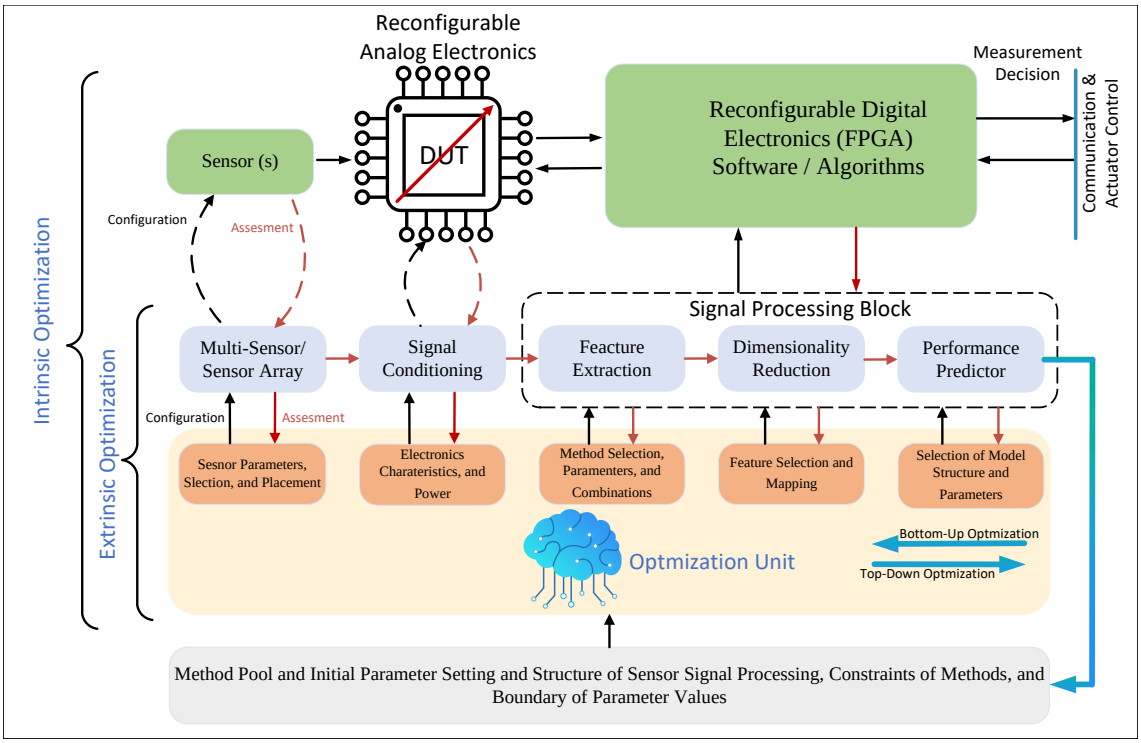

Figure 2.8: Enhanced design methodology for intelligent sensor systems with self-X properties on various levels of abstraction [198].

A joint effort by Arizona State University and Intel Inc. resulted in a new fine-

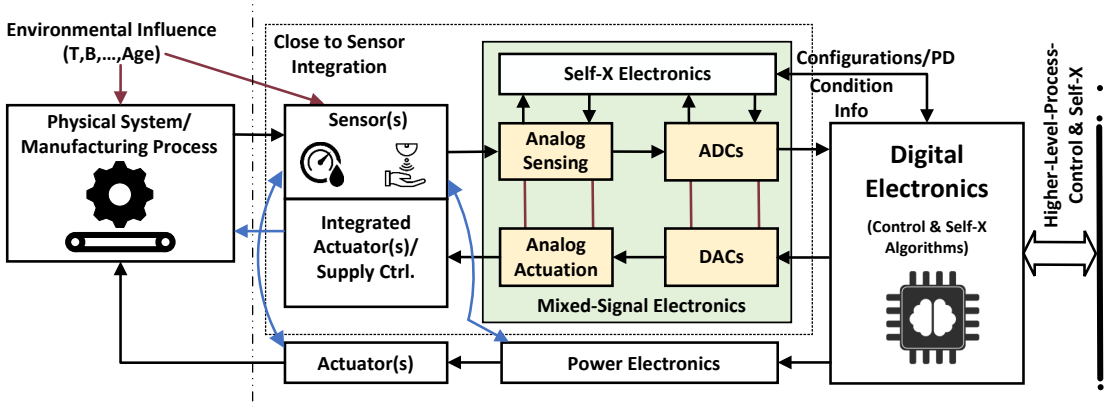

Figure 2.9: Realization of self-X properties at the sensor level [202].

grained transistor-level FPAA structure, named Programmable ANalog Device Array (PANDA) [205]. It features parasitic reduction by leveraging CMOS technology scaling, designed at a 32nm node. PANDA architecture, feature device array blocks and switches [206]. CMOS switch integration within cells facilitates cell transistor sizing, absorbing additional voltage drops during configuration, and prevents performance distortion upon cell connection. The initial PANDA, fabricated using 65 nm CMOS technology, includes a 24 × 25 heterogeneous cell array, reconfigurable interconnect, configuration memory, and a serial programming interface. It also integrates programmable resistors, capacitors, and parasitic BJTs, thereby enhancing its adaptability [206]. This versatility enables the PANDA to emulate circuits with several hundred equivalent analog transistors, making it a suitable platform for evolvable hardware and rapid AMS circuit prototyping [207].

2.2 Assessment Unit for in-field Optimization

One of the major challenges in supporting on-chip self-X features for mixed-signal and analog sensory electronics is the integration of the assessment unit, commonly referred to as Built-in Self-Test (BIST). Otherwise, measurements must be conducted off-chip using expensive and time-consuming laboratory or automatic test equipment (ATE) [208], rendering it impractical for in-field optimization. The inclusion of BIST introduces difficulties [209] that revolve around generating accurate stimuli and measuring responses from the design/circuit-under-test (DUT/CUT) [67]. BIST must be capable of on-chip stimulus generation, often necessitating higher-resolution devices for precise measurement of results. Moreover, the BIST circuitry must exhibit superior accuracy and speed compared to the DUT, further complicating the implementation process. Additionally,

BIST must ensure the controllability and observability of the DUT across diverse environments and applications to achieve comprehensive testing and optimization.

In addition, the integration of BIST faces significant hurdles in terms of the increased complexity and cost of measurements when multiple performance parameters require simultaneous tuning in high-frequency and RF circuits. To relieve the reliance on expensive ATE, authors in [210] proposed an embedded envelope detector as a simple test response feature extractor. This component converts the DUT response to a tailored diagnostic test stimulus into a low frequency "signature." This conversion reduces measurement costs and complexities and eases the performance evaluation process. The signature is then mapped to optimum performance-control values, such as biasing voltages/currents and configurable/tunable circuit elements, using predetermined regression models derived from the experimental data on the DUTs. The DSP and ADC units are pre-calibrated using standard methods. The test stimulus is designed such that the response from the envelope detector is strongly correlated with the DUT's test specifications under multi-parameter process variations. Hence, changes in the performance metrics of different DUTs are indirectly measured by observing the output variations from the envelope detector. These data allow the trained regression model to predict the optimal tuning values from the sensor output. Thus, the proposed methodology enables in one-shot, a simultaneous optimization of multiple design metrics through a single, simple test stimulus with minimal reliance on external test equipment. Although a similar approach was suggested in [211], this methodology deviates by analyzing the output of the DUT from the sensor's output rather than the DUT.

Building upon these principles, the study by [212] presented a hardware architecture tailored for in-field self-calibration of analog/RF ICs utilizing on-die learning. The authors proposed an on-chip analog neural network capable of training to execute a nonlinear regression function. This function is employed to approximate a Figure-of-Merit (FoM), which is indicative of the IC performance. The regression function is driven by readings obtained from cost-effective on-chip sensors in response to simple on-chip-generated stimuli, as depicted in Figure 2.10. The FoM is predicted for all potential settings of the configurable knobs meant for performance calibration, from which the optimal setting is selected. The effectiveness of the methodology is demonstrated via a tunable Low-Noise Amplifier (LNA) designed and produced using IBM's 130nm RF

CMOS process. The experimental results suggest that the introduced self-calibration technique facilitates significant yield enhancement.

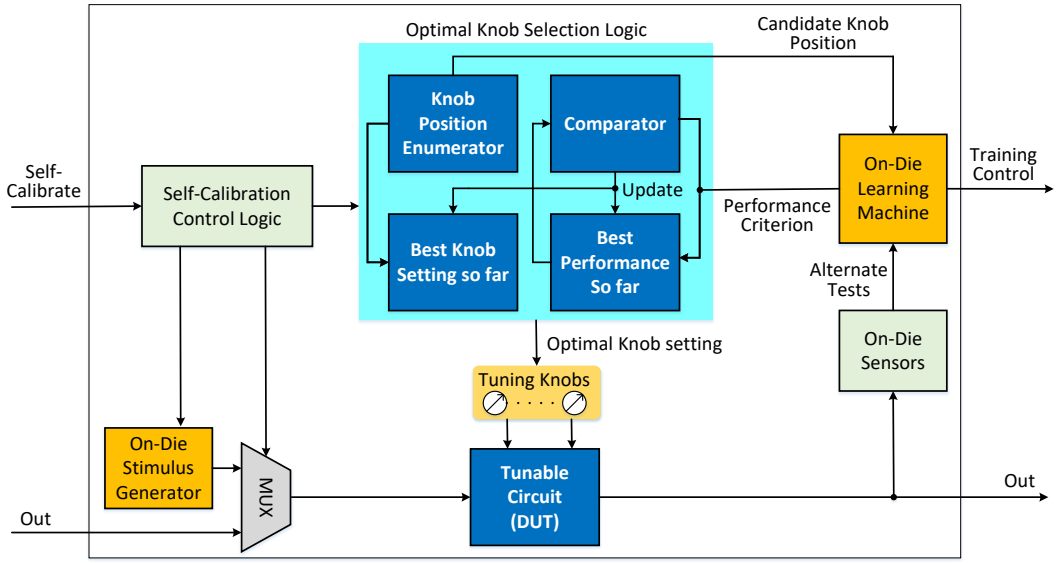

Figure 2.10: Self-calibration architecture proposed in [212].

The authors in [213] introduced non-intrusive sensors (NIS), a new type of feature extractor sensor designed to facilitate built-in self-testing (BIST) for RF circuits. The NIS performs DC or low-frequency measurements, effectively reducing testing costs. Uniquely, these sensors remain electrically disconnected from the CUT, thereby preserving their performance. Therefore, the NIS can be integrated into the design without modifying the CUT to account for sensor effects. The NIS is constructed using basic analog stages that replicate portions of the topology of the main circuit. They also incorporated stand-alone layout components, such as transistors and capacitors, directly copied from the circuit's layout. The dimensions of the NIS components match those of the corresponding components in the CUT. By placing the sensors in close proximity to the CUT, they exhibited the same global process variations and operating conditions. Consequently, the sensor measurements exhibit a strong correlation with the CUT performance, maximizing their proximity to encompass local process variations and temperature. Therefore, any shifts in the CUT performance can be implicitly predicted by analyzing the corresponding shifts in the NIS measurements. In principle, the NIS concept is inspired by the process control monitors (PCM) proposed [214–216] and can be activated on-chip or triggered by an external stimulus.

The first implementation of one-shot self-calibration based on indirect measurement

using NIS is proposed by the authors in [217] using 65 nm CMOS technology. Calibration is achieved by incorporating tuning knobs into the CUT. A pre-trained regression model is utilized in the calibration algorithm to establish the relationship between the circuit performance, sensor measurements monitoring process variations, and tuning knob values as illustrated in Figure 2.11. The tuning knob values are optimized in the software in the background, minimizing the cost and calibration time [104]. Notably, the sensor measurements remained invariant when the tuning knobs were adjusted. Consequently, the sensor measurements only need to be obtained once, after which their values can be plugged into the regression model to optimize the relationship between the performances and tuning knobs without repeating sensor measurements for each tuning knob setting. It is important to note that pre-trained regression models should be refined periodically to account for process shifts over time.

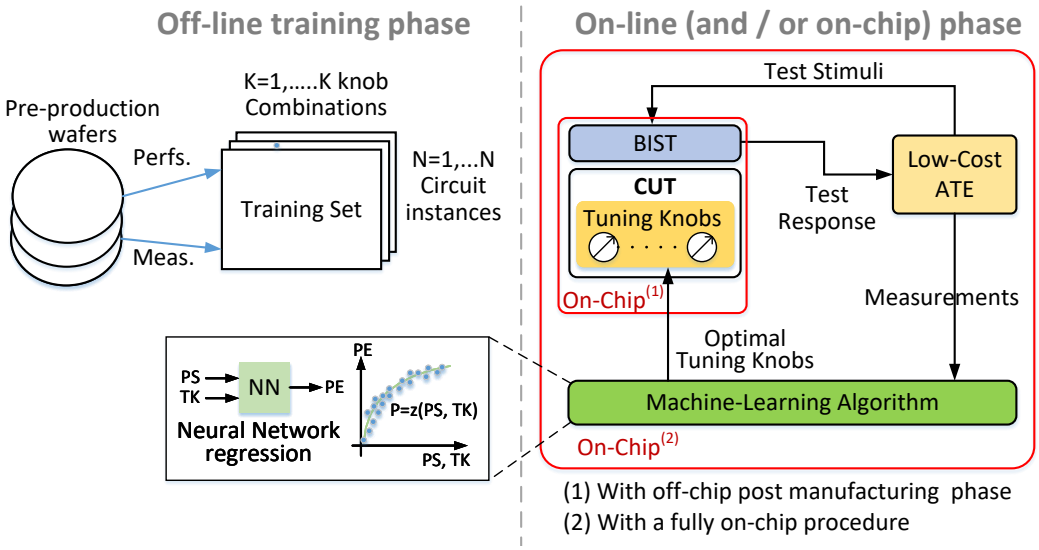

Figure 2.11: One-shot calibration based on non-intrusive sensors and machine learning [218].

To enhance the accuracy of the NIS regression module, it is imperative to employ a more comprehensive training statistics data set garnered from a varied selection of fabricated samples collected from distinct wafer lots. This approach is beneficial for calibrating the design around the central point with limited variables. However, it lacks efficiency when tuning a design with several variables over a wide range, making the training tedious and time-consuming. Therefore, the authors in [82] preferred implementing the BIST circuit based on direct measurement for autonomous tuning of the reconfigurable 2nd-order Butterworth band-pass filter bandwidth. However, a frequency

range of up to 31 MHz is affordable by the ADC/DAC integrated parts. The BIST circuit incorporates sinusoidal and pulse signal generators and a digital optimization unit running metaheuristic optimization algorithms, all within the same chip, as depicted in Figure 2.12. This approach eliminates dependence on external test equipment, general-purpose digital signal processors, or training. The effectiveness of this technique is confirmed through simulations and measurement results obtained from a test chip fabricated using 180 nm CMOS technology. The authors in [83] follow a similar direct measurement approach for optimizing Tow-Thomas bandpass biquads using BIST and integrated optimization unit parts for in-field/in-situ optimization. Notably, this approach is not restricted to specific characteristics of CUT, enabling its application to any linear time-invariant circuits and does not require prior knowledge or training of the CUT. A similar approach is followed by the authors in [83] for optimizing Tow-Thomas bandpass biquads using a BIST circuit with direct measurement and digital optimization parts for in-field/in-situ optimization.

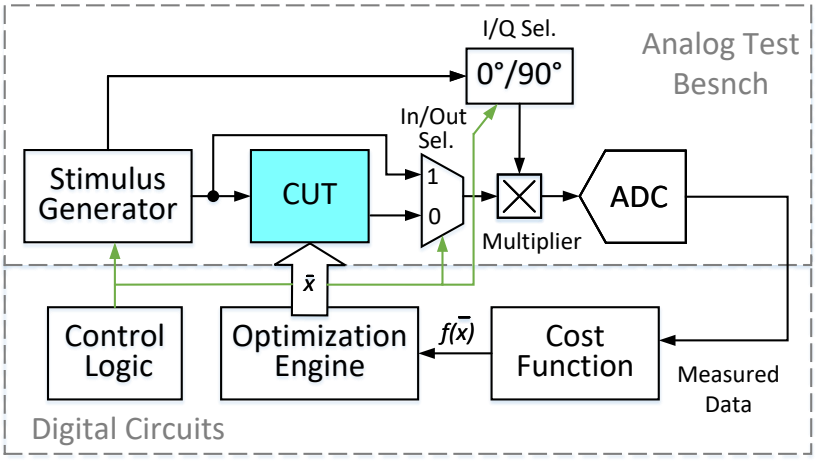

Figure 2.12: Built-in self-optimization system proposed in [82].

Synopsys Inc. developed the Silicon Lifecycle Management (SLM) system following the acquisition of Moortec. The SLM, which is based on in-chip sensing devices and control loops, is seamlessly integrated into SoC designs and is accompanied by a robust data collection strategy [219–222]. In-chip PVT monitors are key for SLM, because they provide real-time post-silicon data under varying physical and environmental conditions. This includes tracking process variation, silicon aging effects, static and dynamic voltage IR drops, and temperature hotspots in dense, small-node devices. Such monitoring aids in precisely optimizing each stage of the semiconductor lifecycle, en-

hancing the power consumption, speed performance, and long-term reliability [220, 223]. Built-in PVT sensors continually track both dynamic operating conditions and static process characteristic shifts, therefore, enabling in-field optimization and early anomaly detection. This helps to prevent failures, ensuring that power consumption and thermal dissipation remain within the design specifications. The SLM can analyze the collected data on-chip for performance and security optimizations, or transmit it to the cloud for further analysis. This dual-level approach ensures the intended device performance as intended and facilitates the early detection and resolution of unexpected device issues, as illustrated in Figure 2.13.

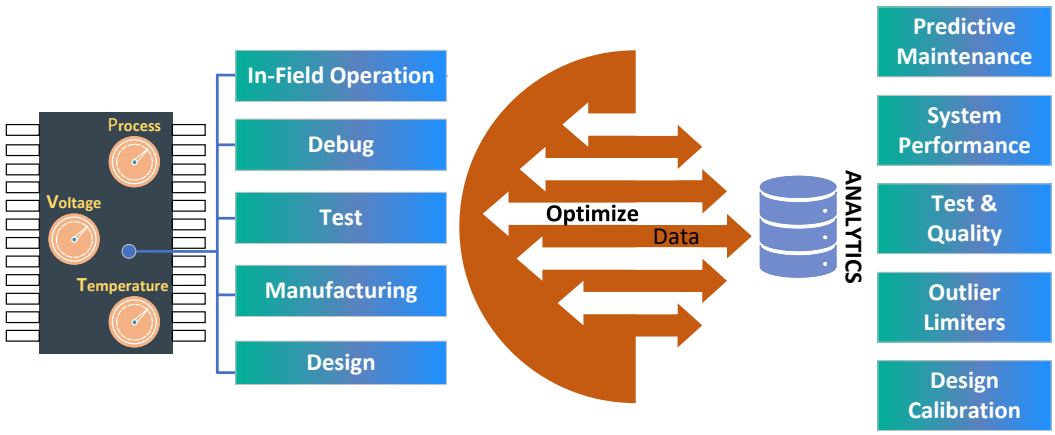

Figure 2.13: Silicon Lifecycle Management (SLM) from Synopsys

2.3 Universal Sensor Interface Systems

In [224], the authors presented a Universal Microsensor Interface (UMSI), a reconfigurable mixed-signal transducer interface circuit developed using 0.5 µm CMOS technology. The UMSI adaptively interfaces with diverse capacitive, resistive, voltage, and current mode sensors and actuators, delivering programmable gain and offset controls, self-testing, self-calibration and various power management features. It provides both digital and analog outputs for the actuator control. The UMSI establishes an intelligent communication link using a central microsystem controller that accommodates a broad spectrum of sensors and actuators. With its real-time reconfigurability, peripheral interfacing, and plug-and-play operation, the UMSI streamlines system design and upgrades. The versatility of UMSI in interfacing with numerous transducers and signal levels outperforms previous multi-sensors interfaces, making it a cost-effective solution

for low-power multi-sensor microsystems.

The authors in [225] presented a versatile, adaptive multi-sensor SoC system for the first time, capable of real-time monitoring of multiple physiological parameters for biomedical applications. This SoC, fabricated using a standard 0.35 µm CMOS process, integrated four on-chip sensors to interface with diverse sensor signals (C, R, I, and V). Based on SC circuit technology, a linear and reconfigurable sensor readout was employed to efficiently process these signals. The system also featured a dual-input energy harvesting interface with a 73% conversion efficiency, capable of harnessing light and RF energy for long-term battery-independent operation. Distinguished by reconfigurability, self-powering, signal processing, and wireless communication capabilities, this SoC offers a more intelligent, adaptable, and sustainable operation than previous models. Furthermore, its ability to serve as a universal sensor platform facilitates easy integration of various sensor types.

As a significant step towards addressing the growing demands of Industry 4.0, the authors from the TU Kaiserslautern have developed a Universal Sensor Interface with Self-X Properties (USIX) [226], as illustrated in Figure 2.14. The proposed chip boasts versatility, flexibility, and robustness, serving as a single interface chip for various physical quantities such as voltage, current, resistance, inductance, capacitance, and temperature. All these measurements can be performed using a single chip manufactured with 0.35 µm technology. Moreover, integrating flip coil circuitry into the design allows for the self-healing capability of magnetoresistive sensors. The IC can supply reference voltage, current, or AC signals to both sensors and external structures.

Following the baseline of sensory electronics with self-X features for Industry 4.0 highlighted in [85], the authors introduced an updated version of the chip named USIX 2.0 [227], specifically optimized for angle computing utilizing a high dynamic range, dual-bridge TMR sensor interface. This revised chip incorporated impedance spectroscopy measurements [228] along with various other circuit capability enhancements. Notably, these enhancements include an in-amp with a high input span and concurrent offset calibration, the design of 4-rows shadow registers for improving the speed of the configuration and enabling hot-swapping between different configurations with the due time of measurement.

In [229], a method similar to USIX is proposed, featuring a fully reconfigurable

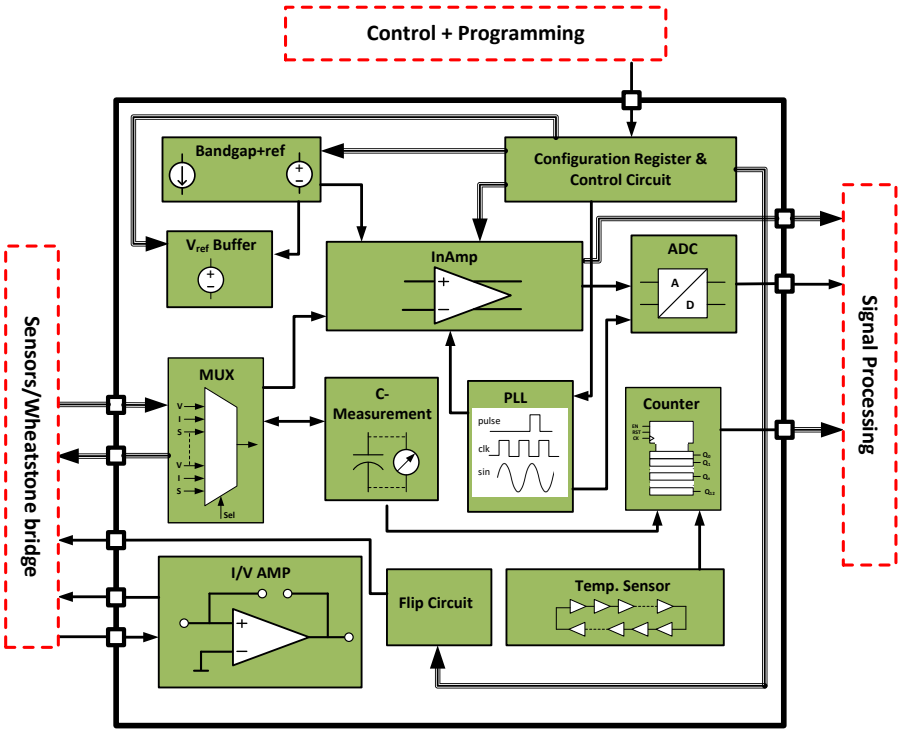

Figure 2.14: USIX chip block diagram as proposed in [226].

universal sensor AFE designed for IoT applications. This AFE can process various sensor outputs (R, C, V, and I) using a single-input bond pad and a reconfigurable AFE. It incorporates a reconfigurable acquisition mode selection method to accommodate a wide range of sensor outputs, and a compensation method to counteract circuit saturation and improve sensor output sensitivity. Additionally, a correlated double-sampling (CDS) technique is used to minimize the impact of low-frequency noise on the sensor output. Notably, the system maintains detection accuracy within approximately a 1% relative error for the target sensor output range using a single input bond pad and AFE, all realized using the TSMC 0.25-µm CMOS process.

In contrast, [230] presented a reconfigurable Universal Multi-Sensor Interface (UMSI) circuit design. The UMSI achieves a broad dynamic range for capacitive and resistive sensors, while preserving ultra-low power consumption. It optimizes sensitivity, linearity, and power consumption by selectively covering the necessary range for each sensor element. The system is fabricated using a CMOS 0.18 µm process and utilizes SC circuits with programmable capacitors to enhance configurability

Building on 0.18 µm CMOS and SC technology, the authors in [231] developed a versatile, high-precision universal AFE interface for multi-parameter (R, C, V) sensors.

This circuit accommodates a wide range of sensor outputs by incorporating a rail-to-rail baseline compensation method and a fine offset elimination technique. Furthermore, self-zeroing and CDS techniques reduce low-frequency noise and offset voltage, prevent sensor signal saturation, and enhance overall precision. Integrating configurable elements within the sensor signal acquisition circuit alongside the baseline compensation circuit extends the applicability range of the sensors.

The "Universal Sensor Platform" (USeP) [232] developed by Fraunhofer IIS and GLOBALFOUNDRIES is a highly reliable, fast, and adaptable sensor platform for IoT applications that utilizes cutting-edge low-power 22 nm SOI CMOS technology from GLOBALFOUNDRIES. It offers a wide range of compatible components for customizing the interface according to the user application demand. The compact USeP platform integrates multiple communication standards and provides robust CPU and memory resources. Therefore it enables integration with fog, edge, and cloud computing environments. At its core is a SoC as a central control and computing unit, supplemented by various pre-calibrated pressure, temperature, acceleration, and gas sensors. These sensors can be custom-mounted onto a top-side redistribution layer (RDL) for greater diversity, and additional sensors can be added through a motherboard that supports wireless communication and energy supply.

The Infineon PSoC™ 6 MCU [233] is a highly configurable SoC that integrates a high-performance microcontroller, low-power flash technology, digitally programmable logic, and high-performance analog-to-digital conversion within a single chip. This integration facilitates the consolidation of up to 100 digital and analog peripheral functions. Notable features include a programmable analog part comprising a 12-bit 1-Msps SAR ADC with differential and single-ended modes, two low-power comparators, built-in temperature sensor, voltage reference, and 12-bit voltage mode DAC. The two op-amps provide buffering for SAR inputs and DAC outputs, while being internal. The SoC also incorporates the latest generation of Infineon's CAPSENSE™ capacitive-sensing technology, enabling robust, reliable touch and gesture-based interfaces. The unique architecture of the PSoC™ 6 MCU allows users to create customized peripheral configurations, making it suitable for various applications. The device, when coupled with Infineon's AIROC™ Wi-Fi, Bluetooth, or combo radio modules, serves as a perfect solution for secure, feature-rich IoT products. The rich analog and digital peripherals facilitate the

creation of custom analog front-ends (AFE) or digital interfaces for system components such as MEMS sensors or electronic ink displays.

NXP Inc. offers NAFE11388 [234], a high-precision, industrial-grade AFE featuring low-leakage multiplexers, low-offset buffers, a 24-bit Delta-Sigma ADC, and a low-drift voltage reference. It includes diagnostic functions for condition monitoring, anomaly detection, and fault detection and utilizes LV diagnostic signals and on-chip voltages for self-testing and calibration. The device offers two calibration voltage sources for system-wide self-calibration and maintenance and an on-chip temperature sensor for continuous die thermal monitoring and temperature drift compensation.

Texas Instruments released PGA900 [235], a compact, high-accuracy, low-noise resistive AFE. It integrates an on-chip ARM®Cortex®M0 microprocessor for user-defined calibration and diagnostic functions. Among other compensation algorithms, the device can perform linearization and temperature compensation using its built-in temperature sensor. Additionally, it includes two AFE chains equipped with a low-noise PGA and 24-bit sigma-delta ADC.

MCP3910 from Microchip [236] is a dual-channel 3V AFE incorporating two synchronous sampling Delta-Sigma ADCs, two PGAs, a phase delay compensation unit, a low-drift internal voltage reference, and calibration registers for digital offset and gain errors correction. Each ADC in MCP3910 offers reconfigurable features, including 16/24-bit resolution, oversampling ratio programmability from 32 to 4096, a gain range of 1 to 32, independent shutdown and reset, and dithering and auto-zeroing capabilities.

In contrast, the MLX90329 from Melexis [237] is a mixed-signal AFE IC that includes gain adjustment, offset control, linearization, and temperature compensation using a built-in temperature sensor, microcontroller, and memory units. Compensation values are stored in EEPROM and can be reprogrammed using the Melexis tool, including the necessary software. Furthermore, it integrates two programmable filters. Several input diagnostics are also integrated for fault detection to detect broken input connections or an out-of-range input signal. This diagnostic information is transferred to the microcontroller to handle further actions such as flagging a diagnostic message. Table 2.1 provides a brief comparison between the commercially stated up-to-date AFEs to the USIX2.0 from our institute.

AFE Chip	USeP	PSoC™ 6	NAFE11388
Technology	22 nm	-	-
Granularity	coarse	coarse	coarse
Sensor signal type	R, V, I, C, L	C, V	V, R
Sensor Calibration	No	No	No
Sensor excitation	Yes	No	No
Built-in stimulation	No	No	Yes
On-chip CPU/MCU/DSP	Yes	Yes	Yes

Table 2.1: Comparison between recent AFEs.

AFE Chip	PGA900	MCP3910	MLX90329	USIX2.0
Technology	-	-	-	0.35 µm
Granularity	coarse	coarse	coarse	Medium
Sensor signal type	V, R	V, R	V, R	R, V, I, C, L
Sensor Calibration	No	No	No	Yes
Sensor excitation	Yes	No	Yes	Yes
Built-in stimulation	No	No	No	Yes
On-chip CPU/MCU/DSP	Yes	No	Yes	No

Table 2.2: Comparison between additional AFEs.

2.4 Discussion and Open Issues

Field-programmable electronic hardware spans three granularity levels: coarse-, medium-, and fine-grained. Coarse-granular FPAAs are ideal for rapid prototyping and complex sensor systems but have a limited evolutionary scope and are user-programmable. Fine-grained evolution offers bio-inspired optimization but has drawbacks, such as hardware resource requirements, non-linearities, and unpredictable outcomes, making it less attractive for industrial use. Medium-granular FPMA offers a balanced solution with a predefined circuit topology, flexibility, and predictability, achieving compliance with industrial standards but with a larger area and lower dynamic performance cost than ASIC.

In-field optimization requires BIST integration with reconfigurable hardware to as-

sess the circuit responses under operational conditions. If the signal bandwidth matches the on-chip ADCs and DACs resources, direct measurement-based BIST can be used. For complex metrics, indirect methods, including intrusive or non-intrusive types, are appropriate. However, these static methods fail to consider performance variations caused by tuning or calibration knobs changes. Although this approach works for centering the design around an optimal operating point, tuning for a wide operational range with more variables becomes tedious and time-consuming.

The evolutionary process involves extrinsic, intrinsic, and mixtrinsic evolution; however, simulation is not always effective, especially when there is a significant difference between the circuit model and the fabrication outcome.

Recent advancements in heterogeneous technology and SoCs have allowed the integration of optimization units, BIST, wireless communication modules, and PVT sensors on evolvable chips for power and speed performance optimization, maintaining safe operating conditions, and enhancing long-term reliability.

Hence, it can be inferred from the reviewed state-of-the-art that certain areas require optimization, specifically in terms of the granularity level and measurement performance evaluation for in-field optimization and PPAC metrics, as demonstrated in Figure 2.15. These issues, while ensuring compliance with Industry 4.0 standards, will be the focus of this thesis.

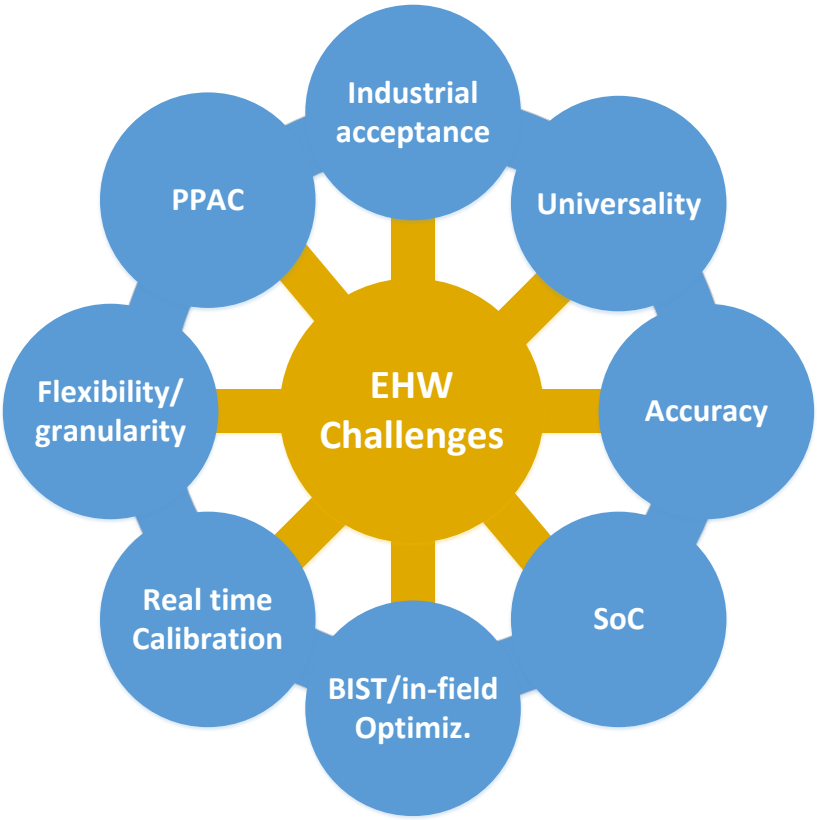

Figure 2.15: EHW challenges as keywords to improve in this work

Chapter 3

Proposed AFE with Self-X Features

In-field optimization of smart sensory electronics (SSEs) with self-X properties imposes challenges in terms of reliability and power efficiency, in addition to the extra die requirement for utilizing configurable elements of the circuit, which eventually leads to an increase in the chip cost and trade-off of the PPAC metrics. Furthermore, a significant hurdle remains in achieving practical in-field optimization of EHW due to the complexity, accuracy, and cost of the feature extractor unit used to evaluate the Device Under Test (DUT).

This chapter introduces the proposed methodology for the in-field optimization of the AFE of SSEs, consisting of a fully-differential indirect current-feedback instrumentation amplifier (CFIA) followed by a fourth-order tunable anti-aliasing filter (AAF), as shown in Figure 3.1. It is worth highlighting that the author has taken responsibility for the circuit and chip design, while another Ph.D. candidate working in parallel on the same project [112] implemented the optimization algorithm in both the software and hardware aspects for extrinsic and intrinsic realization.

Furthermore, to enhance this methodology, this chapter delves into the utilization of non-intrusive sensors for indirect measurements. These sensors are positioned in close proximity to the main DUT, ensuring that they undergo identical variations in process, voltage, and temperature (PVT), thereby guaranteeing accurate and consistent measurements of the environmental and physical impacts. A regression model establishes a correlation between these sensor readings and the performance metrics of the DUT,

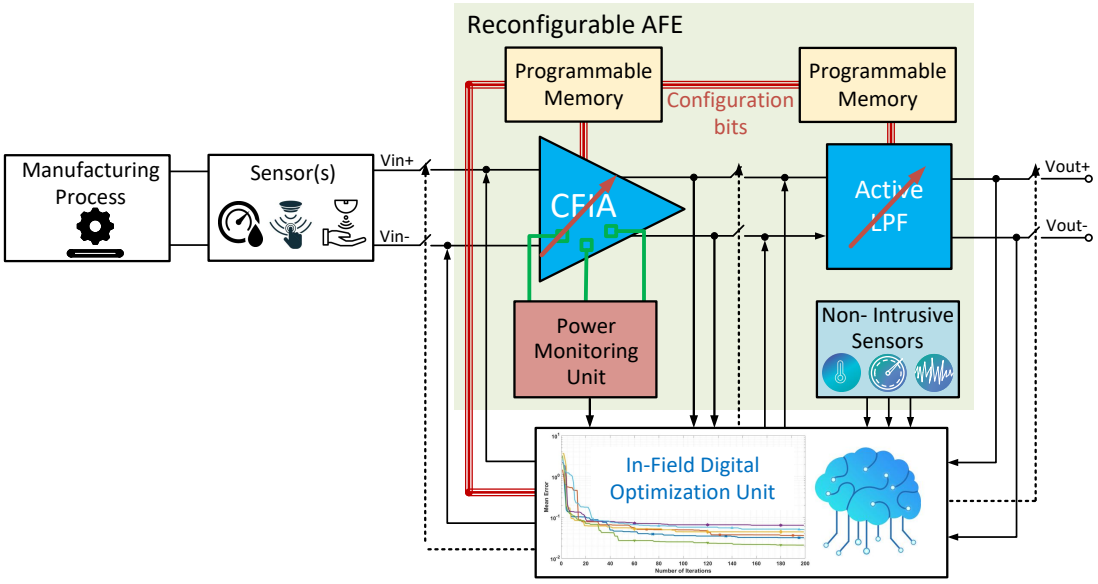

Figure 3.1: Functional diagram of the proposed SSEs with self-X properties for infield optimization

adding a layer of indirect yet efficient performance estimation. One application of this approach involves its integration into optimizing the AAF, which is a critical component in signal conditioning. Specifically, the AAF employs the Sallen architecture with a Butterworth approximation to eliminate noise within the Nyquist bandwidth before the signal is converted by the ADC. This approach extends the available bandwidth range; however, tuning across this range traditionally requires resource-intensive measurements. To tackle this challenge, our methodology introduces a non-intrusive sensor (NIS)-based indirect measurement technique, rendering the tuning process cost-effective and efficient without disrupting the operation of the DUT. By combining low-cost indirect measurement methods such as THD, robust optimization strategies, and non-intrusive sensing techniques, this chapter aims to provide a comprehensive approach for optimizing complex SSEs.

The keywords of this work can be outlined in four perspectives:

1. The presentation of fully differential analog circuits with wide input dynamic range.
2. Restricting the reconfigurable circuit components exclusively to the sensitive parts.
3. Introduce a cost-efficient system performance assessment setup using indirect measurement techniques that complement automatic test equipment (ATE).
4. Reducing uncertainties in observations, primarily stemming from flaws in the sen-

sor and/or ADCs.

In the proposed framework, the overhead associated with implementing the self-X SSE is minimized, offering the potential for superior dynamic system performance due to reduced circuit parasitics and eased demands on the system performance evaluation unit. Whereas the preceding USIX 1.0/USIX 2.0 chips provided comprehensive solutions for the sensor interface and addressed various mixed-signal cells within the readout circuit pathway, the present study emphasizes essential components for subsequent USIX chips and offers a deeper exploration of integrating the suggested concepts. The subsequent sections will delve into the technical details of the CFIA, power monitoring modules (PMM), the design of the AAF with the NIS technique, and the complete prototyping chip design.

3.1 Instrumentation Amplifier

The instrumentation amplifier (in-amp) is an essential component of the AFE dedicated to signal conditioning within the amplitude domain of sensor interfaces and readout circuitry [238,239]. In contrast to the operational amplifier (op-amp), distinctive features of the in-amp include its high input impedance and superior common-mode rejection ratio (CMRR), thus establishing it as a prime selection for conditioning weak sensor signals in noisy environments [22]. Additionally, the in-amp facilitates the matching of the DC common-mode voltage V_{CM}, originating from the sensor element to the input common-mode voltage range (ICMR) of the subsequent blocks, which include the AAF and the final ADC stage.

There are three predominant topologies for implementing in-amp circuits [240]: Capacitive Coupling Chopper-Stabilized in-amp (CCIA) [241,242], traditional three op-amp based in-amp, and Indirect Current-Feedback In-Amp (CFIA) [243–245].

The CCIA is the most power-efficient in-amp and uses switching RC coupling circuits to interface AC sensor signals [246]. Hence, it has superior DC input-blocking properties, enabling the CCIA to neglect the offset voltage from sensor electrodes or bridges with rail-to-rail common-mode voltage sensing capability independent of the adjusted closed-loop gain A_{CL}. Therefore, the sensor bridge and readout circuit can be powered by different supply voltages [247]. However, the CCIA input impedance and the ability

to process low-frequency signals depend on the switching-capacitor (SC) resistance at the selected chopping frequency [248, 249]. Unless an input upconversion stage is designed to pass and amplify DC sensor signals [246], the CCIA acquisition bandwidth is limited to processing the signal frequency above the DC level [250]. Moreover, for low-frequency sensor signals in the sub-hertz range, a large time constant RC circuit must be employed [251–253], which again reduces the amplifier input impedance due to the large capacitor at the input stage. A possible but complex solution for increasing the input impedance is to use pre-charge [254] or positive feedback [248] techniques. However, another complexity considered in the design of the CCIA is the need for a filter circuit to remove the spike distortion from the signal baseband due to chopping transition activity [255]. Because CCIAs are inherently chopped, the amplifier offset voltage and low-frequency noise component (flicker noise) are significantly reduced near the thermal noise level [256]. Furthermore, the gain accuracy is high because it relies on ratio matching of the capacitor [248]. Together, this makes CCIA a perfect candidate for interfacing biomedical signals and neural recording systems [253, 257].

The classical and most popular 3-opamps in-amp also has high input impedance with the possibility of directly coupling DC sensor signals, but its disadvantages are due to the power consumption, design area, and high sensitivity of the CMRR to the matching of bridge-feedback resistors, where a net mismatch of 1% yields a worst-case DC CMRR degradation of 46 dB [258]. A conventional approach to achieving a high degree of resistor matching is to use laser trimming technology; however, this increases the chip cost. The primary limitation of this in-amp variant is that its ICMR is inherently tied to the Output Common-Mode Range (OCMR) of the internal amplifiers, depending on the selected A_{CL} [259]. This poses challenges when amplifying small signals with either low or high V_{CM}, as it risks the saturation of the internal amplifiers or caps the maximum gain relative to the common-mode voltage of the sensor signal.

By employing the active feedback amplifier topology [260], alternatively recognized as a Differential-Difference Amplifier (DDF) [261], CFIA has advantages such as high input impedance, significant open-loop DC gain, and expansive bandwidth [238, 262–264]. When compared with the 3-opamp in-amp, the CFIA emerges as more area and power-efficient because of the shared output driver stage among the input transconductance stages [239]. A distinctive attribute of the CFIA is its ability to isolate the common-mode

voltage of the input stage from that of the feedback stage by deploying two balanced differential stages [265]. Consequently, it can directly interface with sensors exhibiting a common-mode voltage that is different from the CFIA output common-mode voltage, without requiring additional isolation or coupling methods [258, 260]. Through the conversion of voltage signals to current signals by the input and feedback transconductance, and the rejection of the common-mode voltage, the CFIA achieves a CMRR superior to the 3-opamp in-amp [245, 249, 266, 267]. Additionally, any mismatch in the feedback resistor influences only the closed-loop gain error, leaving the CMRR performance unchanged [268].

The capability of the CFIA to amplify the sensor voltages near either of its supply rails is contingent on the type of input stage utilized (NMOS or PMOS). This versatility renders the CFIA suitable for conditioning a diverse array of sensors, catering to signal frequencies spanning from the DC to the expansive bandwidth. Such applications include current sensing measurements [269, 270], strain gauges [271], biomedical signal interfaces [268], micro-electro-mechanical system (MEMS) interfaces [272, 273], magnetic field sensor interfaces [250, 274, 275], and electrical impedance spectroscopy (EIS) [228, 276], among others.

Nevertheless, CFIA is not without its challenges. Two primary concerns arise regarding the DDF core amplifier. First, the gain precision is compromised owing to disparities between the input and feedback transconductance [269]. This necessitates the use of differential transistors of the same type, with meticulous attention paid to layout matching during the physical design phase. Employing cascoded biasing currents can further refine the matching, particularly concerning variations in the input common-mode voltage [239]. The second challenge arise from the restricted input differential range of the open-loop configured input transconductance [261]. This limitation becomes particularly pronounced when interfacing with high dynamic range sensors, such as magnetoresistive sensors [277].

Many conventional linearization techniques, elaborated in the literature, aim to augment the input differential range [278, 279]. However, these strategies often entail compromises, deteriorating the amplifier's dynamic attributes, diminishing the ICMR, and increasing power consumption. An innovative approach to counter this challenge was introduced in [280]. This method capitalizes on the merits of fully differential signal

characteristics and employs negative feedback applied to both the input and feedback transconductance stages of the DDF, engendering a virtual short across each paired set, like the op-amp.

To integrate the self-X features, the configuration capabilities of the critical elements of the CFIA circuit, specifically those with a substantial influence on its performance, are embedded. These configurable components serve as design tuning knobs, as illustrated in Figure 3.3, and are denoted by the arrow symbol [281–283]. These elements comprise digitally weighted scalable arrays controlled by the configuration bits derived from the optimization algorithm unit [284–286] after analyzing the CFIA performance. The methodology for selecting sensitive elements is demonstrated in Figure 3.2. This selection is informed by insights gained through comprehensive Monte Carlo and PVT corner simulations including runs from the optimization algorithm around the fixed topology of the CFIA circuit. The range of the tuning knob is determined to ensure that the design satisfies the worst-case conditions.

For the PMOS transistor array, the gate of any unselected transistor is connected to V_{DD}. Similarly, the NMOS array, is connected to GND as shown in Figure 3.4. It is essential to completely deactivate any unselected transistor to prevent any unintended conduction caused by the residual charge retained at the floating gate capacitance.

Under the equilibrium state, the differential output voltage of the CFIA [287] can be approximated as:

$$(V_{out+} - V_{out-}) = \frac{G_{m1} \cdot R_m \cdot K}{1 + \frac{R_1}{R_1+R_2+R_3} \cdot G_{m2} \cdot R_m \cdot K} \cdot (V_{in+} - V_{in-}) + \frac{\Delta G_{m1}}{1 + \frac{R_1}{R_1+R_2+R_3} \cdot G_{m2} \cdot R_m \cdot K} \cdot V_{CM} \tag{3.1}$$

Where R_m represents the current-to-voltage conversion ratio and K is the voltage gain of the driver stage.

Assuming $G_{m2} \cdot R_m$ is high, the closed-loop differential gain (A_{CL}) can be approximated as:

$$A_{CL} = \frac{(V_{out+} - V_{out-})}{(V_{in+} - V_{in-})} = \frac{G_{m1}}{G_{m2}} \cdot \frac{R_{21} + R_1 + R_{22}}{R_1} \tag{3.2}$$

As demonstrated in Equation 3.2, achieving proper matching between the feedback transconductance and the input transconductance, and presuming their equality, the

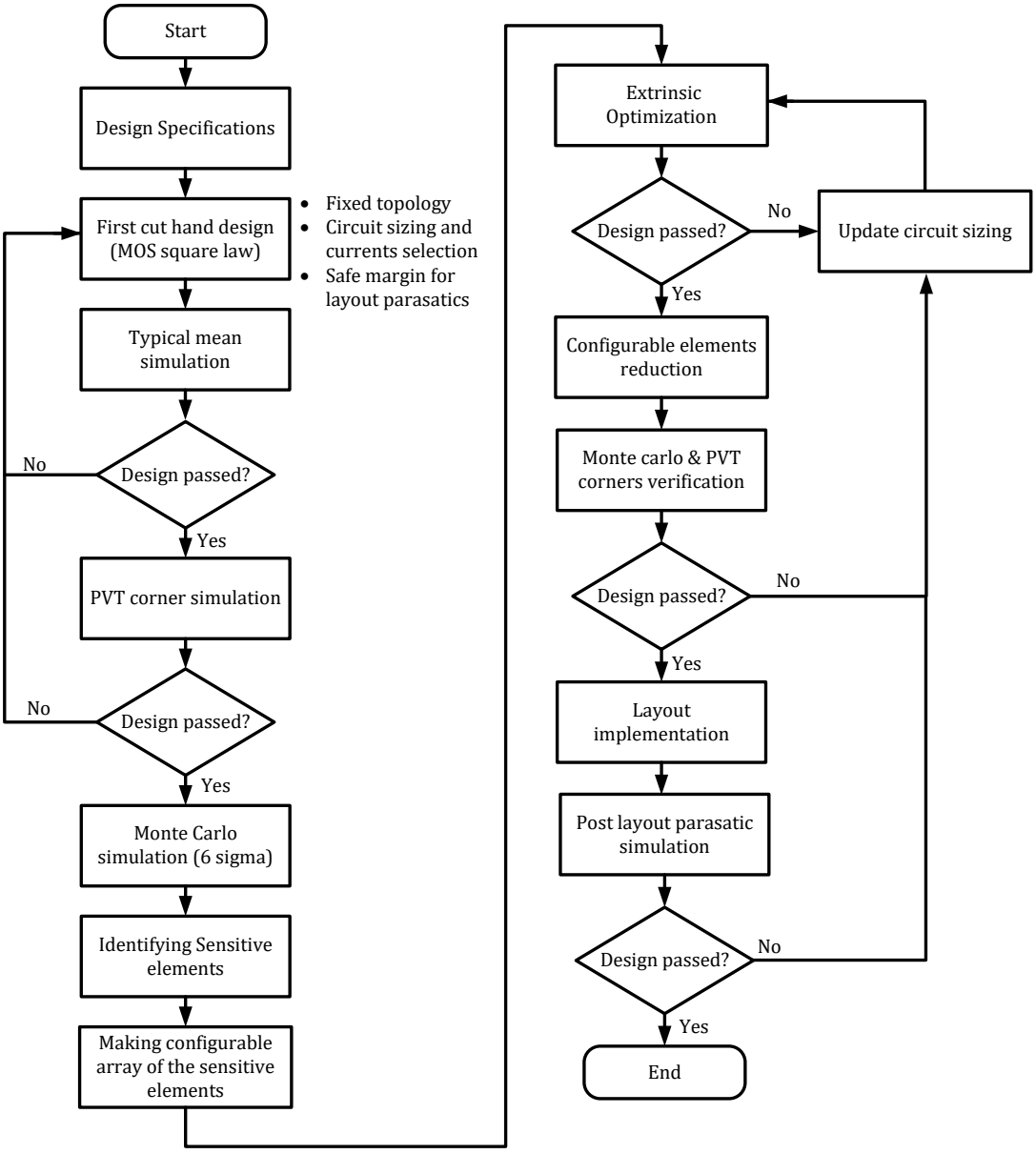

Figure 3.2: Design flow chart for sizing the CFIA.

resulting closed-loop gain is determined solely by the ratios of the resistors.

For configuration storage, hot-swappable 4-row shadow register-based memory is employed to save the configuration pattern and allow dynamic switching between different saved solutions to support in-field optimization. As illustrated in Figure 3.5, a single segment of memory comprises eight bits, representing the fundamental unit cell, and it is basically a serial-in parallel-out register (SIPO). This unit can be cascaded to achieve the desired memory extension. Each segment is equipped with a gated clock circuit to buffer the input global clock signal (GCLK). This design choice mitigates clock-loading effects and ensures data transfer reliability during write and read operation.

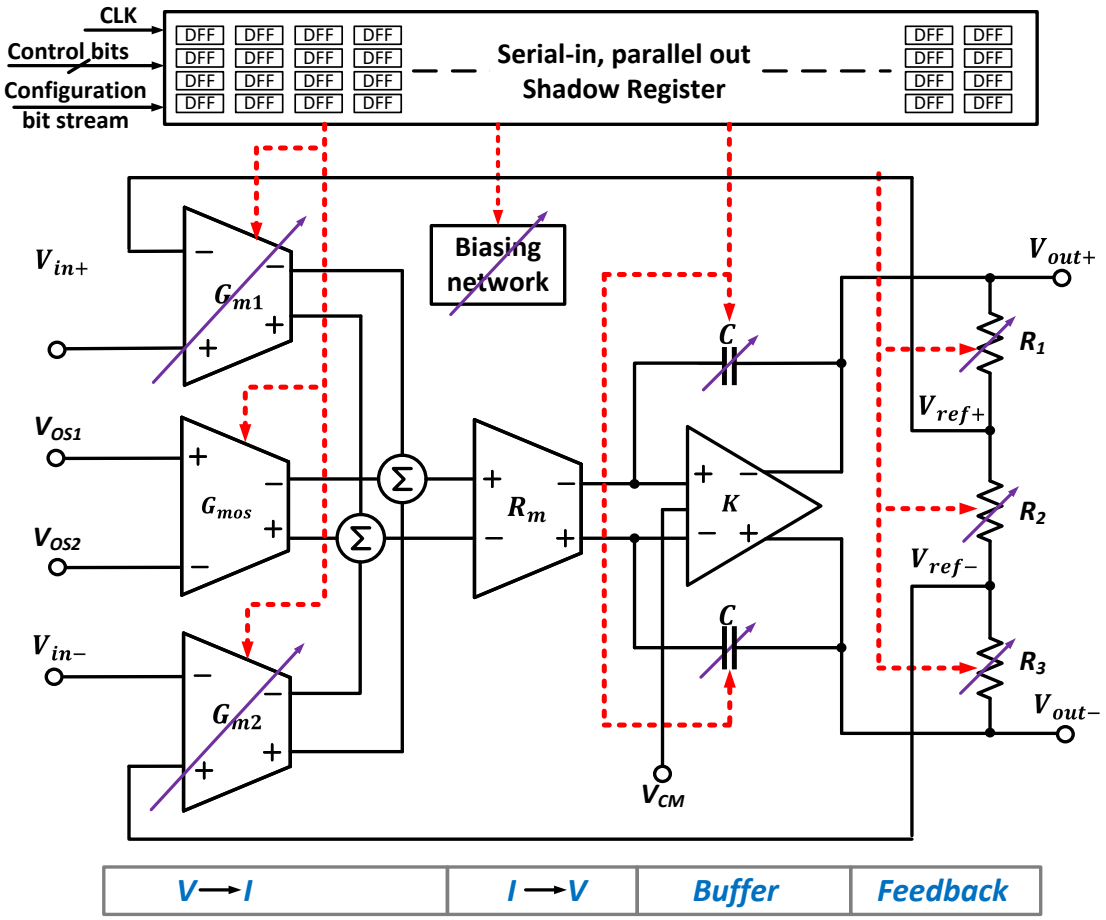

Figure 3.3: A block diagram of the proposed configurable, fully-differential indirect current-feedback instrumentation amplifier (CFIA) for supporting self-X properties.

Within our methodology, the sensitive components of the circuit were singled out based on the simulation data and accounting for PVT variations. The remaining non critical components in the CFIA circuit were fixed to their optimal predesigned values. Our approach offers several advantages over the fine-granular counterpart as stated below:

1. A more compact design footprint;
2. Minimized parasitic effects from switches, thereby enhancing the circuit's dynamic capabilities;
3. Reduced need for configuration memory;
4. Quicker optimization timelines.

The Gain-Bandwidth Product (GBW) of the CFIA typically behaves inversely to its closed-loop gain, mirroring the characteristics of voltage-mode op-amps [288, 289].

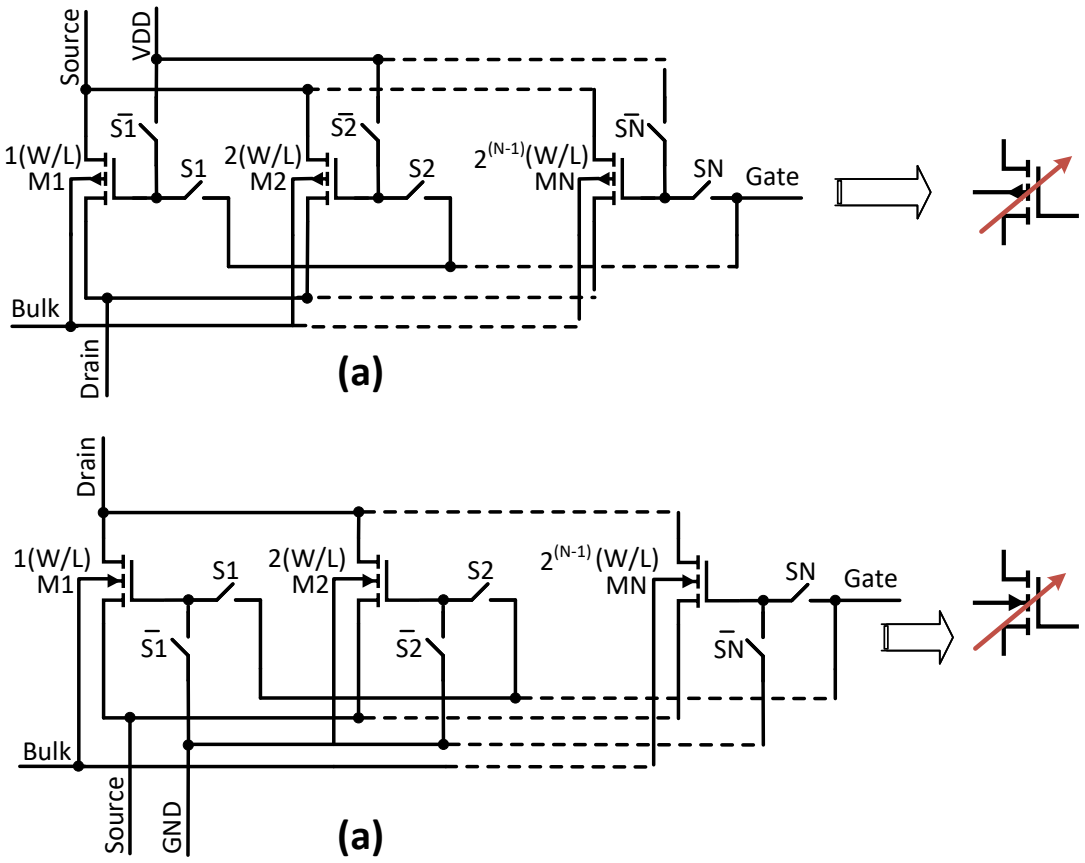

Figure 3.4: Binary weighted configurable MOS transistor array: (a) Configurable PMOS array, (b) Configurable NMOS array.

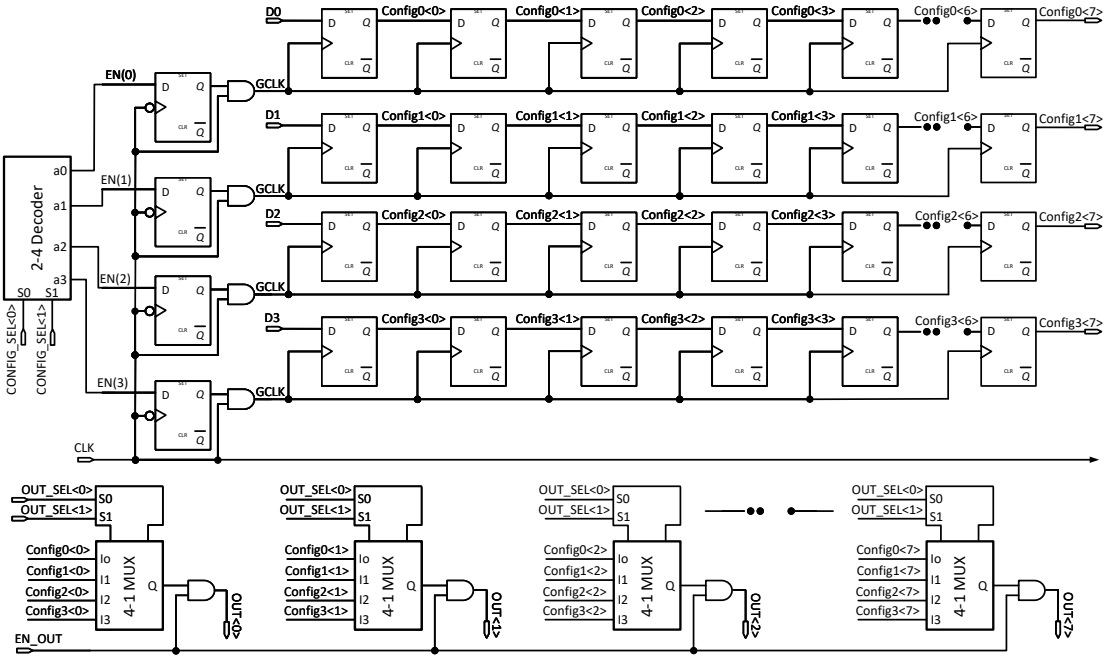

Figure 3.5: 8-bit segment of the shadow register memory for in-field optimization.

This presents a challenge when there is a need to amplify sensor signals that are both weak and have a broad bandwidth. A high GBW is essential in such cases, albeit at the cost of increased power dissipation [263]. An alternative strategy involves compensating the amplifier specifically for higher values of A_{CL} values by using smaller compensation capacitors. This approach can augment both the CFIA bandwidth and slew rate. However, this method may compromise the stability of the amplifier at lower A_{CL} values, particularly in scenarios such as the unity gain buffer configuration, which necessitates the most significant compensation. In the design proposition in [281], a feature for GBW programmability is introduced. This was achieved by reconfiguring the compensation capacitors to ensure stability at the chosen gain with the maximum achievable bandwidth. Flexibility to program the gain across eight distinct levels—1, 2, 4, 8, 16, 32, 64, and 128—is incorporated. Additionally, by adjusting the biasing circuitry, the CFIA cutoff frequency (f_{-3dB}) can be calibrated to reach as high as 250 MHz in post-layout simulation with a unity gain setup or set as low as 0.5 MHz when $A_{CL} = 128$. Furthermore, by programming the biasing current, both the dominant and non-dominant poles of the amplifier can be regulated. This capability is invaluable for restoring the stability of CFIA under unstable conditions.

Figure 3.6 depicts the core components of the CFIA circuit, with a focus on the power monitoring unit (PMM) in detail in the subsequent section. The amplifier employs a buffered class-AB topology as presented in [290, 291]. The design integrates a common-mode feedback amplifier (CMFB) from [292] to maintain the output common-mode voltage of the CFIA close to the desired voltage (V_{CM}). To maximize the output dynamic range, V_{CM} is set to half the supply voltage. Leveraging NWELL CMOS technology, all NMOS transistor bulk connections are grounded, whereas PMOS transistors are tied to V_{DD} unless mentioned otherwise. The power-down scheme is delineated and highlighted in blue. Depending on the transistor type, the gate of the chosen transistor is connected to V_{DD} or G_{ND}, placing the CFIA at zero power consumption (excluding leakage currents) and effecting a full shutdown. This strategy serves two primary objectives: first, to ensure general power conservation when the sensor signal is absent, and second, to ensure safe operation during CFIA configuration, thus preventing potentially harmful transient behaviours. Upon the completion of the configuration stream, the CFIA can resume its normal operational state. The circuit sizing of the CMOS

transistors and passive elements are presented in Table 3.1 and Table 3.2 respectively.

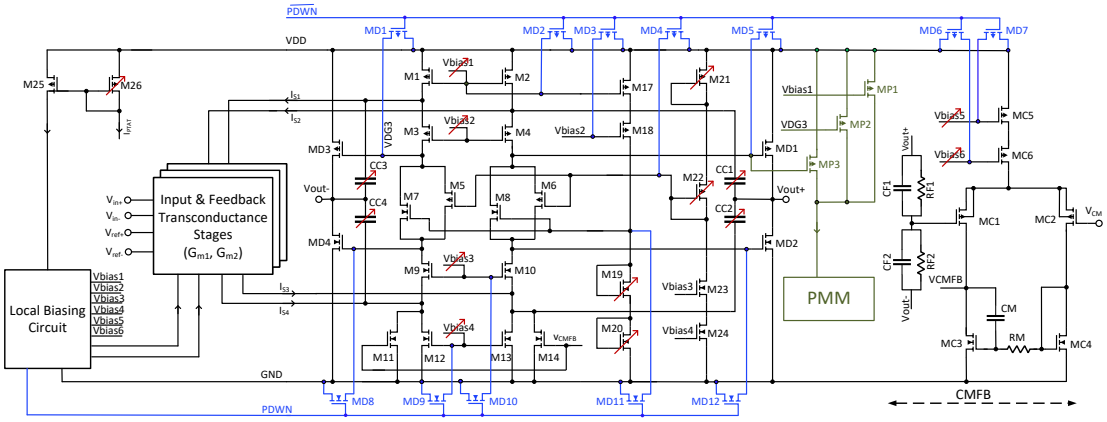

Figure 3.6: Schematic circuit of the proposed CFIA core amplifier.

Transistor NO.	**W (μm)**	**L (μm)**
MD1-MD12	2	0.35
M1, M2	300	1
M3, M4	132	0.7
M5, M6	52	0.55
M7, M8	18	0.55
M9, M10	42	0.7
M11-M14	50	1
MD1, MD3	240	0.35
MD2, MD4	80	0.35
M23	10	0.5
M24	20	1
M17	64	1
M18	32	0.5
M19, M20	7 bits binary weighted; 1-128 (step size 1 μm)	0.5
M21, M22	8 bits binary weighted; 11-256 (step size 1 μm)	0.5
MP1-MP3	1	0.35
M25	20	1
M26	5 bits binary weighted; 120-1055 (step size 10 μm)	1
MC5	256	1
MC6	128	0.5
MC1, MC2	120	0.7
MC3, MC4	20	0.7

Table 3.1: Transistor dimensions of the in-amp core

Component	**Value**
CC1, CC4	4 bits binary weighted (250 fF - 2 pF); step size 250 fF
CF1, CF2	341 fF
RF1, RF2	52 kOhm
RM	78 kOhm
CM	0.5 pF

Table 3.2: Component values of the in-amp passive elements

The tunable input and feedback transconductance, G_{m1} and G_{m2}, are illustrated in Figure 3.7, and the circuit sizing is presented in Table 3.3. This structure offers three selectable stages that are adaptable based on common- and differential-voltage ranges. Stage 1 is suited for situations with high dynamic sensor signals around the CFIA supply midpoint. Stages 2 and 3, which use degeneration resistors, are ideal when the sensor's common-mode voltage is near to V_{DD} or G_{ND}, respectively. Tunability is achieved by programming the biasing current. An additional transconductance stage is incorporated for input offset voltage V_{OS} correction, which is elaborated in the following subsection.

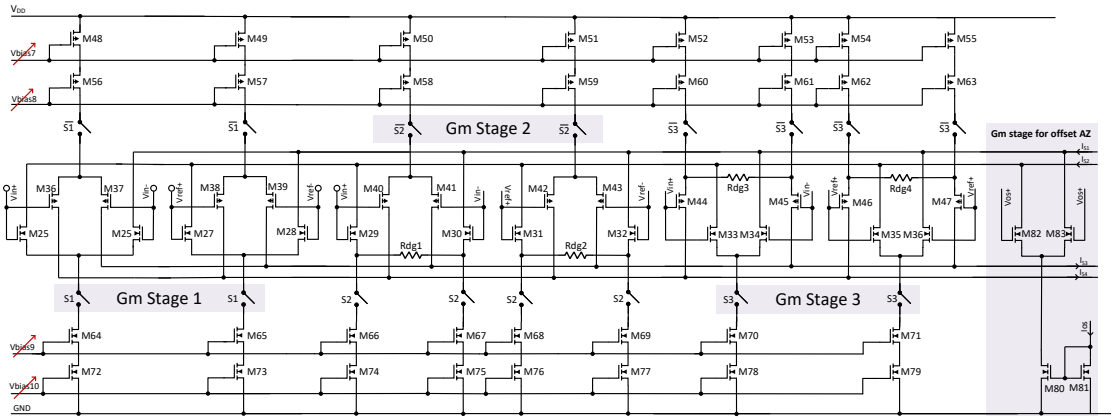

Figure 3.7: Configurable input and feedback transconductance of the CFIA in addition to the offset voltage transconductance stage.

Transistor NO.	**W (μm)**	**L (μm)**
M48-M55	256	1
M56-M63	128	0.5
M36-M47	120	0.7
M25-M36, M82, M83	40	0.7
M64-M71	40	0.5
M72-M81	80	1

Table 3.3: Transistor dimensions of the configurable transconductance of the in-amp

The CFIA circuit is biased using a constant-g_m PTAT (proportional to absolute temperature) current source circuit, as presented in [293]. Figure 3.8 depicts the implementation of a wide-swing cascoded mirror employed to ensure a high power supply rejection ratio (PSRR) and guarantee operation at 3 V. The type of poly resistor was chosen specifically for its temperature coefficient, optimizing the temperature performance of the CFIA. The circuit is engineered to produce a current of 5 µA at the ambient temperature. By mirroring this current, the necessary bias voltages for the CFIA are generated locally. This approach mitigates transistor mismatches between the biasing

circuit and the CFIA, especially when distances span several hundred microamperes between the biasing circuit and the biasing node in the CFIA. The circuit size of the CMOS transistors are presented in Table 3.4.

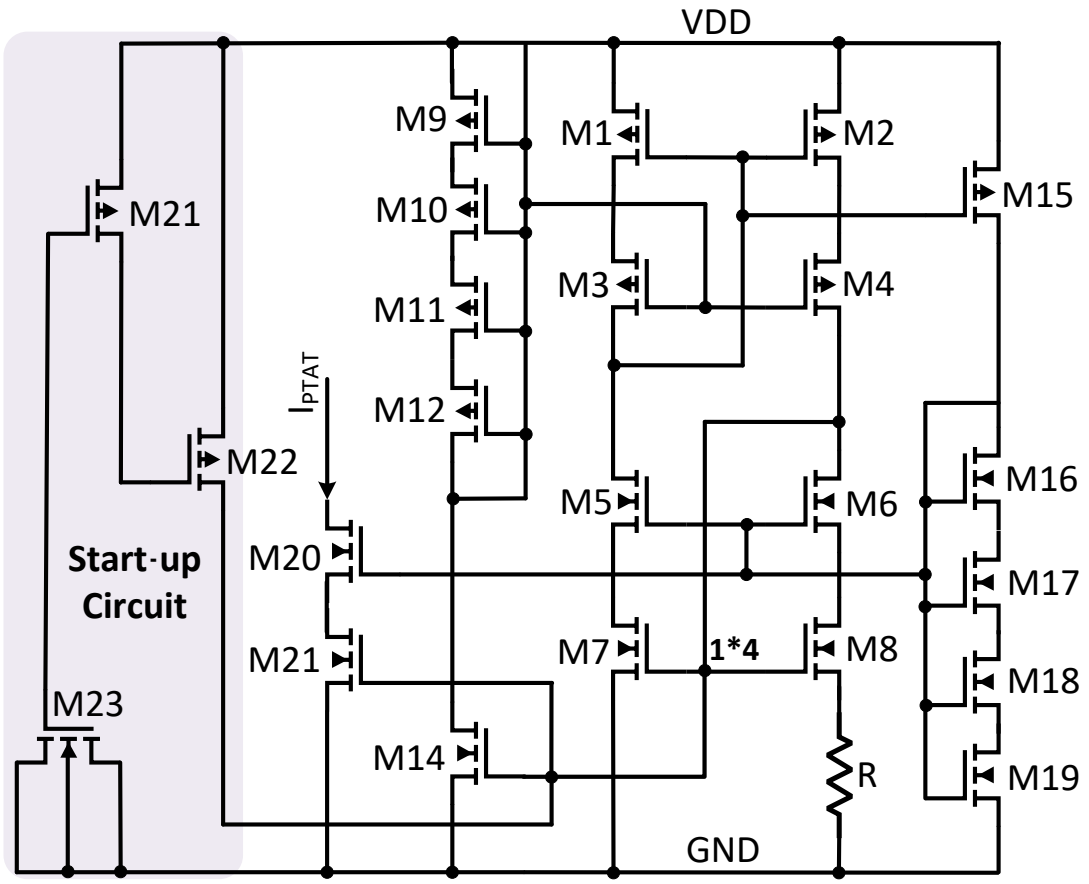

Figure 3.8: Constant g_m PTAT current source used to bias the CFIA circuit.

Transistor NO.	**W (μm)**	**L (μm)**
M1-M4, M15	60	2
M5-M8, M14, M16-M21	20	2
M15	60	2
M8-M12	30	2
M21	2	2
M22	10	0.35
M23	15	15

Table 3.4: Transistor dimensions for the PTAT circuit

3.1.1 Power Monitoring Module (PMM)

The PMM has a dual role: it seeks the most power-efficient solution within the optimization algorithm, ensuring that the power efficiency is optimized in the loop. In addition, it verifies the safety of the optimization pattern for the DUT. Unlike optimization in

programmable digital devices such as FPGAs or feedback networks in amplifiers and filters, core amplifier optimization might yield higher power solutions that meet design objectives. Some optimization risks exceed the amplifier's current density limits at the rails or internal nodes. This can result in supply line voltage drops or even cause significant issues such as electromigration in connectors, which can either lead to immediate chip failure or reduce its reliability. Merely widening the metal to handle extreme currents is not ideal, because it enlarges the layout and adds parasitic capacitors, thereby affecting the post-fabrication performance. In a fixed analog design, the current draw is well-defined and tailored to the design needs. Designers, guided by foundry data books, select the wire widths to maintain safe current densities.

In the realm of printed circuit boards (PCBs), a common approach to measuring circuit current is to observe the voltage drop across a small current-sense resistor (CSR) positioned on the primary supply voltage rail using a differential amplifier and an ADC [294]. The voltage drop on the CSR must not significantly impact the headroom voltage of the circuit, even under high current conditions. Additionally, the AC voltage drop, stemming from dynamic operation causes voltage variations in the CSR at the same operational frequency. Therefore, the PSRR becomes a critical parameter when gauging the amplifier's power at high frequencies using this approach. When adapting this technique to integrated circuits, it is crucial to recognize that it evaluates the power measurement on the main supply rails that may share multiple cells. Therefore, distinct power rings should be implemented to gauge the power usage of the individual cell. In certain scenarios, detecting the power threshold value is vital; however, continuous measurement is not imperative. The authors in [295] proposed a basic method for maximum power detection using a simple current-sense sensor, albeit inadequate for evaluating the power across various optimization solutions.

The advancements in CMOS technology have enabled the integration of on-chip Hall-effect sensors [274, 296, 297]. These sensors serve as an alternative method for high-precision, on-chip current measurements applicable to both AC and DC currents. They provide an output voltage that is proportional to the input current and exhibit excellent linearity. However, they require a dedicated readout circuitry equipped with compensation capabilities for the offset voltage and sensitivity drift with temperature. Additionally, an ADC is required to convert the voltage signal into a digital format.

Notable examples from leading semiconductor foundries include the monolithic devices TMCS1126 from Texas Instruments [298] and MLX91377 from Melexis [299].

In [300], an alternative technique for indirect CFIA DC power estimation is introduced. As depicted by the green components in Figure 3.6, this approach mirrors the scaled-down current values from the power-hungry branches into the current-starved ring oscillator [301], as shown in Figure 3.9. This strategy modulates the current drawn and, consequently, the power dissipation, converting them into clock frequencies. Digital processing within SSEs can conveniently interpret the generated signal. Because the output frequency is proportional to the drawn current, this method not only identifies the power threshold value but also provides a credible approximation of power usage across different optimization solutions. Consequently, the optimization algorithm converges to the most power-efficient solutions from the available search space.

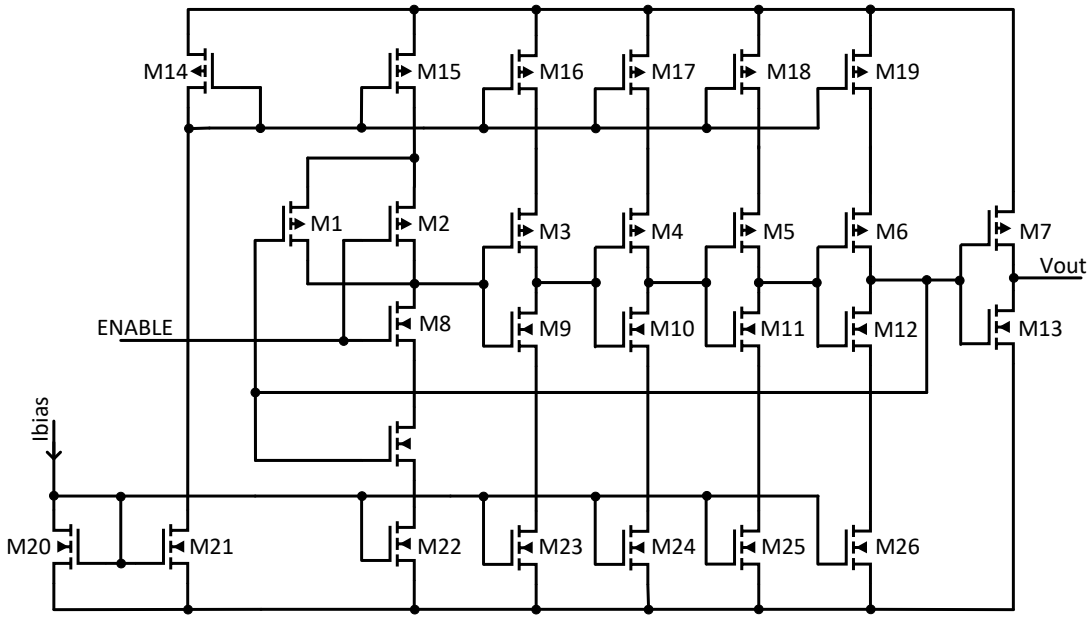

Figure 3.9: Current starved ring oscillator used to modulate the CFIA current in the PMM.

3.1.2 Input-Offset Voltage Autozeroing

The input offset voltage, V_{OS}, determines the amplifier's resolution for recognizing the minimum input voltage within the sensor readout circuit. Additionally, the absolute value of V_{OS} can potentially push the amplifier towards output saturation when a high A_{CL} is selected, consequently diminishing the output dynamic range and reducing the ADC resolution.

The introduction of V_{OS} from random process variations can be reduced through precise matching of circuit elements in the layout using techniques such as common centroid, interdigitating, and dummy devices. Nonetheless, as outlined in the introduction, this static approach fails to address post-fabrication dynamic deviations. Conversely, the systematic V_{OS} from design flaws introduces an irreducible offset error. Even well-designed CMOS amplifiers can exhibit offset voltages on the order of several millivolts. Dynamic circuit levels strategies, such as offset auto-zeroing (AZ) and chopper techniques, cited in [64,302], are increasingly favoured for their ability to dynamically correct offset voltage post-fabrication and compensate for both static and dynamic variations.

The chopper technique [65] operates by transposing low-frequency disturbances such as offset and flicker noise to a higher frequency domain, followed by low-pass filtering to isolate the signal of interest, albeit at the cost of restricting the bandwidth of the amplifier. Although continuous signal processing stands out as a significant benefit of this method, addressing the output signal ripples, which adds to the circuit's complexity, is imperative [265].

The offset auto-zeroing technique employs a two-phase sampling approach, first capturing the offset voltage and then compensating for it in the subsequent phase. This can be implemented in the analog domain by storing the offset voltage on a capacitor, or in the digital domain using shift registers or counters [64].

Analog Auto-Zeroing (AZ) requires frequent refresh periods to restore the voltage of the capacitor and intermittently halts signal processing at the sampling frequency rate. This makes it more suitable for sampled signal processing circuits [303, 304]. For continuous signal processing applications, a potential workaround involves the use of at least two amplifiers in a ping-pong configuration, alternating between the calibration and amplification modes [265]. However, this method introduces spikes in the output signal during amplifier switching [305]. Additionally, charge injection disturbances from non-ideal MOS switches affect the sampling capacitor in the analog AZ. Although optimizing the switch design or refining the AZ topology can mitigate these disturbances, complete elimination remains unavoidable.

Digital AZ [306–313] can save the offset correction on the digital register once at the device power on state and can only be repeated if required. Therefore, it benefits from the continuous signal processing capability and has no charge injection effect.

Our proposed method [281,282] for offset voltage correction is based on the digital AZ and is presented in Figure 3.10. Two 10 bits DACs are used to convert the successive approximation register (SAR) decision into a differential voltage. The additional g_m stage converts the differential voltage into a differential current to balance the offset voltage by compensating the currents in the summing node of the input stage. Long-channel transistors are used in the offset transconductance transistors to extend the input linear range while the biasing current is designed to cope with the offset range. Furthermore, the full-scale voltage of the DAC is defined by the upper and lower level of the reference voltages which is designed to fit the linear range of the differential transistors. As a result, the DAC resolution and consequently the offset voltage resolution will be improved. Furthermore, our proposed scheme supports offset trimming using data provided by the optimization process. This can be achieved by multiplexing the SAR outputs with the optimization pattern supplied by the shadow register as shown in Figure 3.10.

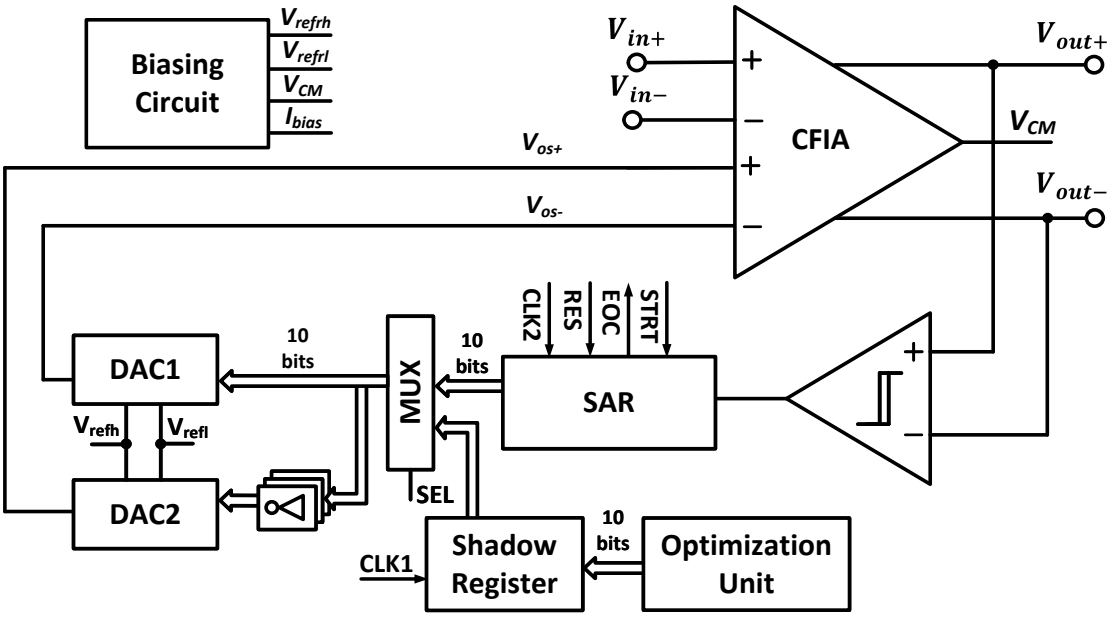

Figure 3.10: Proposed CFIA with programmable and automatic digital offset autozeroing.

During the design, the statistical offset voltage (V_{OS}) of the CFIA was first determined by running the Monte Carlo simulation (MC) with a large number of samples (1000 samples) under extreme voltage and temperature variations. The MC process model is simulated with a 6 Sigma variation to account for the worse-case process profile. The autozeroing circuit is designed and added to the CFIA to cope with the extracted maximum absolute value of V_{OS}). The MC is then repeated because the autozeroing

circuit itself can have its own offset, and it is possible to change the original value of the CFIA V_{OS}. The worst-case corner results of the post-layout MC simulation are shown in Figure 3.12 yields in 99.9% of the V_{OS} falls in the range of ±10 mV. During the calibration mode, the gain of the CFIA is set to the maximum value (128); therefore, the offset voltage of the digital loop control, including both the offset source from the transconductance stage and the comparator will be divided by this value. Figure 3.13 shows the AZ process under the worst two imported statistical samples from the MC run, one for the maximum positive V_{OS} and the other for the maximum negative V_{OS}. Considering the CFIA setup gain, the result proved the offset voltage correction of below 40 μV. A clock frequency of 50 kHz is used to run the AZ and provides sufficient time for the CFIA to settle correctly. The SAR must be reset before starting the next offset calibration process as shown in Figure 3.11.

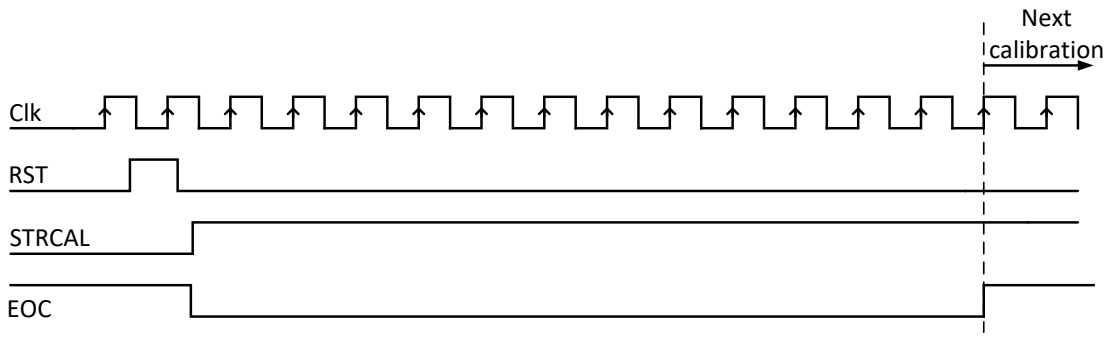

Figure 3.11: Digital offset autozeroing control sequence.

In addition to the automatic circuit, the offset voltage trimming pattern can be externally applied and saved in the shadow register memory. The total number of configuration bits used to program the CFIA is 56 bits, including the offset correction bits.

The physical implementation of the complete CFIA circuit is shown in Figure 3.14, and it consumes a total area of 0.912 mm^2. Symmetry and matching rules are regularly followed in the layout design. Furthermore, the wiring widths are designed to handle the current densities for circuit reliability. Three metal layers are used to complete the layout routing in the cell, whereas the thick metal 4 is reserved for top-level chip routing to the pad frame. The feedback network resistors, compensation capacitors and degeneration resistors are laid out over the NWELL layer to improve the noise coupling immunity from the backside of the P-substrate.

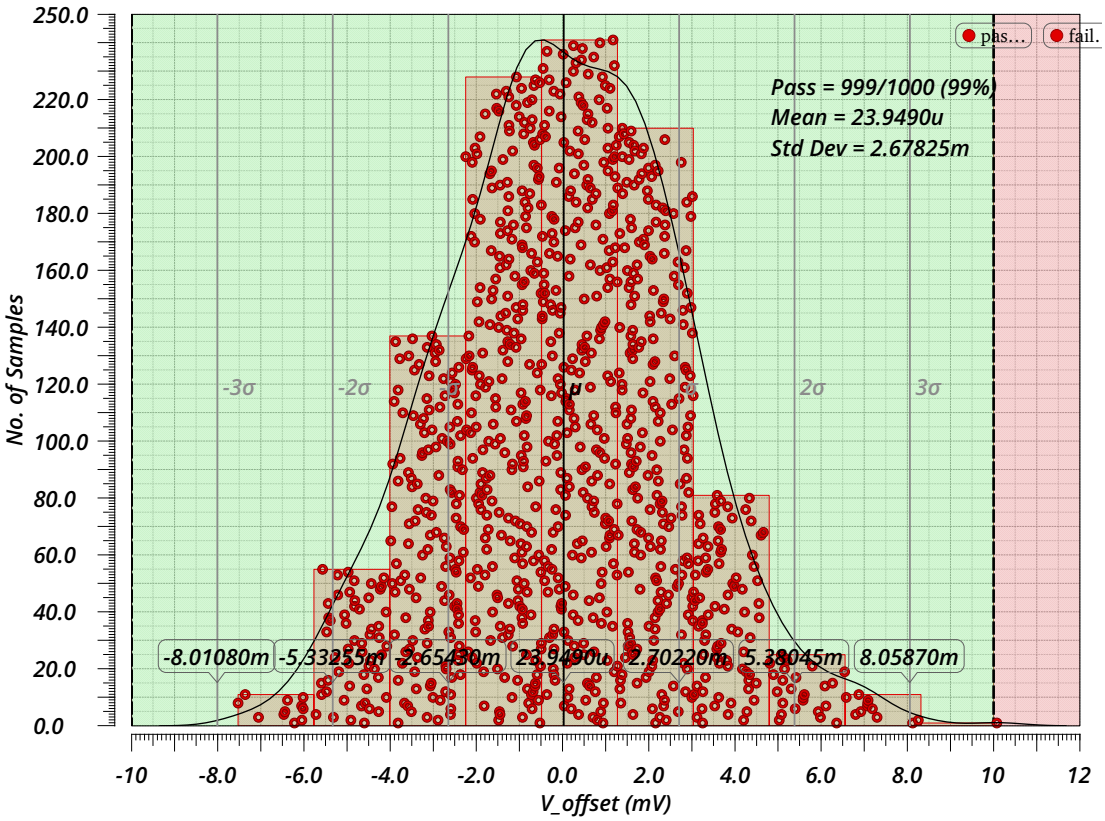

Figure 3.12: CFIA post-layout MC simulation result of the V_{OS} above worst case condition ($V_{DD} = 3.0$ V and $T = -40$ °C).

3.1.3 THD-Based Power-Efficient Indirect Measurement Method

Figure 3.15 illustrates a block diagram showing the proposed methodology designed for a cost-effective, indirect performance assessment within the SSE. This approach employs CFIA, which serves as a test vehicle for intrinsic evaluation. A sinusoidal stimulus with predetermined amplitude and frequency parameters is synthesized by the integrated DAC of the digital optimization unit and is subsequently applied to the CFIA for optimization purposes. Subsequently, the output response of the CFIA is acquired and digitized utilizing the high-speed ADC embedded within the optimization unit. The THD is then computed based on the digitized system response, facilitating a comprehensive prediction of numerous CFIA characteristics, both concurrently and indirectly.

The efficacy of this methodology is based on the understanding that various design imperfections, namely, slew rate (SR), gain-bandwidth product (GBW), input common-mode range (ICMR), effective number of bits (ENOB), full-power bandwidth, and signal-to-noise ratio (SNR) manifest as nonlinear distortions at the output of the closed-loop amplifier. These distortions serve as indicators of the aforementioned imperfections,

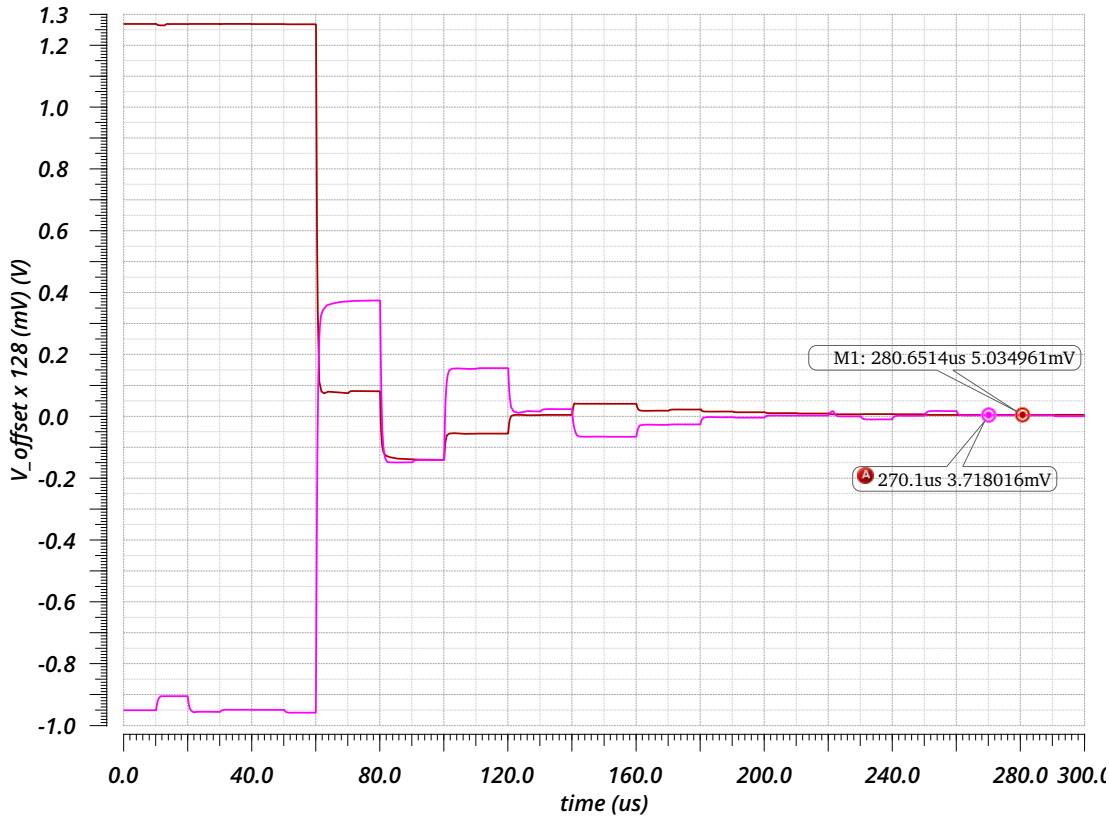

Figure 3.13: Digital offset autozeroing under imported worst statistical corners and CFIA gain equal to 128.

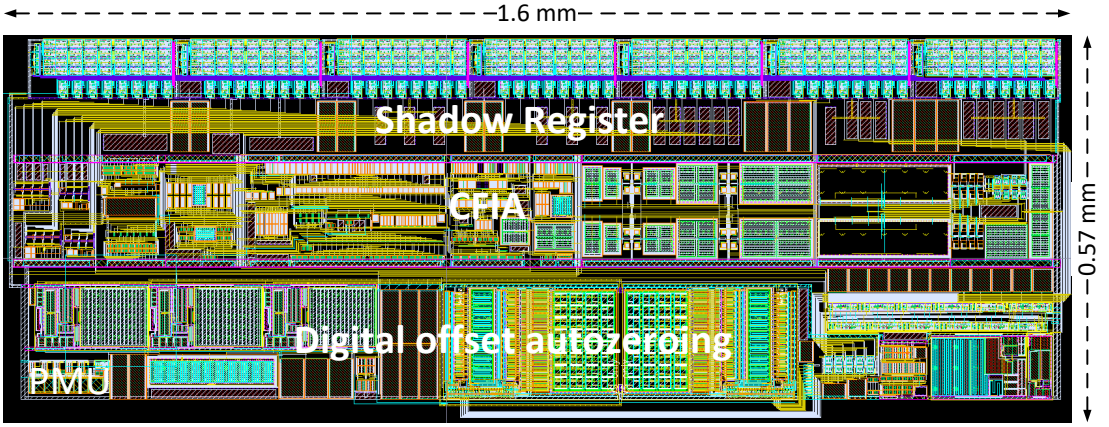

Figure 3.14: The layout design of the CFIA circuit, including the digital offset correction scheme, PMM, and memory.

thereby enabling their assessment and subsequent optimization by computing only the THD value. Furthermore, PMM is incorporated with the THD optimization loop. Finally, the proposed experience replay particle swarm optimization (ERPSO) [314], a modified version of PSO, is chosen as the optimization unit.

The ERPSO algorithm enhances classical PSO by incorporating an experience replay

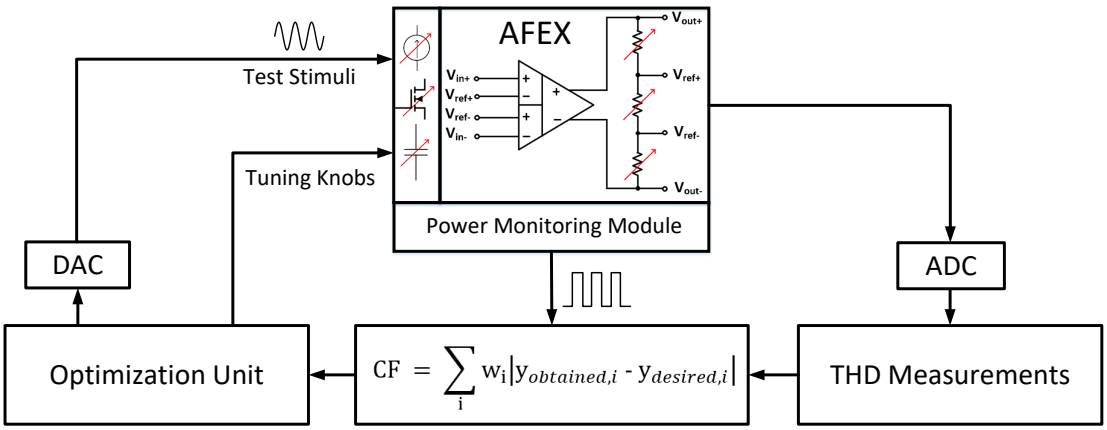

Figure 3.15: Block diagram of the proposed methodology for a power-efficient THD-based indirect measurement method for CFIA in-field optimization.

buffer (ERB), which stochastically selects historical global best positions of particles to navigate complex objective spaces in SSEs, as illustrated in Figure 3.16. The process begins with a random initialization of the particle velocities and positions, followed by the application of a Fast Fourier Transform (FFT) to the output of the reconfigurable CFIA under sinusoidal stimulation. The THD is calculated from the output spectrum, and the power consumption is estimated using the PMM unit. These values serve as fitness functions for the ERPSO algorithm, guiding the update of the personal and global best positions as required. It is important to emphasize that evaluating the impulse response at the conclusion of the optimization process is crucial for verifying the stability of the achieved solution.

3.2 Anti-Aliasing and Anti-Imaging Filter

The second vital component of the AFE chain is the analog filter. Its primary roles are two-fold: first, it acts as an anti-aliasing filter (AAF) for the sensor signal post-amplification, and second, it can handle the significant input impedance load of the ADC. However, an additional dedicated ADC driver may be required when the filter demonstrates an inadequate driving capacity. When an active filter is employed, it offers the potential for post-signal amplification, although the pre-amplifier circuit is often adequate.

Furthermore, the analog filter has two additional applications: it can perform anti-imaging (reconstruction) filtering to smooth out quantized, digitally generated sinusoidal

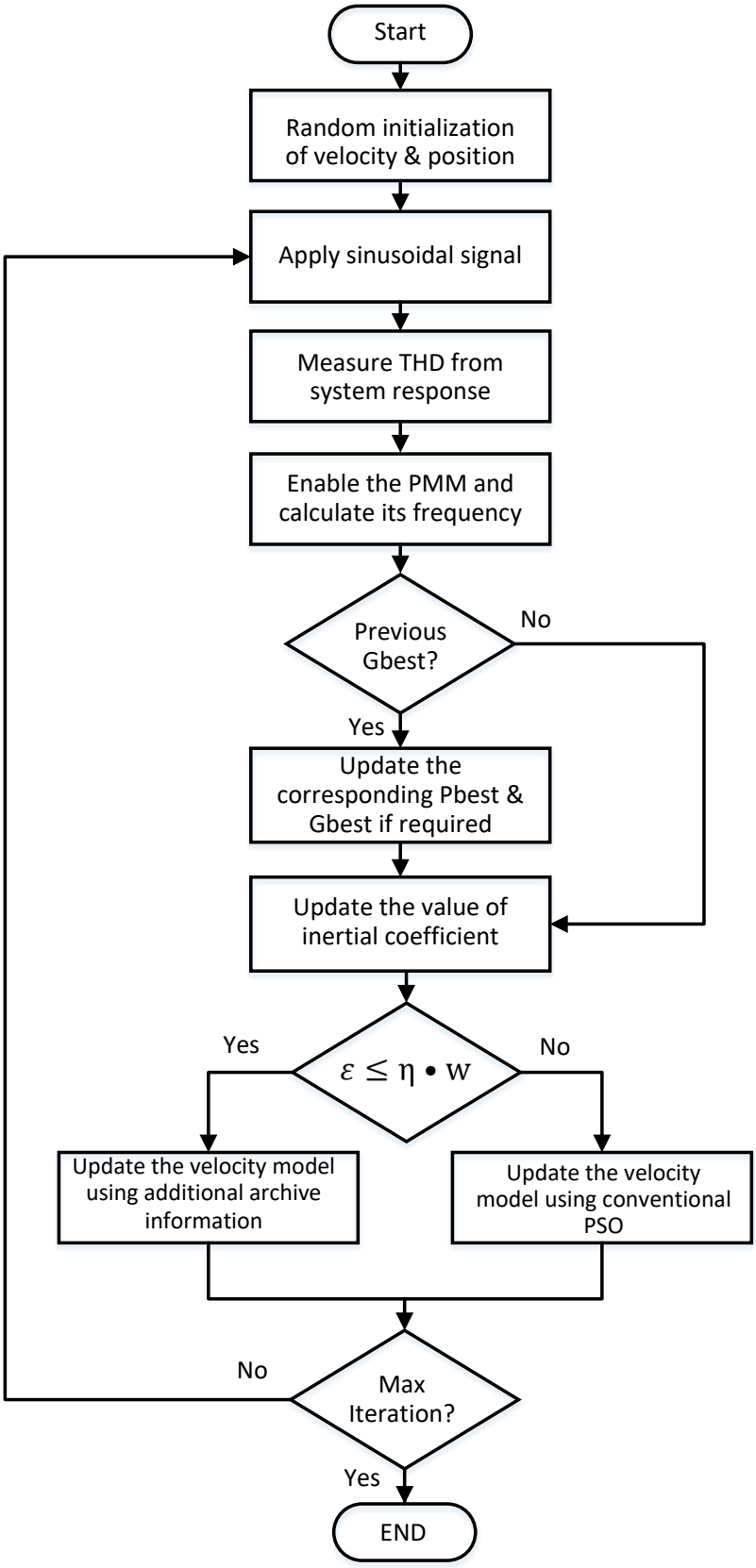

Figure 3.16: Flowchart of the proposed optimization methodology incorporating the ERPSO algorithm, PMM, and THD-based low-cost indirect measurements.

stimuli signals [315,316], which are essential for Electrical Impedance Spectroscopy (EIS) measurements [317–319] and the generation of Built-In Test Signals (BIST) for in-field optimization to support the self-X properties at the chip level [83]. This section delves into the specifics of selecting and designing suitable filter types. It also proposes a novel approach for adjusting the cut-off frequency of the filter across an extensive bandwidth range.

3.2.1 Filter Type Selection

Four key factors guide the selection of an appropriate active filter type for our applications: 1) choice between continuous-time (CT) and switched capacitor (SC) filters; 2) bandwidth tunability, ensuring precise and stable quality factor settings over a broad range, which is essential for EIS applications; 3) sufficient linearity to accurately reconstructing sinusoidal stimuli signals, especially in the range of 500 mV_{p-p} or higher; and 4) considerations of area and power consumption. Given that the designed in-amp is of the CT type, CT filters are favored to avoid clock interference commonly associated with SC filters [320].

Three prominent methods for implementing active CT monolithic programmable filters are active RC, MOSFET-C, and transconductance-C (G_mC) filters. Active RC filters excel in linearity when handling large swing signals, owing to their utilization of closed-loop negative feedback amplifier circuits combined with linear passive elements (R and C), which define the filter's transfer function [292, 321]. The magnitude of the loop gain, representing the difference between the open-loop gain and the desired closed-loop gain of the amplifier circuit, should be sufficiently high at the operational frequency to ensure a linear transfer function governed by the feedback elements [322]. Additionally and more importantly, considering the gain frequency response peaking due to the filter quality factor (Q), the minimum requirement for the GBW can be expressed as [323,324]:

$$GBW \geq \kappa \cdot f_c \cdot A_{CL} \cdot Q, \qquad \kappa : 8 \text{ to } 100 \tag{3.3}$$

where f_C is the filter cutoff frequency.

Designing CMOS op-amps/in-amps with a higher GBW presents a challenge because it requires increased power consumption, thus imposing an upper limit on the design.

Bandwidth tunability can be achieved by employing a scalable resistor and capacitor banks, allowing discrete adjustments with finite resolution. However, fine-tuning requires extensive banks with small unit components [325]. A significant issue arises when the on-resistance of the MOSFET selector switches and its parasitic capacitors dominate the primary RC feedback elements. This dominance adversely affects the filter linearity and alters the transfer function [326, 327].

A higher GBW is a design challenge in CMOS op-amps/in-amps and requires a higher power consumption. Therefore, it sets the upper design constraint. Because f_C is defined by the RC time constant, bandwidth tunability can be achieved using banks of scalable resistors or capacitors, thereby providing discrete tunability with finite resolution. Fine-tuning implies the use of large banks with small unit sizes [325]. Besides the chip area, a problem arises for the small R and C values when the on-resistance of the MOSFET selector switch and the parasitic capacitors becomes dominant over the main RC feedback elements, degrading the filter linearity and shifting the filter transfer function [326, 327]. For EIS applications requiring a low cutoff frequency (f_C) of just a few hertz, utilizing a scalable resistor and capacitor banks becomes impractical due to the need for excessively large passive components. This is unfeasible for integration, even with current semiconductor technologies that support poly-silicon resistors with extremely high sheet resistance.

In contrast, transconductance-C (G_mC) filters are open-loop integrators based on un-buffered operational transconductance amplifiers (OTAs) that facilitate operation at higher f_C values with reduced power and area requirements, albeit at the cost of signal amplitude linearity [292, 320, 322]. The f_C of these filters is set by the OTA's open-loop transconductance (g_m) and feedback capacitors, making them more susceptible to circuit parasitics than the active closed-loop filters [328]. Frequency tuning can be achieved using arrays of scalable transconductances and capacitors, with continuous tuning possible by adjusting the transconductance biasing current [137, 329].

Linearization techniques are crucial for enhancing the linearity and expanding the dynamic range of G_mC filters to process larger signals [315, 330]. However, these filters may suffer from performance degradation across the tuning range [331], which is a significant concern for achieving the wide tunable frequency range essential for high-quality EIS.

Authors in [228] identified practical limitations due to the use of (G_mC) filter. They accomplished improved results by using MOSFET-C filter replacement based on a closed-loop op-amp, where a tunable range of (5 Hz-3.5 MHz) is achieved [317] using digitally weighted MOS resistors and by controlling the gate voltage of the transistors [332]. However, MOSFET-C filters still suffer from non-linearity distortion owing to the limited linear range of the MOS resistance and the resistance variation resulting from the interpretation of v_{gs} with the input signal amplitude. Therefore, the MOSFET-C filter is more suitable for processing small signals [327], which requires post-amplification to the ADC full-scale voltage. This thesis emphasizes the work on MOSFET-C to attain a wide tunable range and improve the linearity issue. The remaining considerations for the filter design are the filter circuit structure, transfer function approximation, and filter order, which are covered in the next subsection.

3.2.2 Proposed Filter Design

The multiple-feedback (MFB) filter topology provides a straightforward approach for constructing active low-pass R/MOSFET-C fully differential filters [317,333]. This topology is well-suited for filters with a fixed bandwidth. However, achieving variable (f_C) is challenging because tuning the frequency independently from the filter quality factor and amplifier gain is difficult due to their interdependence.

Alternatively, the Tow Thomas filter topology [334] allows for possible f_C tunability; however, it requires two op-amps per biquad and additional feedback elements, leading to higher area and power consumption.

The Sallen-Key topology, with equal network resistors [324] offers a more flexible frequency tunability and fewer feedback elements than both the MFB and Tow Thomas topologies. However, a fully differential implementation requires either two single-ended op-amps per biquad [335] or a single differential amplifier with a modified network [336], with the latter being more complex in terms of tunability and using more feedback elements.

In this thesis, a 4^{th} order tunable, fully-differential Sallen-Key low pass filter [337], based on the non-inverting fully-balanced differential-difference amplifier (FB-DDF), is introduced, as illustrated in Figure 3.17 [283, 338, 339]. This circuit comprises two biquads, each with a unity gain buffer amplifier. The buffer configuration has several

advantages. First, it ensures precise gain settings owing to the larger loop gain. Second, it demands a lower GBW per biquad, as described in Eq. 3.3. Third, the input offset voltage (VOS) minimally affects the output, obviating the need for an additional offset calibration circuit. Finally, it offers a reduced closed-loop output resistance, which is essential for the Sallen-Key architecture, thereby enhancing the filter performance in the high-frequency attenuation band [340].

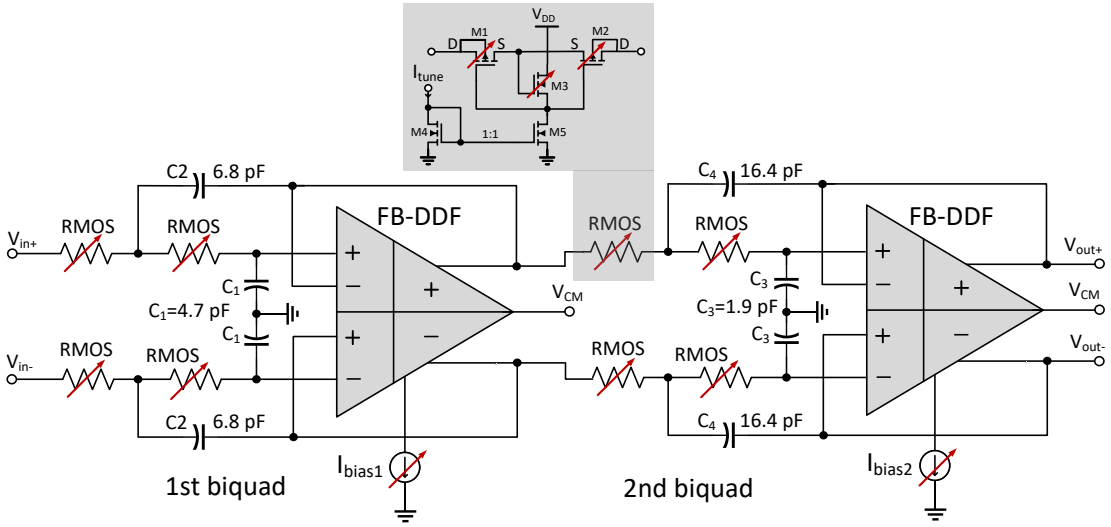

Figure 3.17: Proposed active fourth-order fully differential and programmable Sallen-Key low-pass filter with Butterworth characteristics.

Utilizing the filter design coefficients from [324], the capacitor ratios in each biquad fix the quality factor of the filter. This method is employed to achieve a Butterworth approximation, as detailed below.

$$Q_1 = \frac{1}{2}\sqrt{\frac{C_2}{C_1}} = 0.5412 \tag{3.4}$$

$$Q_2 = \frac{1}{2}\sqrt{\frac{C_4}{C_3}} = 1.3065 \tag{3.5}$$

The cutoff frequencies for the individual biquads are determined as follows

$$f_{C1} = FSF \cdot f_C = \frac{1}{2\pi R\sqrt{C_1 C_2}} \tag{3.6}$$

$$f_{C2} = FSF \cdot f_C = \frac{1}{2\pi R\sqrt{C_3 C_4}} \tag{3.7}$$

where FSF is the frequency scale factor, for Butterworth approximation FSF=1.

Given that the quality factor is defined by the ratios of capacitors rather than their absolute values, achieving a stable Q is feasible through careful matching of the layout. As indicated by the equations, (f_C) can be adjusted by varying only the resistor values without affecting Q.

The Butterworth approximation, which is known for its favourable amplitude and impulse response, makes this filter particularly suitable for EIS and sensor readout circuits, particularly for conditioning sensor signals with pulse-like characteristics. In contrast, while offering a sharper transition region, the Chebyshev approximation introduces ripples in the passband and more pronounced ringing in the impulse response. However, for EIS measurements, which involve discrete single-frequency sinusoidal signals, passband ripples, and impulse response ringing are not significant concerns [316]. Nevertheless, the complex coefficient requirements for the Chebyshev approximation and the associated higher power consumption due to increased Q make it a less desirable choice for the proposed circuit design. Consequently, and for the same reason, higher-order filters are not recommended in this work.

To enhance the filter linearity, the design incorporates a linearized high-value tunable bulk-drain connected MOS floating resistor adapted from [341], as shown in Figure 3.17. Furthermore, our approach utilizes scalable MOS arrays for adjustable spans, offering flexibility in tuning current (I_{tune}) requirements. Connecting multiple units in series increases the resistance and improves linearity by reducing the v_{sd} dependency, as discussed in [342]. However, the proposed configurable resistor design leads to increased parasitics in the filter network, thereby affecting the filter response.

Initially, smaller filter capacitors were selected. However, the interaction between the amplifier's input capacitance and the parasitic capacitance of the MOSFET resistors, which is particularly noticeable after layout implementation, necessitated iterative adjustments. Both the capacitance values and the quality factor (Q) were consequently increased following the procedure outlined in [324].

The design uses two equal and grounded capacitors ($C_{1,2}$) instead of differentially half-sized connections. This choice is due to the unequal parasitics of the top and bottom plates, as noted in [37,343], which results in better common-mode rejection and stabilizes the CMFB loop of the amplifier [322].

The core amplifier in the filter is similar to that used in the in-amp design. However, the input and feedback tail currents are not cascoded to meet the higher current requirements for the desired Gain-Bandwidth Product (GBW). This modification does not affect the ICMR performance, because the ICMR for the filter is predetermined by the common-mode voltage from the in-amp output to half of the supply voltage. To further reduce the amplifier's output resistance, the output transistors are designed with a minimum channel length and high biasing current. This approach also reduces transistor capacitance and enhances amplifier stability with fewer compensation capacitors. The biasing currents of the biquads ($I_{bias1,2}$), and consequently the GBW, are tunable according to the selected f_C. This allows for energy savings during low-frequency operation, with the maximum GBW achievable up to 270 MHz.

The PTAT circuit used in the in-amp is also employed to bias the core amplifiers of the filter. However, the MOS resistors exhibited a proportional change in temperature. While the resistor biasing current is adjustable and can compensate for temperature variations, incorporating a Complementary to Absolute Temperature (CTAT) current source, as depicted in Figure 3.18, provides an advantageous degree of self-compensation. The CMOS transistor sizes are listed in Table 3.5.

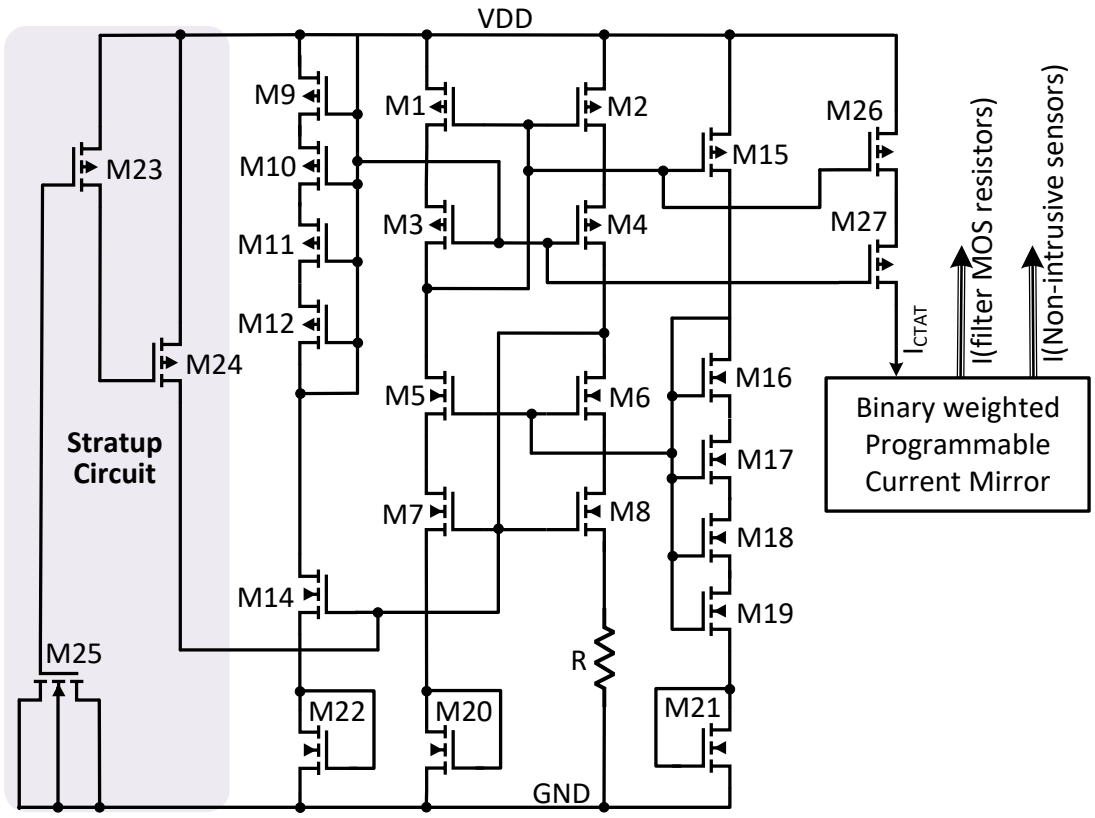

Figure 3.18: CTAT biasing circuit used to generate the tunable current of the MOS resistors and NIS in the filter

Transistor NO.	**W (μm)**	**L (μm)**
M1-M4, M15	60	2
M5-M8, M14	20	2
M20-M22	80	1
M16-M19	10	2
M23	10	1
M24	10	0.35
M25	14	14

Table 3.5: Dimensions of the CTAT circuit transistors.

The physical design of the filter is fully customized and is depicted in Figure 3.19, occupying an area of 0.7991mm^2 including the area of the shadow register. 32 bits are used to program the filter. Adhering to layout matching rules and symmetry, the design preserves the benefits of fully-differential signal properties, mirroring the approach used in the in-amp design.

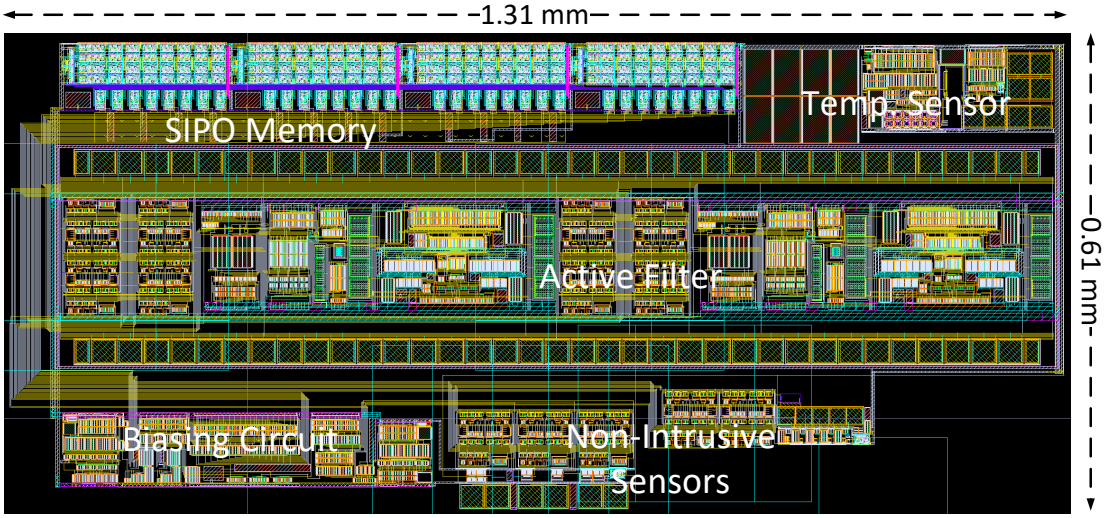

Figure 3.19: Physical implementation of the proposed filter.

Figure 3.20 displays the gain response of the proposed filter, showing variations in response to different MOS resistor weights and adjustments in I_{tune} from 100 nA to 30 µA, in increments of 100 nA. This adjustment allows the f_C to span from 30 Hz to 10 MHz. In the achieved bandwidth range, the MOS resistor functions as a variable resistor with a range of 4 kΩ to 900 MΩ.

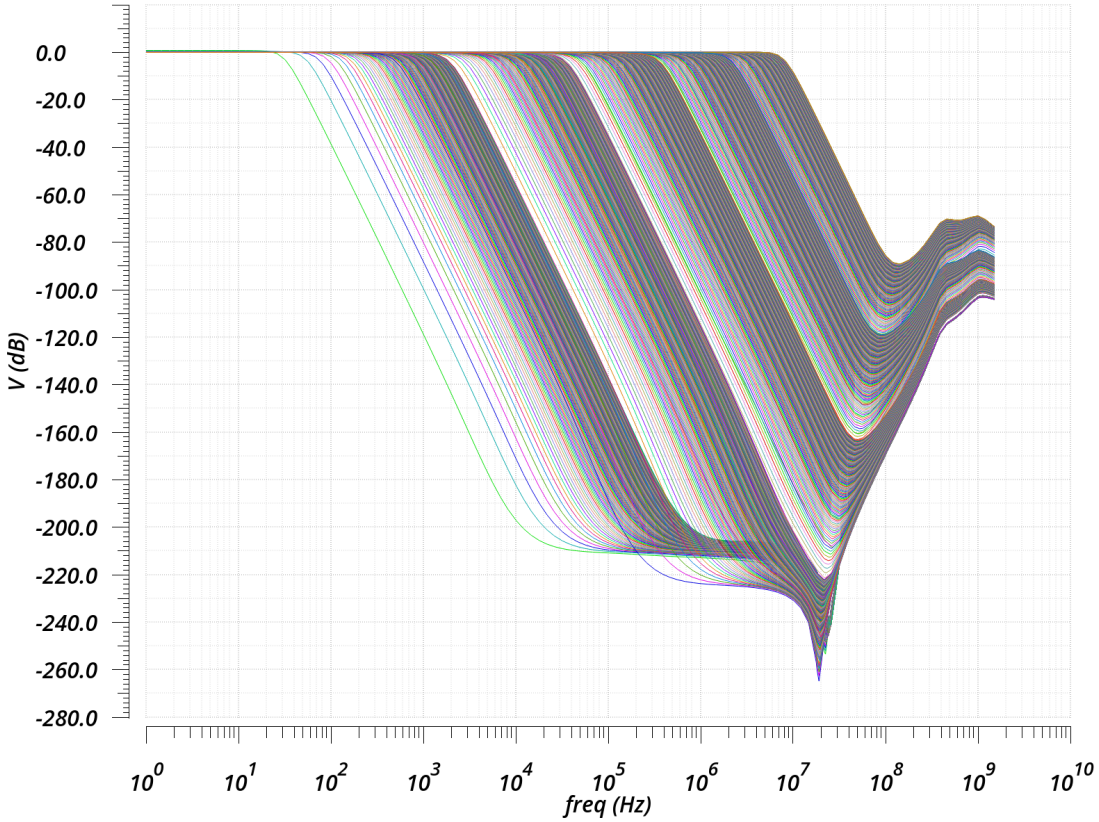

Figure 3.20: Post-layout simulation results representing the gain frequency response of the proposed filter.

The filter exhibits a total harmonic distortion (THD) of 0.55% with a 1 v_{p-p}, 1 MHz input signal. The filter stability is assessed using a step signal, and the output response is illustrated in Figure 4.36. Contrary to the typical Butterworth approximation with a higher overshoot, this filter experiences a mid-transfer function drop due to parasitic feedback stage effects, resulting in a roll-off drop to -70 dB/decade instead of -80 dB/decade. Table 3.6 summarizes the performance of the designed filter under nominal conditions. The robustness of the design against process, voltage variations, and industrial temperature range (-40 °C to 85 °C) has been validated.

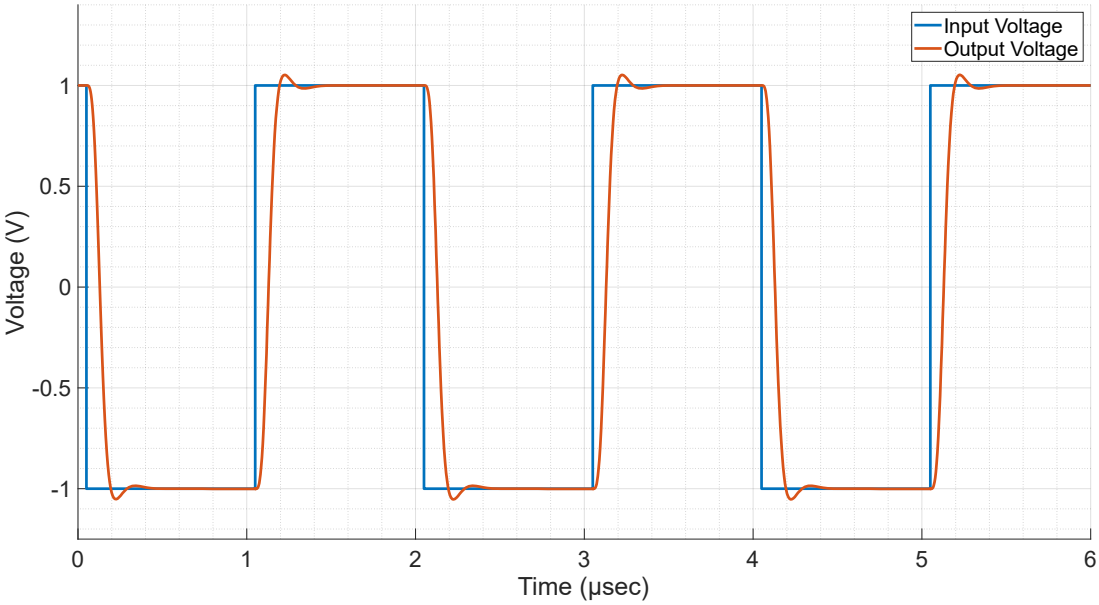

Figure 3.21: Post-layout simulation results representing the pulse response of the proposed filter.

Table 3.6: Post layout performance of the proposed filter, $V_{DD} = 3.3\,V, V_{CM} = 1.65\,V, T = 27\,°C$.

Parameter	**Value**
DC gain	0 dB
Power dissipation	≤ 60 mW
Total harmonic distortion (THD) @ $V_{ID} = 1V_{P-P}, 1$ MHz	0.55 %
Stop band rejection	-70 dB
Lower f_C	30 Hz
Upper f_C	10 MHz

3.2.3 Indirect Measurement Approach for Filter Tuning

Our proposed methodology [344] for tuning the filter bandwidth leverages indirect measurement techniques (IMs) utilizing non-intrusive sensors (NIS) [345, 346] for infield optimization. These NIS, which function as basic PVT monitors based on ring oscillators [215, 347, 348], are positioned near the DUT, the filter in this case to experience identical PVT conditions. The Key characteristics of these sensors include their compact

size and simplicity of interpreting their quasi-digital signal output. The standard IMs strategy, which employs a regression model to predict filter performance, is integrated with a metaheuristic optimization algorithm for the adaptable NIS. Two types of ring oscillators are designed, sharing the same MOS resistors, tuning currents, and capacitor types as the filters, as depicted in Figure 3.22.

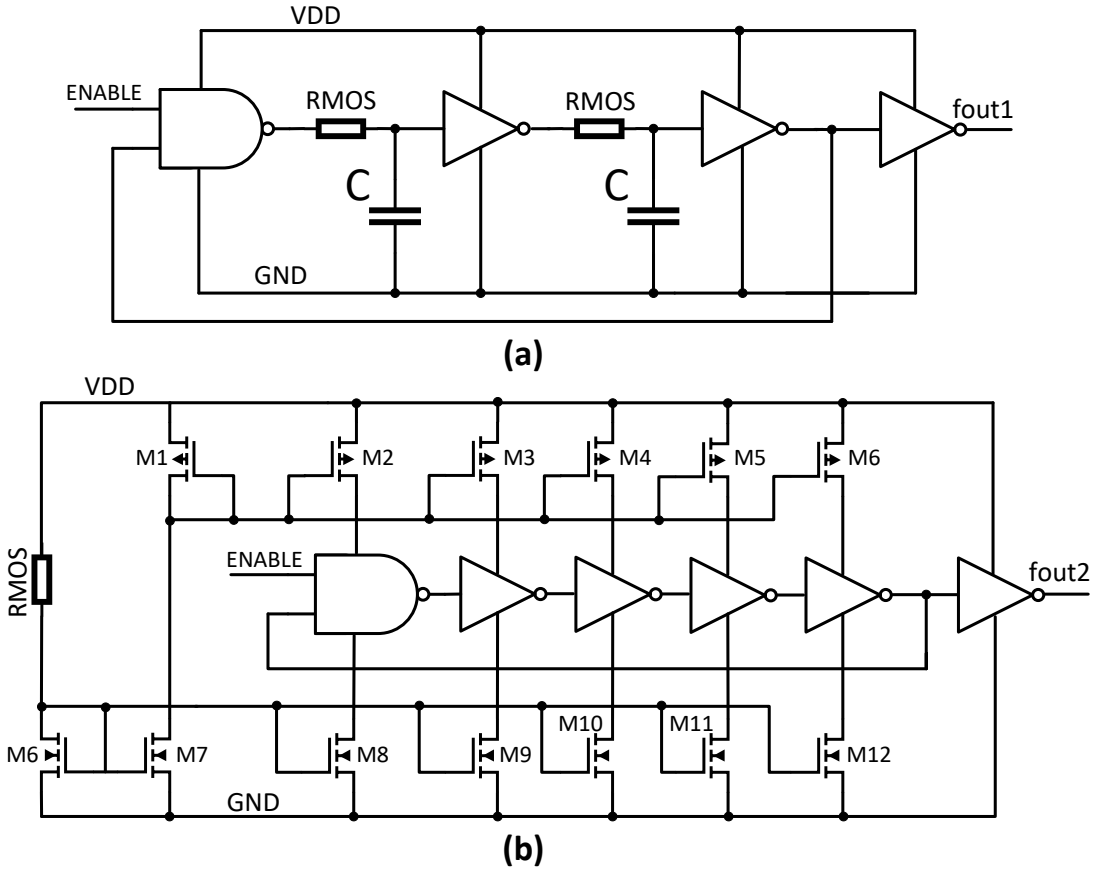

Figure 3.22: Non-intrusive sensors based on (a) ring oscillator and (b) current starved ring-oscillator.

Figure 4.43 illustrates the designed CMOS temperature sensor (TS) [349], which outputs a quasi-digital signal. This TS is pivotal for adjusting the filter in response to temperature changes and monitoring the die temperature for safe operation. The TS comprises two primary components: a temperature-sensing core (TSC) and current-controlled oscillator (CCO). The transistor sizes are presented in Table 3.7 and the physical implementation is depicted in Figure 3.24 with a total area of $0.0287\,mm^2$.

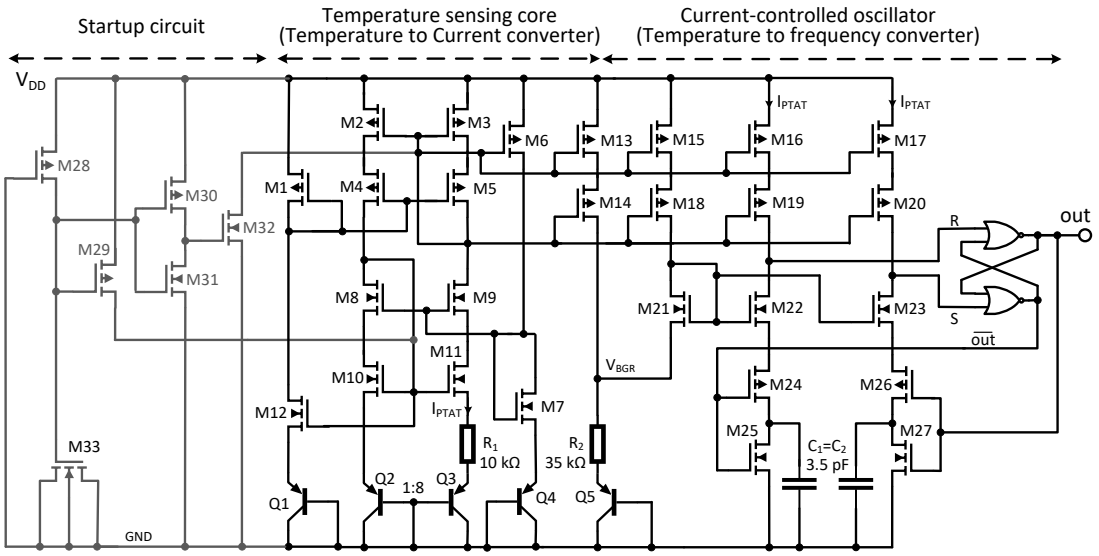

Figure 3.23: Schematic design of the proposed CMOS temperature sensor with quasi-digital output signal.

Transistor NO.	**W (μm)**	**L (μm)**
M1-M20	60	2
M8-M12, M21-M23	20	2
M24, M26	6	0.35
M25, M27	2	0.35
M28	0.5	24
M23, M29	5	0.35
M30	2	0.35
M31	1	0.35
M33	30	30

Table 3.7: Transistor sizes of the temperature sensor.

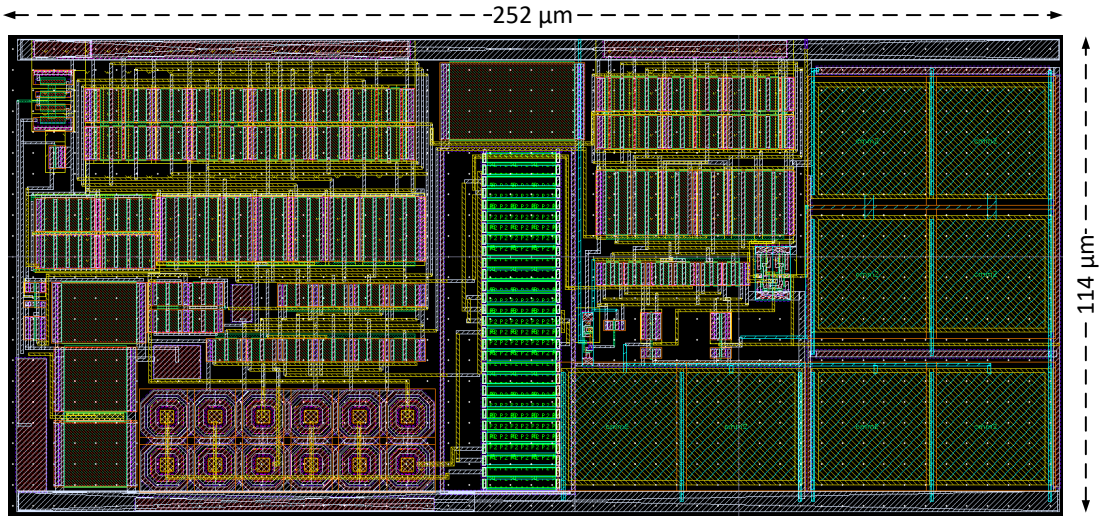

Figure 3.24: Physical design of the proposed CMOS temperature sensor with quasi-digital output signal.

The TSC, functioning as the central element, transforms the temperature into a current by exploiting the highly linear ΔV_{BE} PTAT current reference of the parasitic Bipolar Junction Transistors (BJTs) in CMOS technology. In turn, the CCO converts this temperature-dependent current into frequency.

The heart of the TSC is the bandgap reference circuit (BGR). This circuit not only generates a PTAT current (I_{PTAT}) but also produces a reference trigger voltage (V_{GR}) for the current comparator in the CCO stage. The I_{PTAT} is then mirrored into the CCO, which emits a quasi-digital signal. This signal translates the temperature variations into frequency changes while maintaining a consistent duty cycle of 50%. To enhance the current matching and achieve a high power supply rejection ratio (PSRR), the BGR circuit incorporates wide swing cascode mirrors (M1-M12), requiring only two additional BJTs (Q1, Q4). This design choice effectively balances the performance with component minimization.

The PTAT current is determined by [350]:

$$I_{PTAT} = \frac{V_{BE2} - V_{BE1}}{R_1} = \frac{V_T \cdot \ln(m)}{R_1} \tag{3.8}$$

where V_T is the bipolar thermal voltage, and m represents the size ratio between transistors Q3 and Q2. In this design, the value of m is fixed at eight The temperature coefficient (TC) of the generated PTAT current can be derived as:

$$TC\left(I_{PTAT}\right) = \frac{1}{I_{PTAT}} \cdot \frac{\partial I_{PTAT}}{\partial T} \tag{3.9}$$

$$TC\left(I_{PTAT}\right) = \frac{1}{V_T} \cdot \frac{\partial V_T}{\partial T} - \frac{1}{R_1} \cdot \frac{\partial R_1}{\partial T} = TC\left(V_T\right) - TC\left(R_1\right) \tag{3.10}$$

The first term of equation 3.10 exhibits a positive TC of approximately (0.086mV/°C). To augment the TC of (I_{PTAT} and consequently boost sensor sensitivity (($S = \frac{\partial I_{PTAT}}{\partial T}$)), a sheet resistor with a more pronounced negative TC is used. Conversely, the second-order component of ($TC\left(R_1\right)$ can cause nonlinearity errors in the sensor's measurements at high and low temperatures. Therefore, a poly resistor with the smallest negative TC available in our technology was chosen. The I_{PTAT} is set at $5\mu A$ at room temperature, balancing power dissipation with the resistor size, which is dictated by the sheet

resistance.

Additionally, a key factor in lowering (I_{PTAT} is to prevent the self-heating effect of the resistor, which could otherwise introduce offset errors in the temperature readings.

The CCO circuit, a CMOS current-mode relaxation oscillator [351], uses a basic current-mode comparator (M21-M23) from [352] to create a clock signal by comparing capacitor voltages with the reference voltage ((V_{BGR})). With an adequate comparator gain, the frequency of the thermally-responsive oscillating signal can be approximated as:

$$f_{OSC} = \frac{1}{T_{OSC}} = \frac{I_{PTAT}}{2C_{1,2}V_{BGR}} \tag{3.11}$$

Because in the design, $C_1 = C_2$ and are charged with the same amount I_{PTAT} and compared to equal trigger voltage (V_{BGR}), the duty cycle of the output signal is almost 50%. The V_{BGR} circuit is not designed to have a minimum possible TC as in the prevalent case of BGR circuits. In this design, the TC of the V_{BGR} is tuned by adjusting the R_2/R_1 ratio during the simulation to compensate for the residual nonlinearity effect of both the TSC and CCO units. Because the TC of the MIM capacitor used in the design is very small and can be ignored, the output clock signal exhibits PTAT characteristics with linearity dominated by the linearity of the PTAT current source.

The clock signal can be generated with a single capacitor as in [352], which requires a full discharge before each charge cycle. This involves the addition of a delay circuit, possibly composed of inverters and capacitors, and a quick discharge switch to the ground. Although simple, the PVT sensitivity of the delay circuit can affect the frequency accuracy, a problem lessened by using larger capacitors at the expense of the design size. Alternatively, a basic current-starved oscillator can convert the PTAT current to frequency; however, it has voltage supply dependencies. The transistors (M28-M33) form the essential startup circuit for the BGR, injecting sinking and sourcing currents into the upper and lower mirrors of the BGR to ensure reliable startup under adverse PVT conditions. These dynamic startup currents diminish to zero following the successful activation of the BGR, thus not affecting the I_{PTAT} characteristics.

The novelty of this research lies in the application of the optimization algorithm to the NIS, which replicates the DUT adjustment methods and enables filter tuning without

halting its operation. In the regression model's (RM) training phase, as illustrated in Figure 3.25, both the sensors and the filter undergo identical operating and PVT conditions and are linked to the same settings. The tuning patterns coarsely span the entire frequency range during this phase.

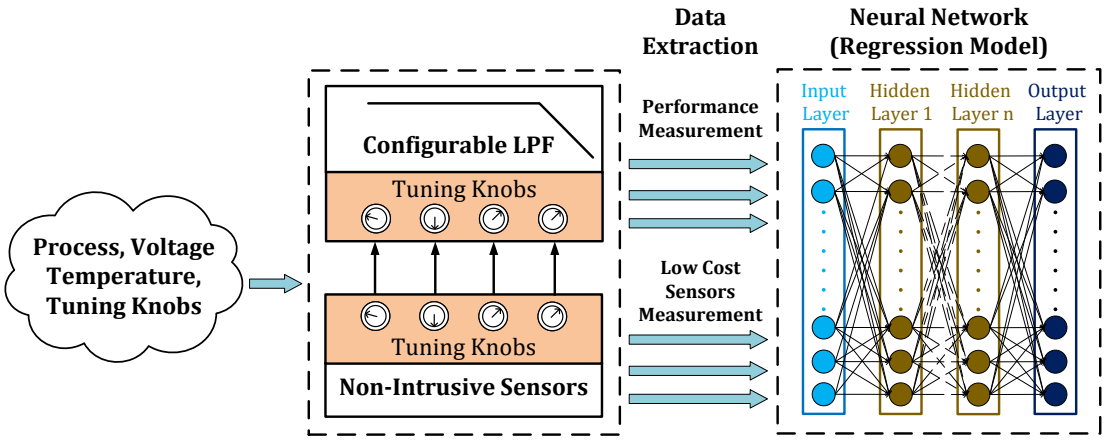

Figure 3.25: Filter and non-intrusive sensors in the training phase.

In this thesis, reconfigurability is implemented in the NIS for the first time, with the entire optimization process conducted using the NIS tuning knobs (TK), instead of the filter TK, as depicted in Figure 3.26. After optimization, the TK values are transferred to the main DUT. A Random Forest Regressor (RFR) is employed to establish a precise regression model linking the NS outputs, TK, and DUT performance. The RFR facilitates an indirect estimation of the DUT performance using cost-effective measurements of the quasi-digital output frequency of the NIS. The workflow of the proposed method is shown in Figure 3.27.

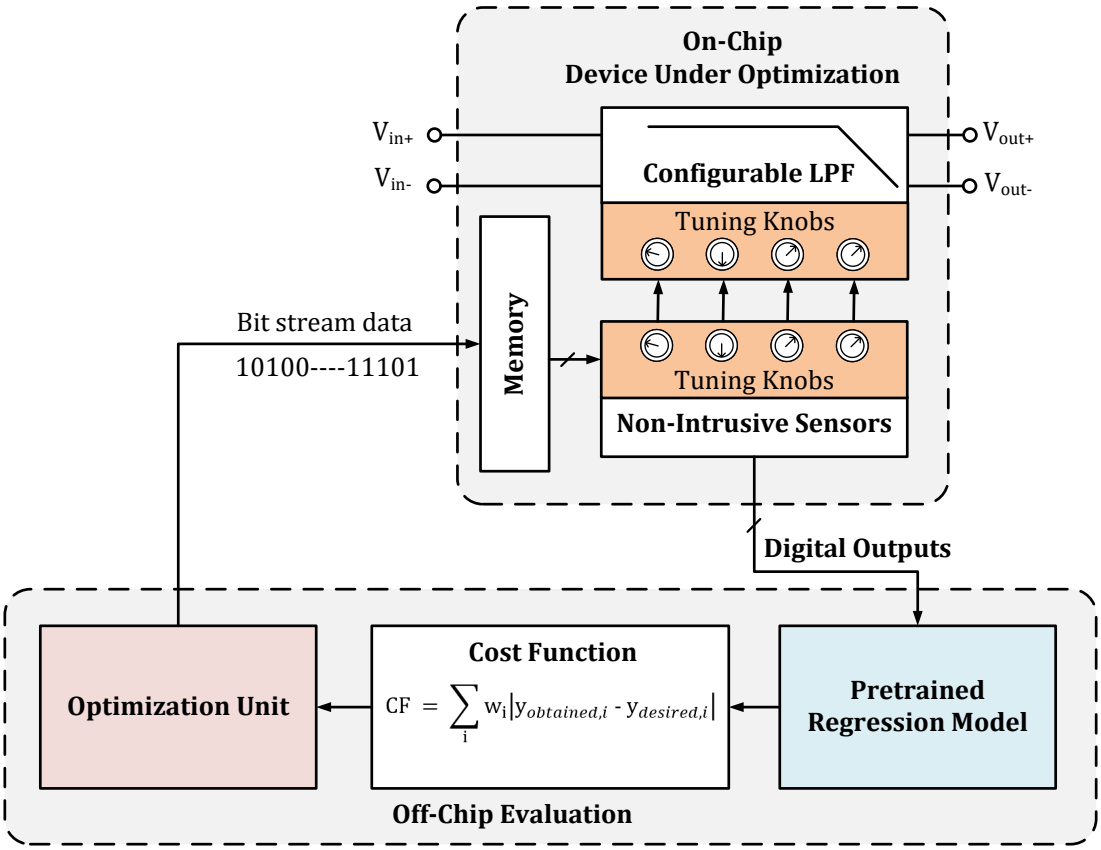

Figure 3.26: The block diagram of the proposed filter tuning approach using IM and reconfigurable NIS.

For filter tuning optimization with a neural network, the process begins by shortlisting the optimal TK values for training from the optimization space, thereby reducing the dataset size and evaluation time. The NIS outputs and the DUT performance are then simulated under similar PVT conditions. 80% of this data set is randomly chosen for RFR training, and the remaining 20% is used for performance evaluation. During testing, a particle swarm optimizer (PSO) determines the TK values of the NIS. The NIS output and current TK values are fed into the pre-trained RFR to indirectly estimate the DUT performance. The PSO uses the RFR's response to adjust the TK values for subsequent iterations.

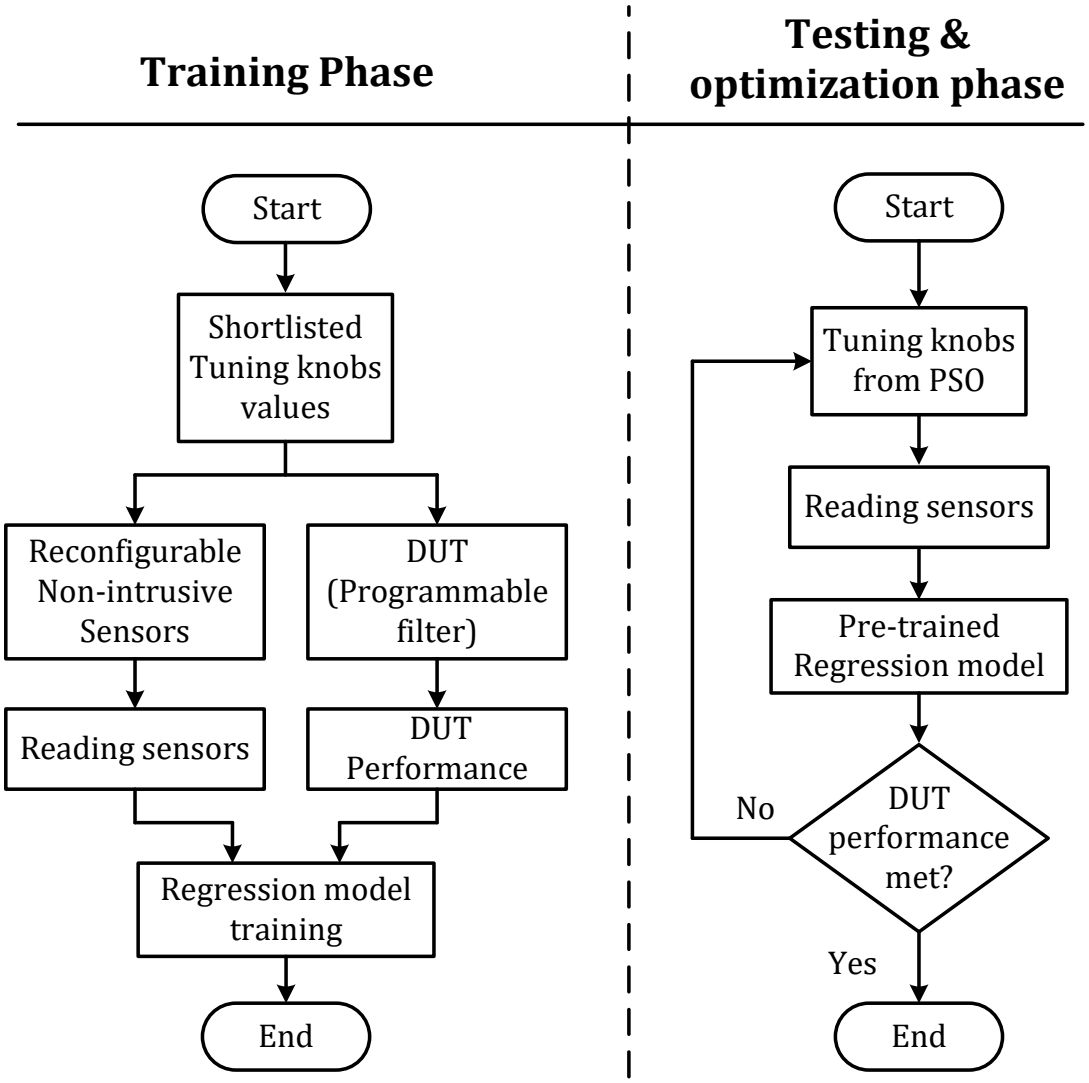

Figure 3.27: Flow chart of the proposed IMs approach with reconfigurable NIS.

Figure 3.28 graphically represents the performance of the RFR post-layout simulation. Using 1000 estimators and the mean squared error criterion, the RFR achieved an Adjusted R Squared (ARS) value of 90.13%. This experiment was conducted using 10 particles over 100 iterations.

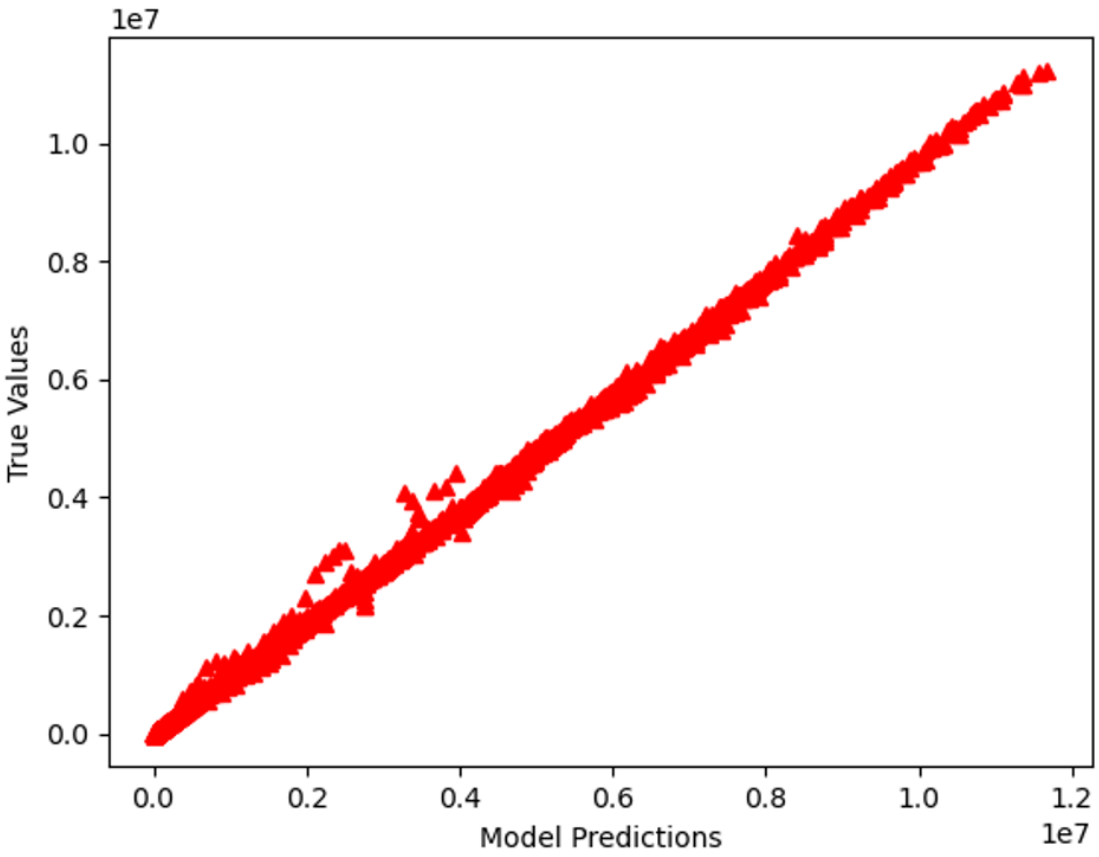

Figure 3.28: Scatter plot of the predicted and true values of the tuned filter.

3.3 Chip Implementation

The CFIA and tunable filter have been integrated into a single prototyping chip, in addition to the circuit design of another Ph.D. candidate at the institute for his doctoral research [353]. Figure A.1 demonstrates the block-level components of the chip. In this figure, the section pertinent to our research is highlighted in the amplitude domain, reflecting the intrinsic characteristics of our circuit concept. Two distinct CFIA modules are developed. Each module is equipped with its shadow register and PMM. The shift register comprises a $D_{outDebug}$ output for debugging purposes that meets DFT requirements. The first CFIA module operates without an offset voltage correction mechanism. Instead, the offset transconductance stage is manually adjusted via an external DC source. On the other hand, the second CFIA module integrates a digital offset auto-zeroing scheme.

After the CFIA stage, a tunable filter is integrated into the chip design to optimize the chip architecture and reduce the number of I/O pins. The CFIA registers memory has

been set up to transfer data internally to the register memory of the filter. Furthermore, non-invasive sensors, including temperature sensor, were deliberately incorporated next to the filter circuit.

The circuits are designed using Cadence design tools and XFAB's 0.35 μm CMOS NWELL technology, and supported by the Europractice program. The chip covers a total area of 10.89mm^2 and includes 100 input/output pads consisting of 62,921 transistors, as depicted in Figure 3.29. Figure A.2 shows the chip bonding to CPGA100 package type.

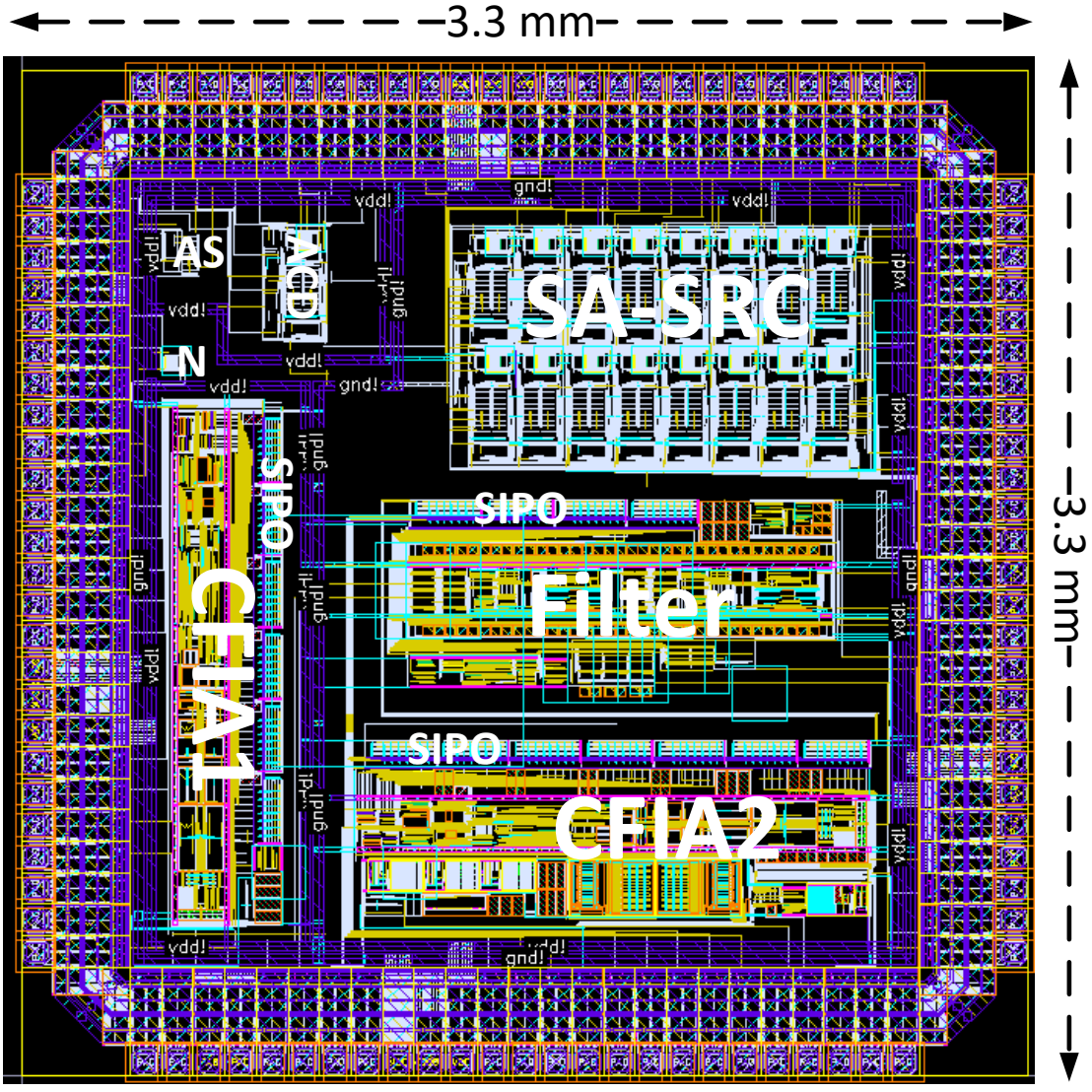

Figure 3.29: The physical implementation of the prototyping chip.

In comparison, the previous USIX 1.0 and USIX 2.0 versions from our institute occupied areas of 11.59 mm^2 and 18 mm^2 respectively. These chips offered a comprehensive solution for interfacing with sensors and for handling various mixed-signal cells in the

readout circuit pathway. However, the current project focus on the key cells of the AFEX within an economically viable prototyping chip.

The chip is constructed using four metal layers. The first three layers, up to metal3, are dedicated to laying out and routing cells in the lower design hierarchy. In contrast, a thicker metal4 layer is utilized for routing the power rings in the top-level hierarchy, chosen for its capacity to handle higher current density. To mitigate local IR drops on the supply rails and to not surpass the driving capability of a single power pad, 11 pads are allocated specifically for powering the chip. The remaining pads include 61 digital I/O pads and 28 analog pads. The driving capability of the digital pads is carefully chosen to align with the speed of the designed circuits. If not properly matched, an excessive driving margin could lead to unnecessary additional dynamic requirements for the power metal width.

Substrate contacts are liberally placed among the cells to maintain a consistent bulk potential across the chip surface, which is crucial for preventing latch-up issues and the formation of forward diodes. Furthermore, decoupling capacitors are distributed between the supply rails to support the internal stability of the V_{DD} during dynamic operation.

Because the analog cells are deactivated (powered down) during digital activities, including memory data writing or PMM or NIS reading, it is possible to merge the analog ground with the digital ground and save more physical area. The pad frame is designed to house the chip using CPGA100 package.

Prior to the fabrication, a sign-off simulation is performed by simulating the basic functionality of both the CFIA and the LPF at the chip level under nominal conditions. This includes post-layout parasitic extraction to confirm the true connectivity and assess the impact of the pads on design performance.

Initially, the shadow register is evaluated, as illustrated in Figure 3.30. The CFIA and filter cells are then assessed using a configuration pattern derived from block-level extrinsic optimization. Figure 3.31 demonstrates the transient testing of the CFIA cell with a sinusoidal input signal, where the gain is dynamically varied from 1 to 2. Following the CFIA approach, the filter circuit is tested using two distinct configuration patterns. These tests, which are designed to alter the cutoff frequency, are shown in Figure 3.32. Given that the simulation has confirmed the basic functionality and top-level integrity of the chip, the process advances to the fabrication stage. A comprehensive intrinsic

evaluation of the chip is presented in the subsequent chapter.

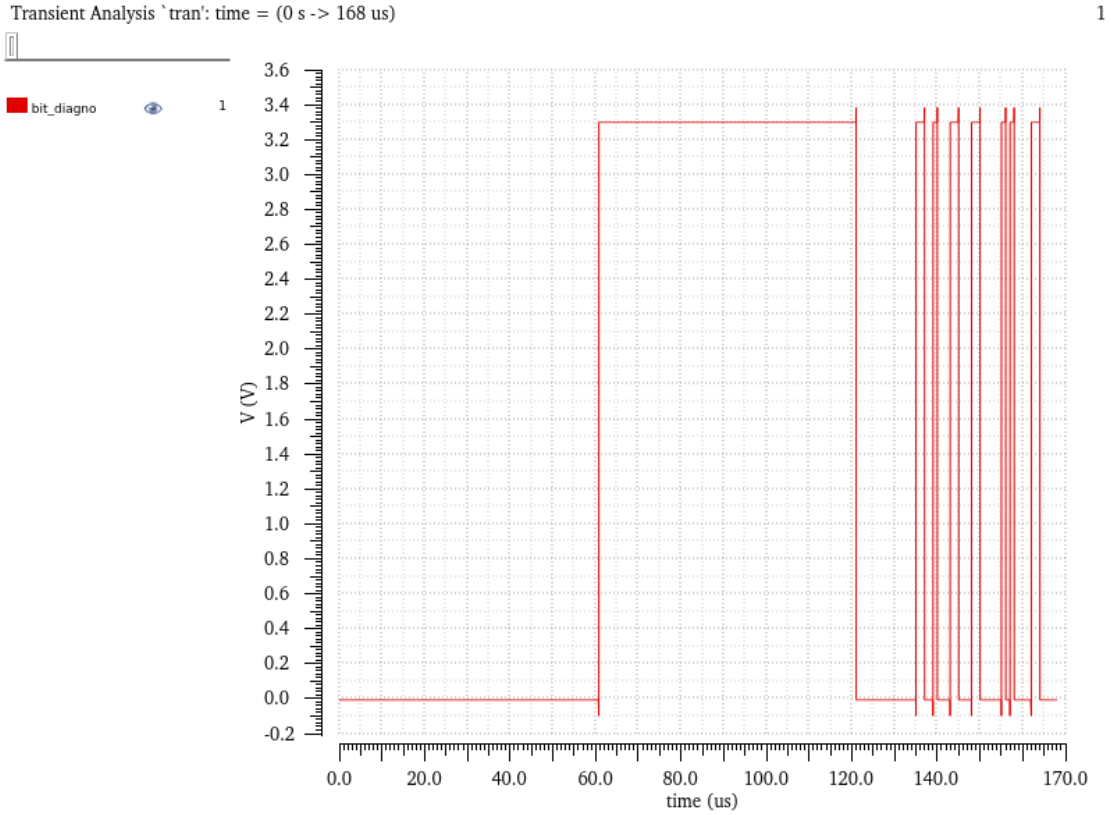

Figure 3.30: Post-layout simulation result at the chip level for the shadow register debugging output bit.

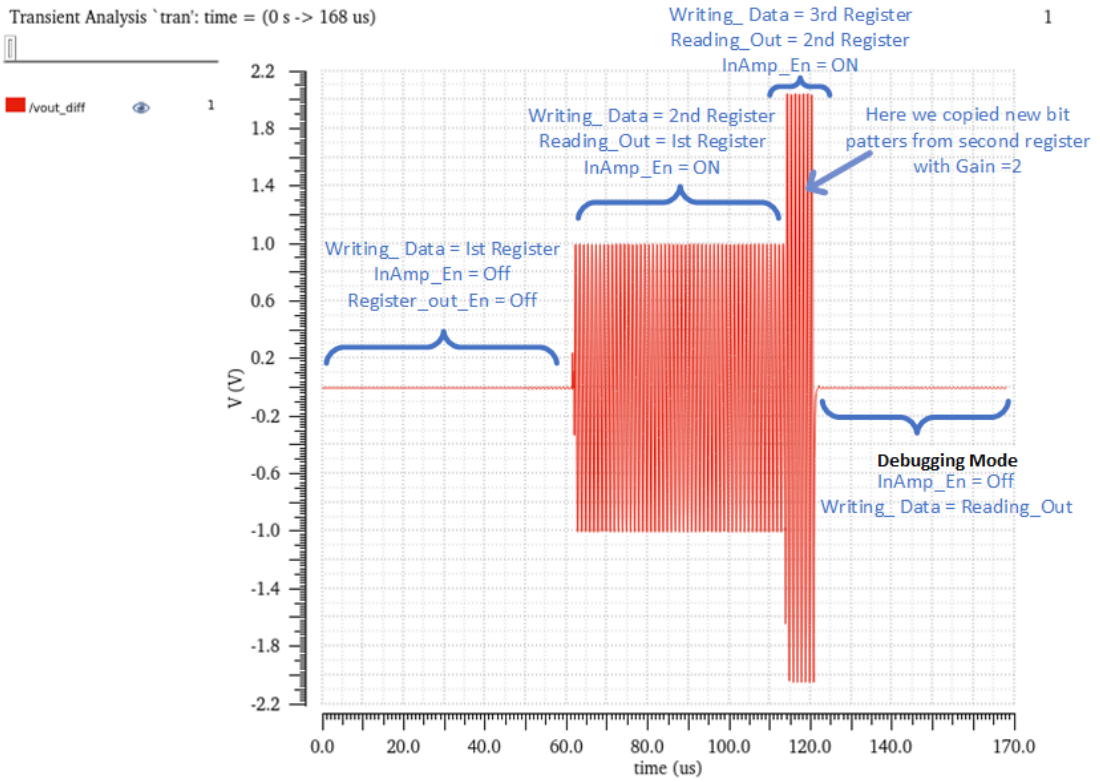

Figure 3.31: Post-layout simulation results at the chip level for the CFIA with different gains using configuration patterns obtained from the optimization process.

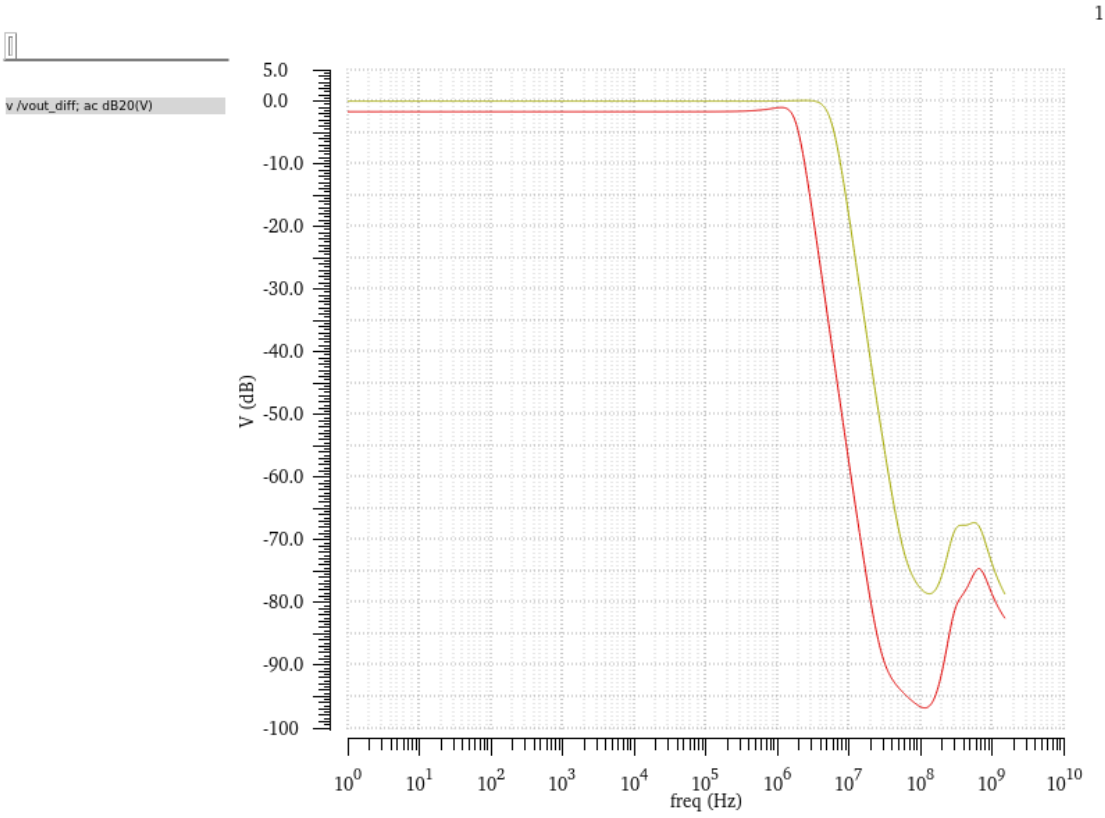

Figure 3.32: Post-layout simulation results at the chip level for the LPF with two different configurations.

Chapter 4

Experimental Setup and Chip Results

This chapter outlines practical chip testing [354], and details the actual measurement outcomes achieved through laboratory measurements using the proposed methodologies, following the chip fabrication and packaging through the EUROPRACTICE program. The chip micrograph is displayed in Figure 4.1a, and Figure 4.1b illustrates the chip layout.

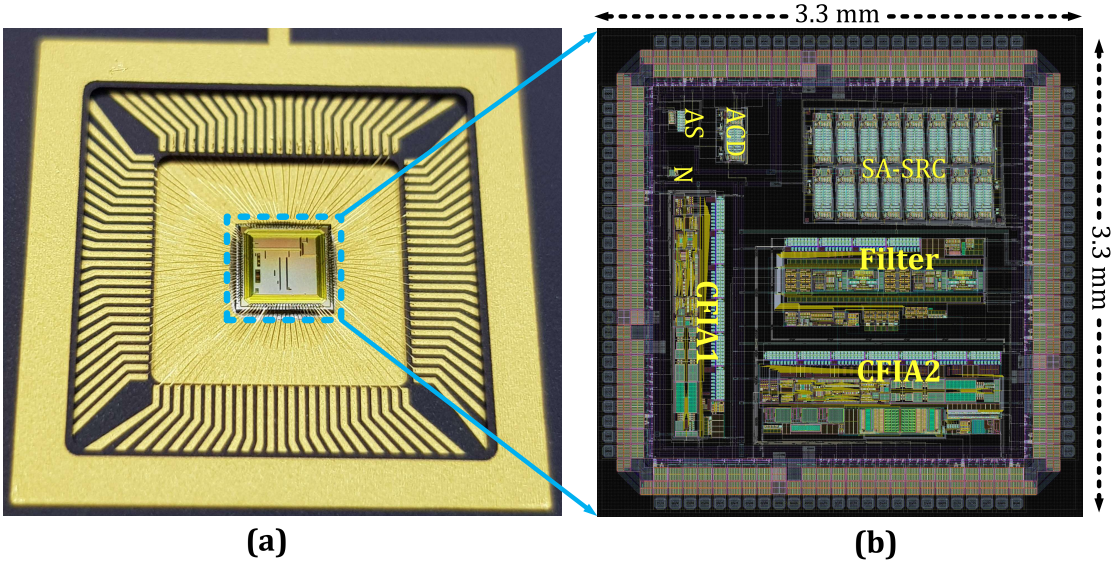

Figure 4.1: MPC USIX chip: (a) Chip layout with the pad frame, and (b) micrograph showing the bonding wires and sealing ring.

The die is coated with a passivation layer for surface protection, which obscures the layout details. It is incorporated in a CPGA 100 package and is a multi-project chip

(MPC) consisting of amplitude and spike-domain analog front-end circuits with self-X properties (AFEX). These MPC cells form the basis of an advanced universal sensor interface with self-X attributes, termed as the USIX chip. However, this thesis focuses exclusively on the amplitude-domain part of the chip. The chapter is structured into two primary sections: the first discusses the in-amp's practical testing, and the second examines the filter test.

4.1 Instrumentation Amplifier Testing

4.1.1 Intrinsic Implementation and Architecture of the Self-X System

Figure 4.2 presents the block diagram of the proposed intrinsic implementation, depicting the internal setup for on-site optimization of the CFIA through the indirect measurement approach. This experiment utilizes two Red Pitaya boards. The first (FPGA board 1) handles the data collection, THD analysis via FFT, and data transmission to the server. The second (FPGA board 2) manages the ERPSO execution, serially transfers configuration patterns to the CFIA, and computes the signal frequency for the power-monitoring module.

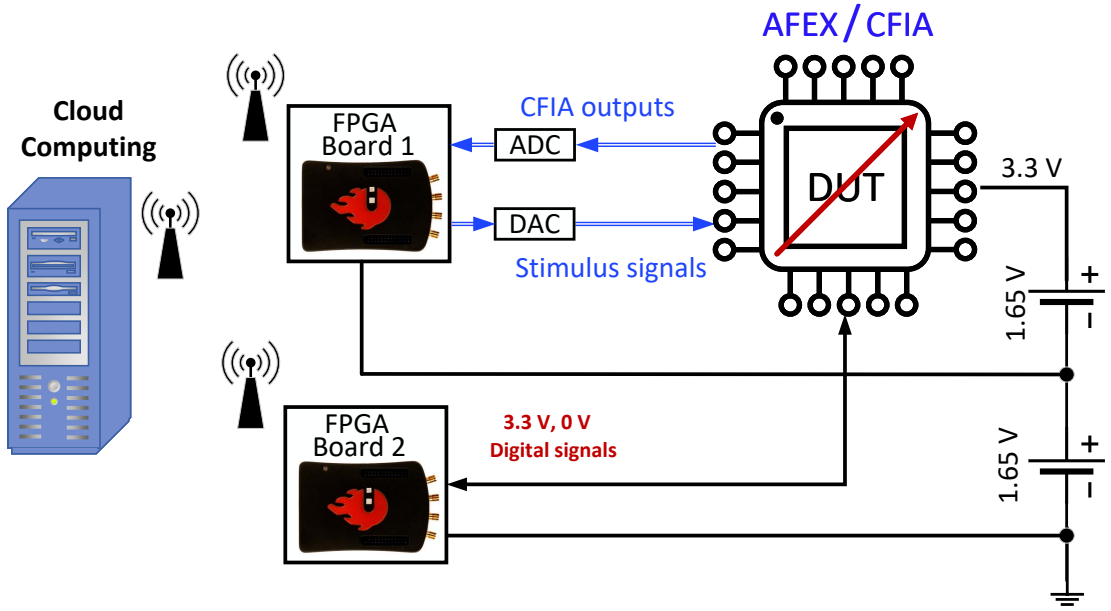

Figure 4.2: Block diagram of the proposed in-field optimization of the reconfigurable CFIA circuit.

The analog outputs of the Red Pitaya board, being grounded at 0 V, necessitate a DC level shift of 1.65 V for FPGA board 1 to align with the CFIA's dynamic input

range in single supply mode at 3.3 V. Alternatively, to synchronize the dynamic ranges of the FPGA board and CFIA chip, options include a transformer balun, such as Coilcraft's PWB2010, or an active DC level shifter using broad-bandwidth fully-differential amplifier circuits, such as Texas Instruments' LMH6553 or Analog Devices' LTC6363. Nonetheless, opting for a transformer confines the experiment to higher frequencies, and the latter solution is discarded to avoid the uncertainties introduced by additional analog components in the prototype demonstration chain

Figures 4.3 and 4.4 illustrate the comprehensive implementation of the self-X design in the CFIA circuit on Red Pitaya boards 1 and 2, respectively. The creation of essential binary files for these boards, which are necessary for the development of this architecture, is performed using the Vivado design suite from Xilinx. The RF DACs integrated into the Red Pitaya boards are used to produce fully-differential stimulus signals for evaluating the CFIA circuit. In parallel, the RF ADCs capture the output response of the CFIA circuit. Both the ADC and the DAC boast a 14-bit resolution. The ERPSO process is conducted on Red Pitaya board 2, whereas Red Pitaya board 1 is designated for THD measurement execution.

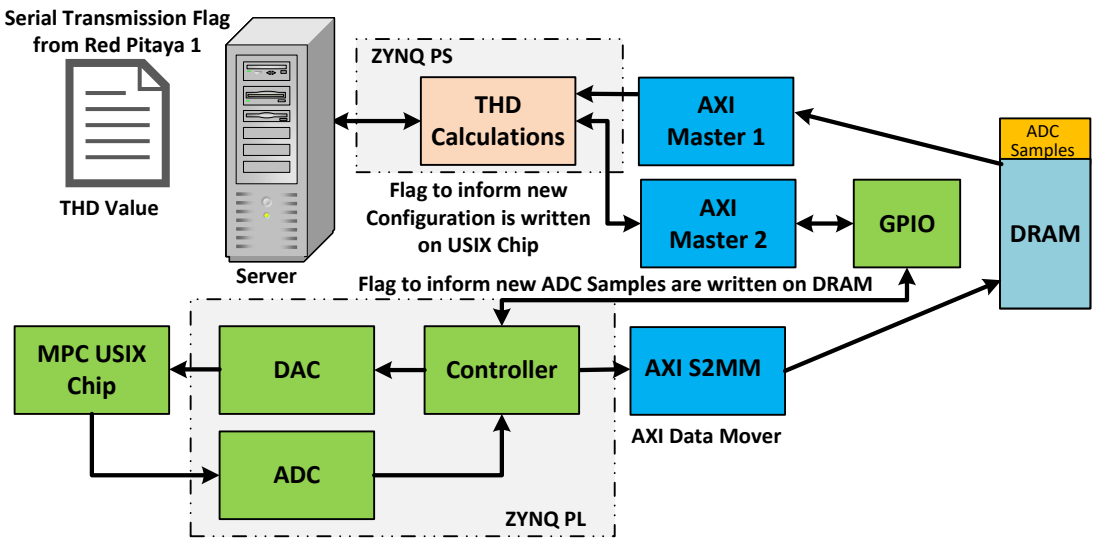

Figure 4.3: Detailed implementation of the self-X architecture for the Red Pitaya board 1.

4.1.2 Workflow of the Optimization Process

Figure 4.5 displays the optimization process, mirroring the performance optimization framework of Synopsys [221]. This process involves two Red Pitaya boards, each equipped

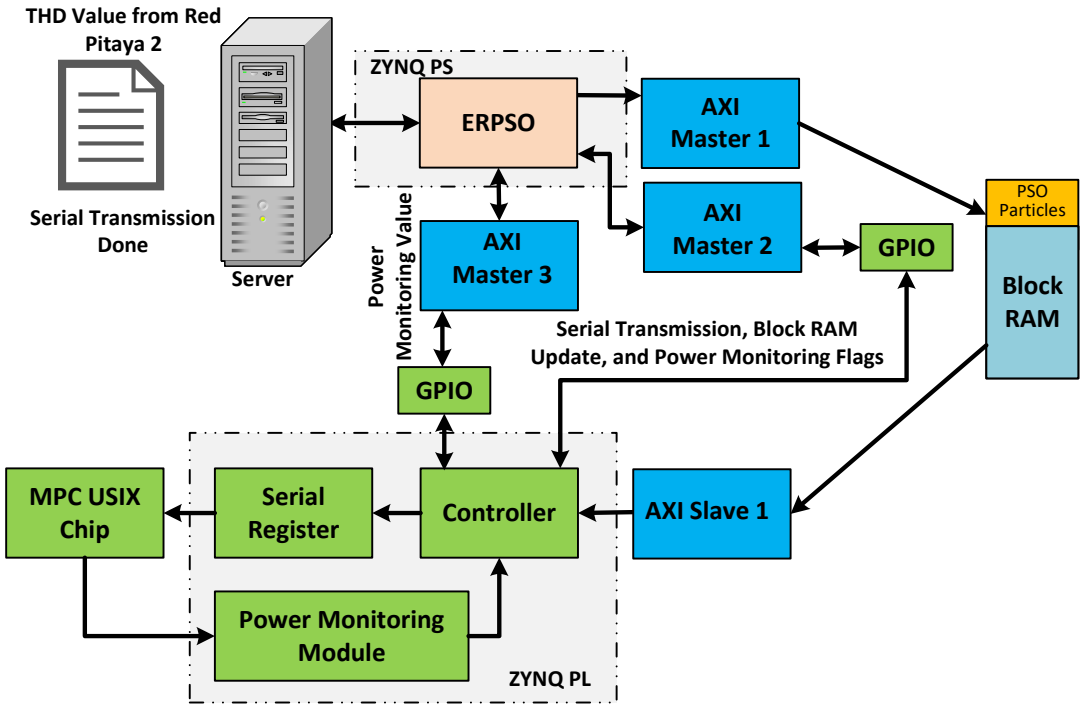

Figure 4.4: Detailed implementation of the self-X architecture for the Red Pitaya board 2.

with their respective ADCs/DACs to form the assessment unit. The objective is to determine the optimal THD value while minimizing power usage, using a hierarchical multi-objective optimization strategy. The reconfigurable components within the CFIA circuit act as tuning knobs. The optimization algorithm reconfigures the system, which inputs the configuration pattern into the CFIA. Subsequently, the output response of the CFIA is recorded. This cycle continues until a predefined termination criterion is satisfied. Finally, the optimization outcomes are compiled and presented at the end of the optimization process.

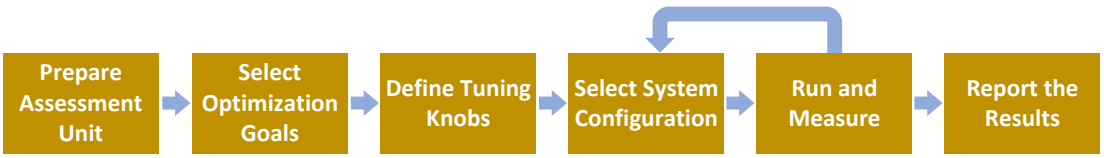

Figure 4.5: Performance optimization workflow of smart sensory electronics.

The optimization procedure is initiated with the serial transmission of ERPSO particle values to the CFIA shadow register through Red Pitaya board 2. During this data entry phase, the CFIA is temporarily powered off to prevent unpredictable transitional states. Once the data input is complete, the CFIA is reactivated. Subsequently, Red

Pitaya board 1 receives a notification through the server to commence THD calculations for the respective ERPSO particle solution.

In the THD calculation phase, Red Pitaya board 1 applies a fully-differential sinusoidal stimulus to the CFIA input and captures its output using the onboard RF DAC and ADC, respectively. The acquired data samples are then stored in the shared dynamic random-access memory (DRAM) of the Red Pitaya board through an advanced extensible interface (AXI) stream to memory-mapped IP. Once the data acquisition is complete, the controller module signals an acknowledgement flag, informing the Red Pitaya board's processing subsystems (PS) about the completion. The THD is then calculated using these samples on the PS side of Red Pitaya board 1. This THD value is relayed to Red Pitaya board 2 via the server for integration into the ERPSO algorithm. Subsequently, the ERPSO triggers the power-monitoring module to indirectly gauge the DC power consumption of the current solution by measuring the output frequency from the power-monitoring circuit of the CFIA.

It is important to note that during THD analysis, power monitoring is disabled to prevent transient pulse-switching disturbances from affecting the analog outputs. This optimization cycle repeats until reaching the maximum iteration count. Figure 4.6 depicts the experimental laboratory setup for this methodology. The four-layer PCB prototype board was designed using Eagle Autodesk software, incorporating separate power and ground layers with decoupling capacitors near the power pins of the chip to enhance the noise performance.

4.1.3 Measurement Results

4.1.3.1 Shadow Register Verification

The initial step in the verification involves loading the CFIA circuit with a default configuration pattern acquired from the post-layout extrinsic assessment. This configuration is serially sent from the Red Pitaya to the CFIA's shadow register, with a data rate of 1 Kb/s, using a method akin to serial peripheral interface (SPI) protocol mode 0. In this setup, the Red Pitaya and the chip operate as master and slave, respectively. When idle, the clock polarity remains logically low. The shadow register captures the data on the rising edge of the clock and changes the data on the falling edge. Control over the shadow register's read-write operations is governed by using four bits: two for writing

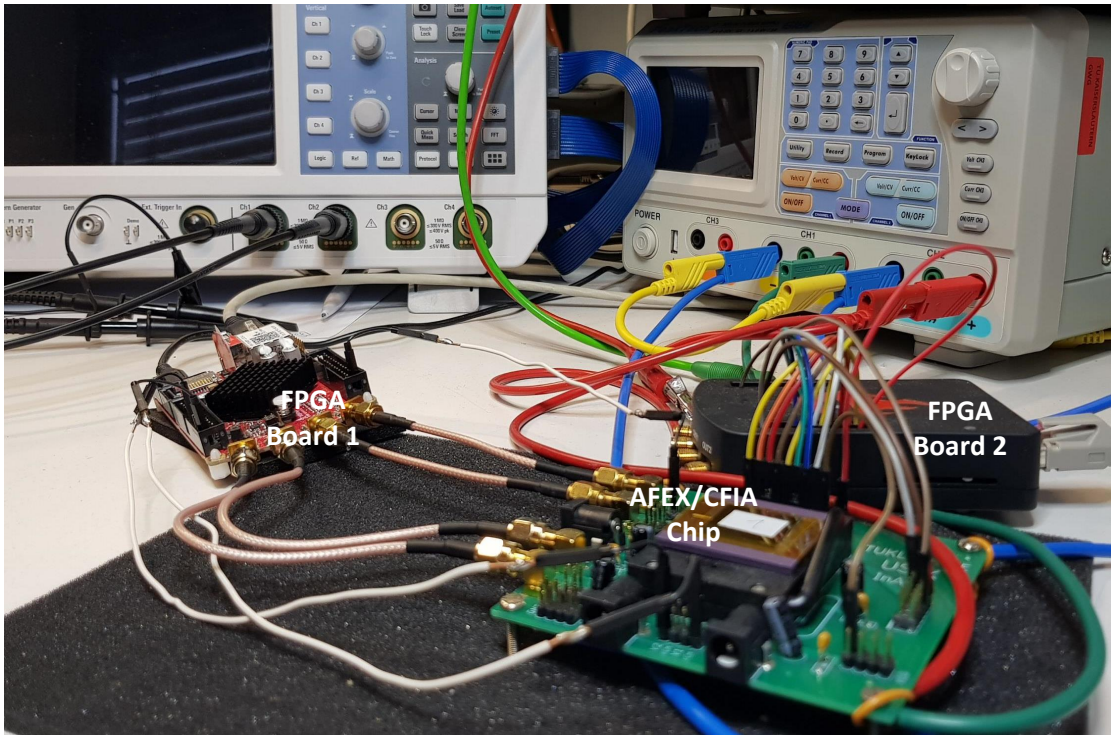

Figure 4.6: Lab setup for the evaluation of the proposed methodology.

and two for reading as explained in Chapter 3. The register's most significant bit (MSB) is linked to the (Dout_Debug) pin, facilitating the debugging of the register's serial data.

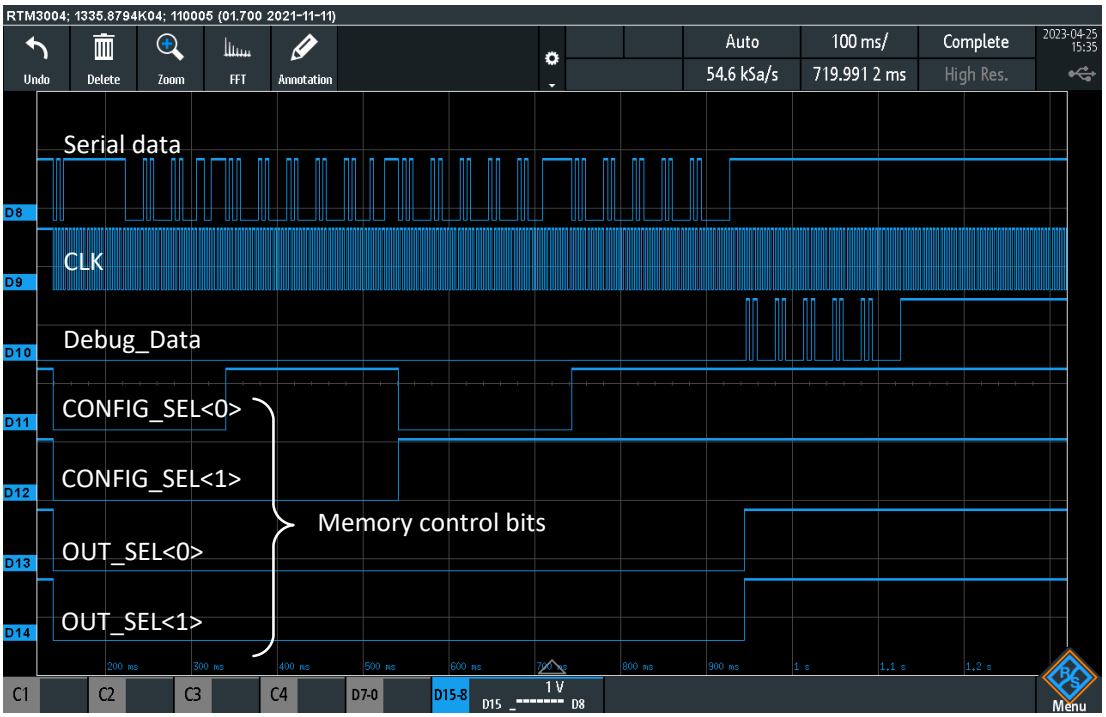

Figure 4.7: Verification of the shadow register function using the debugging pin.

4.1.3.2 CFIA Testing Using the Default Configuration

Although the circuit performed successfully in simulations with the RC extraction netlist and passed the PVT checks using Monte Carlo (MC) and worst-case (WC) simulations across a broad industrial temperature range (from −40 °C to 85 °C), including ±10% supply voltage variation, real-world measurements indicated instability. This instability could result from changes in the device characteristics caused by the fabrication and packaging processes, despite accounting for a 6 sigma process variation in the simulations.

Figure 4.8 presents the MC post-layout simulation assessing the CFIA's phase margin (PM) as a measure of the unity-gain closed-loop stability in its default setting. The evaluation used 500 samples with a Gaussian distribution to mimic the actual process profile, incorporating both the process and mismatch variations in the complete CFIA circuit. As shown, the CFIA maintained reliable PM at extreme corners, ensuring a 100% yield for a PM target of over 45°. During these tests, each differential output pair was connected to a 15 pF capacitive load and a 10 kΩ resistive load. Notably, the default configuration utilizes only the two least significant bits of the adjustable compensation capacitor and minimizes the power consumption in the output stage, leaving room for further PM improvement if needed, although simulations suggest that it is unnecessary.

Figure 4.9 displays the observed practical output behavior when both inputs are connected to a DC common-mode voltage (VCM) of 1.65 V. The input capacitance of Rohde & Schwarz's mixed-signal storage oscilloscope (MSO) is 14 pF in the X10 channels with 10 MΩ impedance, aligned with the load capacity of the designed CFIA.

Regardless of the unwanted oscillation, the output signals are informative, indicating that a symmetrically balanced layout results in uniform and in-phase outputs, leading to a high common-to-differential-mode rejection ratio. Consequently, the differential output signal (Vout_diff) exhibited a lower oscillation amplitude. The capability of the fully differential circuits to cancel out common-mode signal noise is a significant advantage. Nonetheless, oscillations at the output suggest that the CFIA struggled to track the input signal linearly.

Figure 4.10 displays this nonlinearity by comparing the CFIA's output DC characteristics, as the inputs linearly swept from 0 to 3.3 V with unity gain configuration and 33 mV steps, against post-layout simulation results.

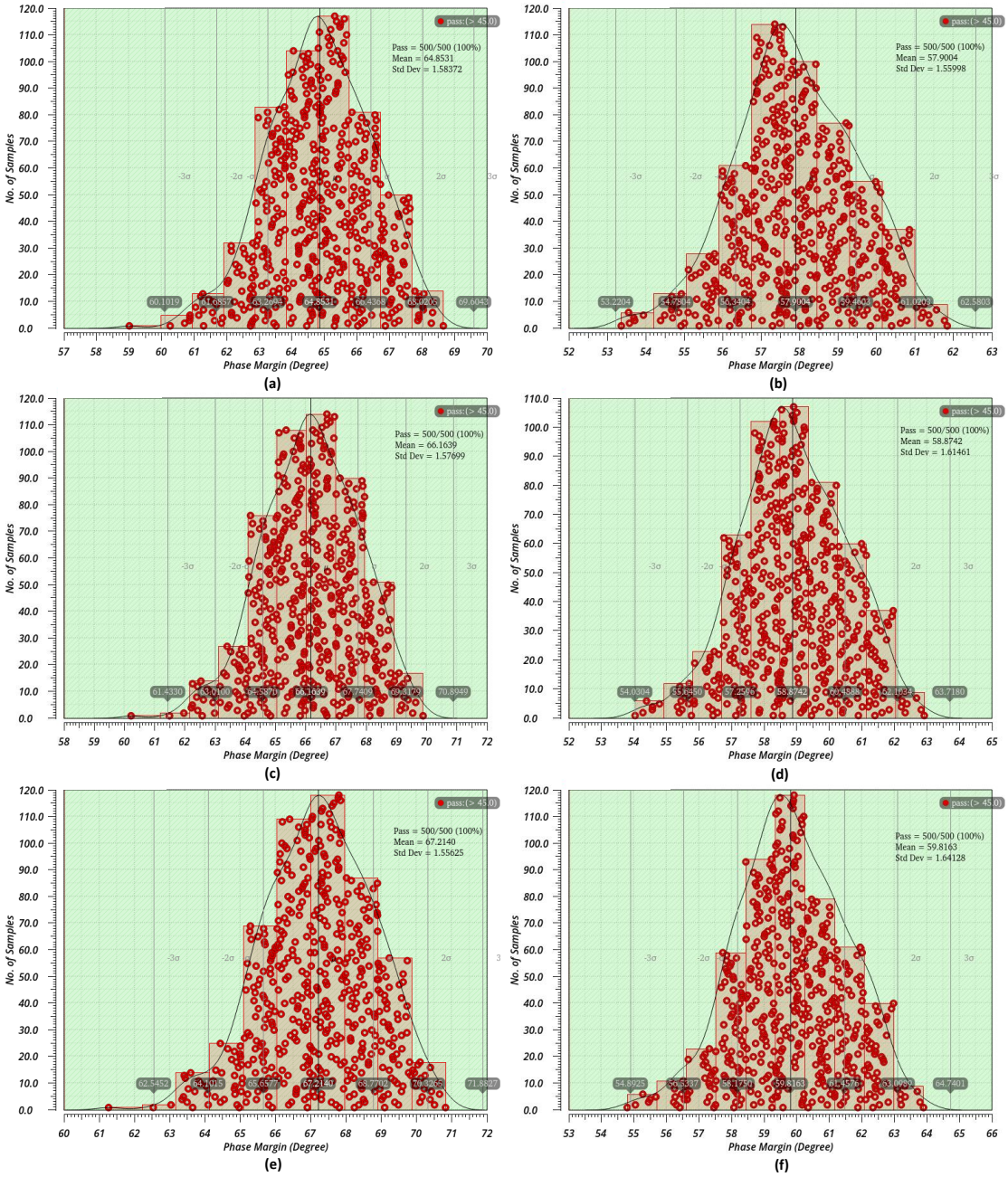

Figure 4.8: MC simulations on the post-layout CFIA netlist with RC extraction type using 500 samples per corner: (**a**) $V_{DD} = 3.0\ V$ *and* $T = -40$ °C; (**b**) $V_{DD} = 3.0\ V$ *and* $T = -85$ °C; (**c**) $V_{DD} = 3.3\ V$ *and* $T = -40$ °C; (**d**) $V_{DD} = 3.3\ V$ *and* $T = 85$ °C; (**e**) $V_{DD} = 3.6\ V$ *and* $T = -40$ °C; (**f**) $V_{DD} = 3.6\ V$ *and* $T = 85$ °C.

Figure 4.11 shows the transient response of the output to a 1 Vp-p, 1 MHz fully differential sinusoidal input, underscoring the time domain distortion. Moreover, Figure 4.12 illustrates the differential output in the frequency domain, captured via the FFT analysis. This output distortion leads to harmonic disruption in the frequency spectrum of the signal, thereby linking the nonlinearity of the CFIA to the measured THD value. A THD value of -30 dB in this context signals significant nonlinearity.

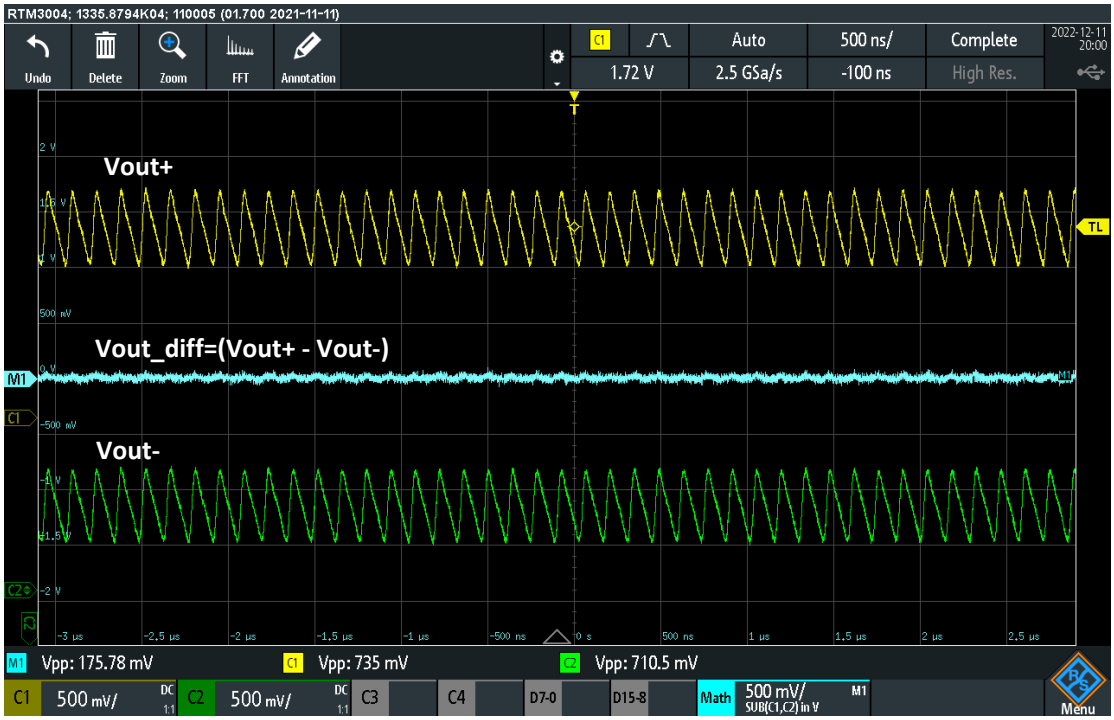

Figure 4.9: Unstable condition of the CFIA under default pattern configuration.

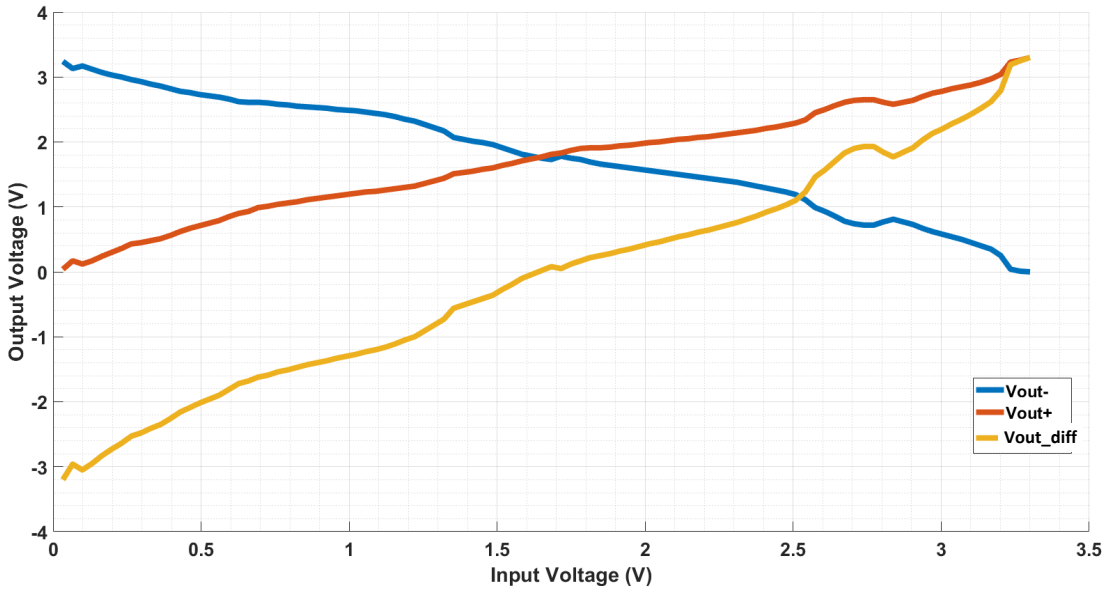

Figure 4.10: Output DC characteristics of the unstable CFIA under unity gain configuration compared to the post-layout simulation.

The aforementioned experiment is first carried out on 15 chips, handpicked from a lot of 32 chips numbered in sequence. For this test, chips numbered 1 and 3 to 16 were examined, all exhibiting comparable traits, likely due to their shared wafer origin in manufacturing. This suggests that, if the circuit is designed with fixed-size components, the entire batch may be discarded. This scenario highlights the importance

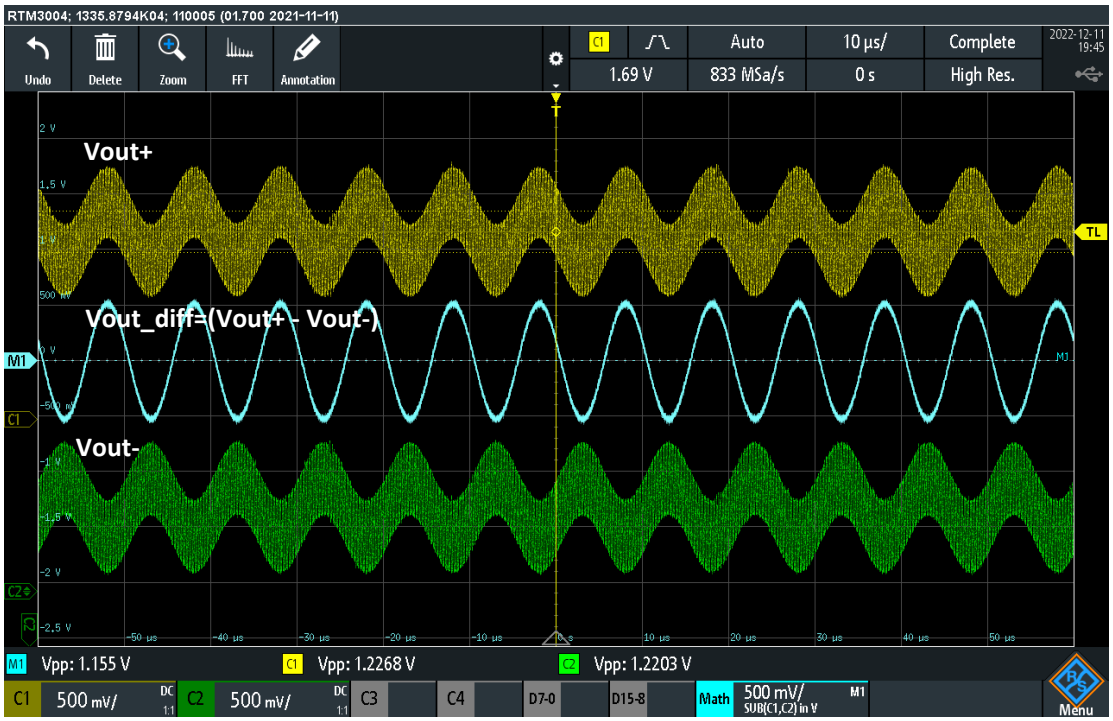

Figure 4.11: The transient response of the output to the fully differential sinusoidal input signal under unstable conditions.

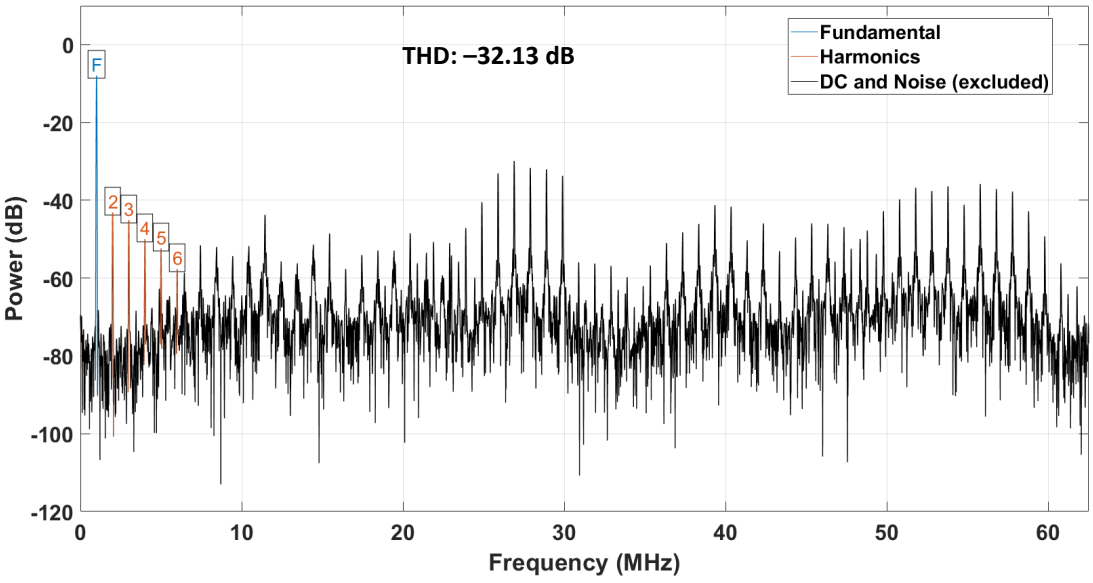

Figure 4.12: FFT output of the CFIA under unstable condition.

of configurable circuits with self-X capabilities in resolving such issues. As a result, in the next experimentation phase, the chip underwent in-field optimization using the ERPSO algorithm. This step aimes to identify the optimal configuration pattern for bringing the CFIA into its best operational zone

Before optimization, the power monitoring module (PMM) is tested by altering the

bias current of the CFIA via the current DAC, followed by tracking the output pulse frequency of the module. As explained in Chapter 3, the PMM circuit is a current-to-frequency converter that produces a quasi-digital signal with a 50% duty cycle, as depicted in Figure 4.13. The CFIA current is measured using the PeakTech 6181 power supply current meter, which has a 1 milliampere resolution. A frequency-to-digital converter (FTD) on the Red Pitaya was developed to interpret the PMM signal frequency and convert it into a decimal value, as shown in Table 4.1 using selected values. The FTD module starts counting up on the first rising edge of the PMM output signal and stops at the next rising edge to determine the corresponding frequency. Operating at 125 MHz, the FTD counter is aligned with the Red Pitaya system clock. Since the highest PMM frequency is under 10 MHz, the FTD resolution is sufficiently accurate for these measurements.

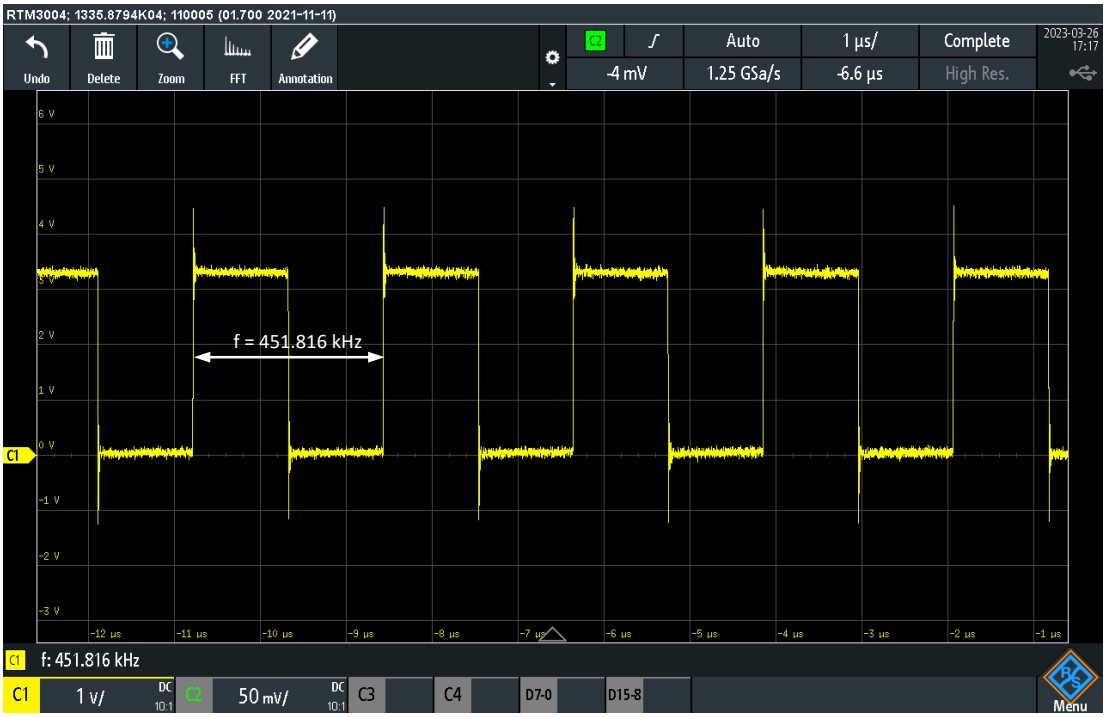

Figure 4.13: Output signal of the integrated power monitoring module.

Figure 4.14 illustrates that the power monitoring system demonstrates sufficient linearity, aiding the optimization algorithm by supplying essential CFIA power information. This assists in identifying and choosing the most effective solution within the explored scope. Notably, the linearity curve is affected by the resolution of the current measurement equipment.

Table 4.1: Recorded values of frequency-to-decimal conversion of the power monitoring module.

Config Nr.	Clock Frequency	Decimal Equivalent	CFIA Current
1	325 kHz	24,561	1 mA
2	520 kHz	15,372	2 mA
3	701 kHz	11,401	3 mA
4	875 kHz	9162	4 mA
5	1.05 MHz	7233	5 mA
6	1.21 MHz	6618	6 mA
7	1.42 MHz	5627	7 mA
8	1.57 MHz	4725	8 mA
9	1.71 MHz	4566	9 mA
10	1.82 MHz	4404	10 mA
11	4.45 MHz	1626	24 mA
12	4.53 MHz	1595	25 mA
13	4.86 MHz	1489	27 mA

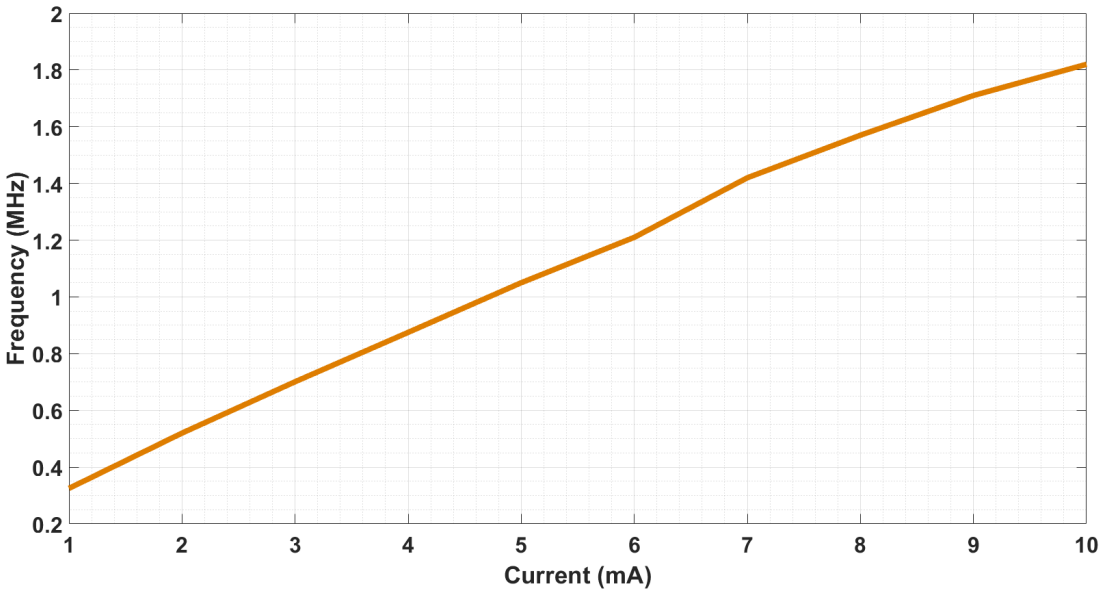

Figure 4.14: Linearity performance of the power-monitoring module showing the relationship between the PMM frequency and the CFIA current.

4.1.3.3 CFIA Performance Optimization Using the Proposed Methodology

A 1 Vp-p, 1 MHz fully differential sinusoidal stimulus is generated by Red Pitaya 1 using the Digital Signal Synthesizer (DSS) from the Xilinx Vivado IP blocks, serving as the test input for the optimization process. The output from the CFIA is captured by the Red Pitaya ADC at a 125 MHz sampling rate, aiding in THD analysis via FFT. The optimization algorithm utilized 15 particles and 200 iterations, adopting an agglomerative multi-objective optimization strategy with 80% emphasis on THD reduction and

20% on power monitoring. To ensure robustness against the events of lucky shots, the optimization is repeated across 10 distinct trials on the first chip (chip1). Detailed insights into the optimization algorithm are provided in [300, 314]. Figure 4.15 displays the average error-convergence trajectory of the optimization algorithm. To guarantee robust stability, the CFIA is set up in a unity-gain configuration.

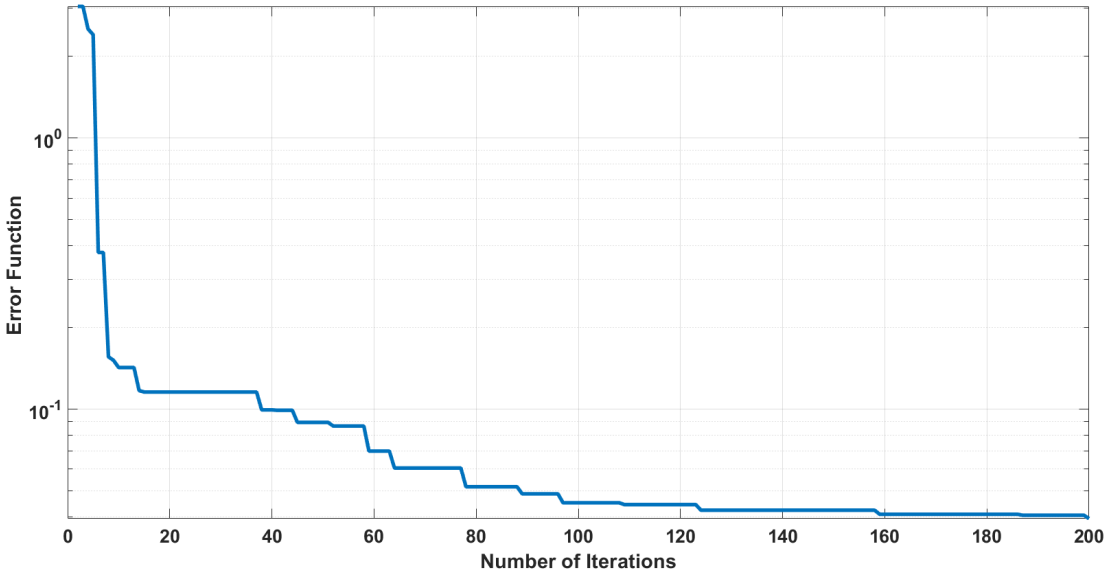

Figure 4.15: Mean values of the error-convergence curve of the CFIA optimization.

Figure 4.16 displays the frequency spectrum of the input test stimuli, while Figure 4.17 shows the FFT graph indicating the CFIA output frequency response for a solution found by the algorithm. Following the optimization, the average THD value achieved is -72 dB, with a power consumption of 55 mW. The findings indicate that the CFIA has been optimized to its maximum within the limits of the test signal used. Consequently, it is theorized that an enhancement in the THD value of the test stimuli would likely lead to a corresponding improvement the THD performance of the CFIA. This outcome can be expressed as follows: Figure 4.18 through an error bar graph for 10 separate runs. Simultaneously, Figure 4.18b illustrates the optimization results for a single iteration conducted on 15 different chips.

Figure 4.19 shows the sinusoidal output response, which clearly lacks oscillations. The slew rate, determined from the impulse response, is approximately ± 11 V/µs. In addition, a step response test is performed to confirm the stability. The outcomes, illustrated in Figure 4.20, reveal that the CFIA has a phase margin greater than 60°.

Figure 4.21 showcases the DC characteristics, highlighting the dynamic input range at

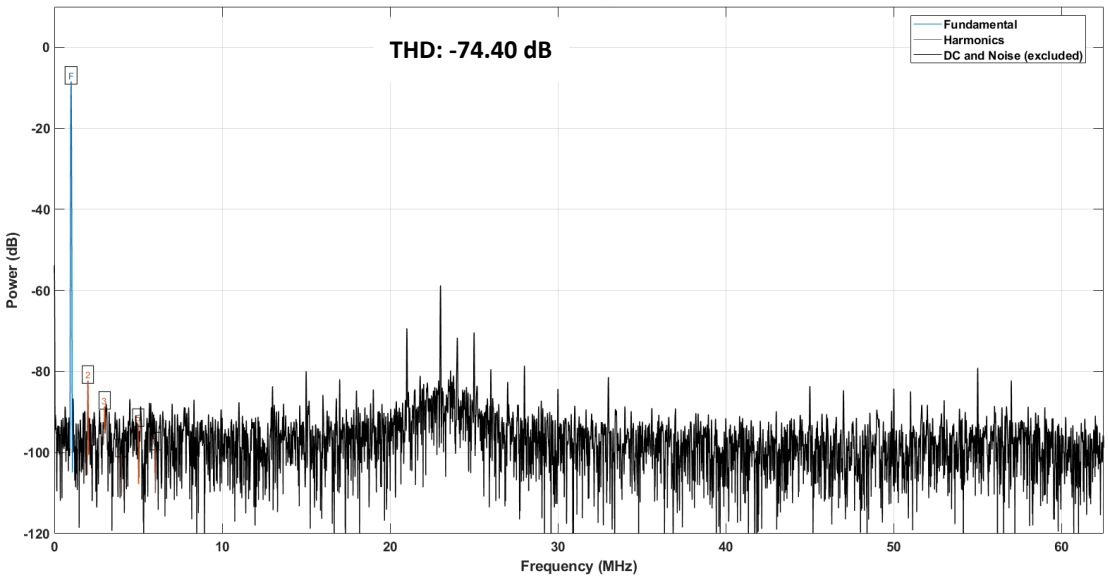

Figure 4.16: FFT output of the test stimuli used for optimizing the CFIA.

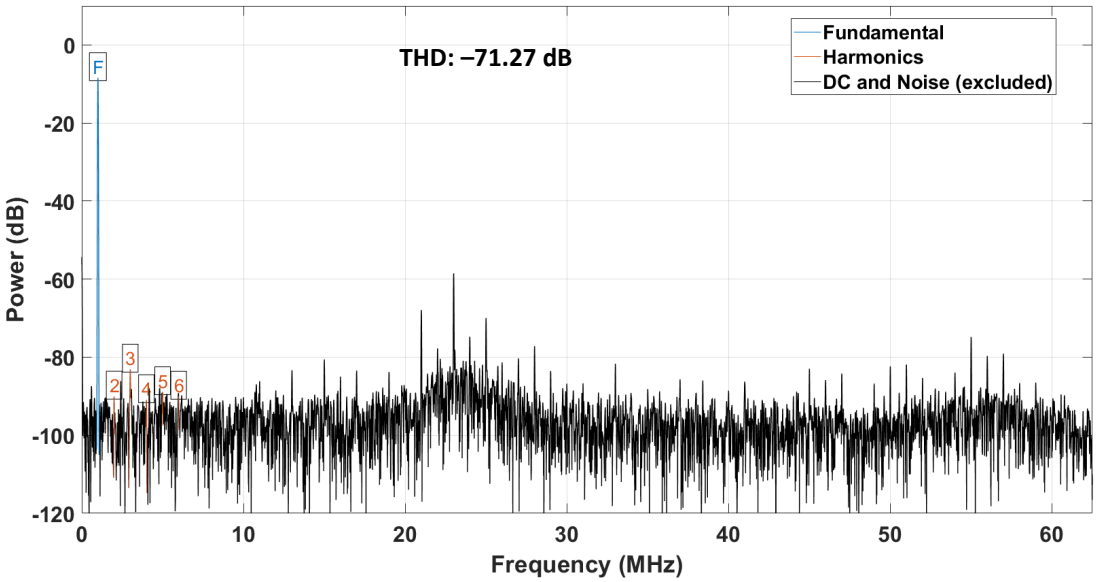

Figure 4.17: FFT output of the stable CFIA solution found using the optimization.

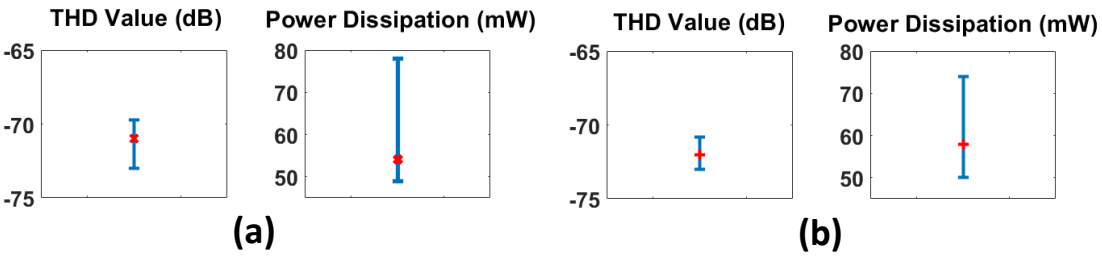

Figure 4.18: Box plots of the ERPSO algorithm: (a) over 10 independent runs on a single chip, and (b) a single run for 15 independent chips.

unity gain. This extensive differential range is particularly effective for interfacing high-output differential sensor signals, such as tunnel magneto-resistance (TMR). Different

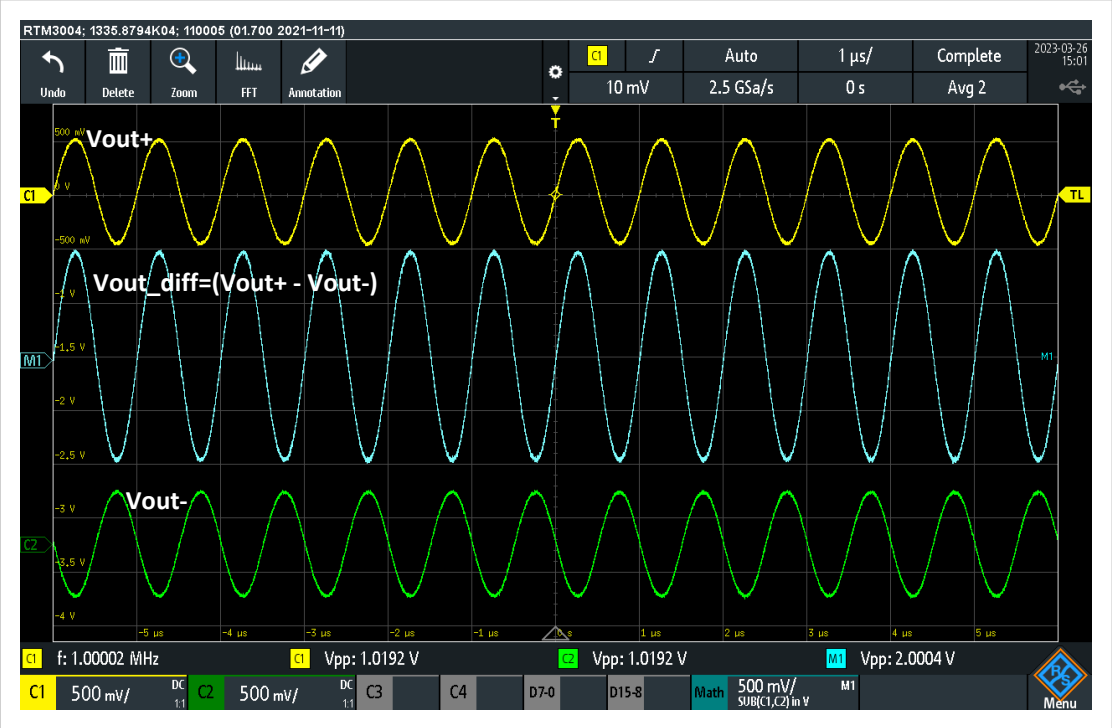

Figure 4.19: Large signal sinusoidal output response of the CFIA after the optimization.

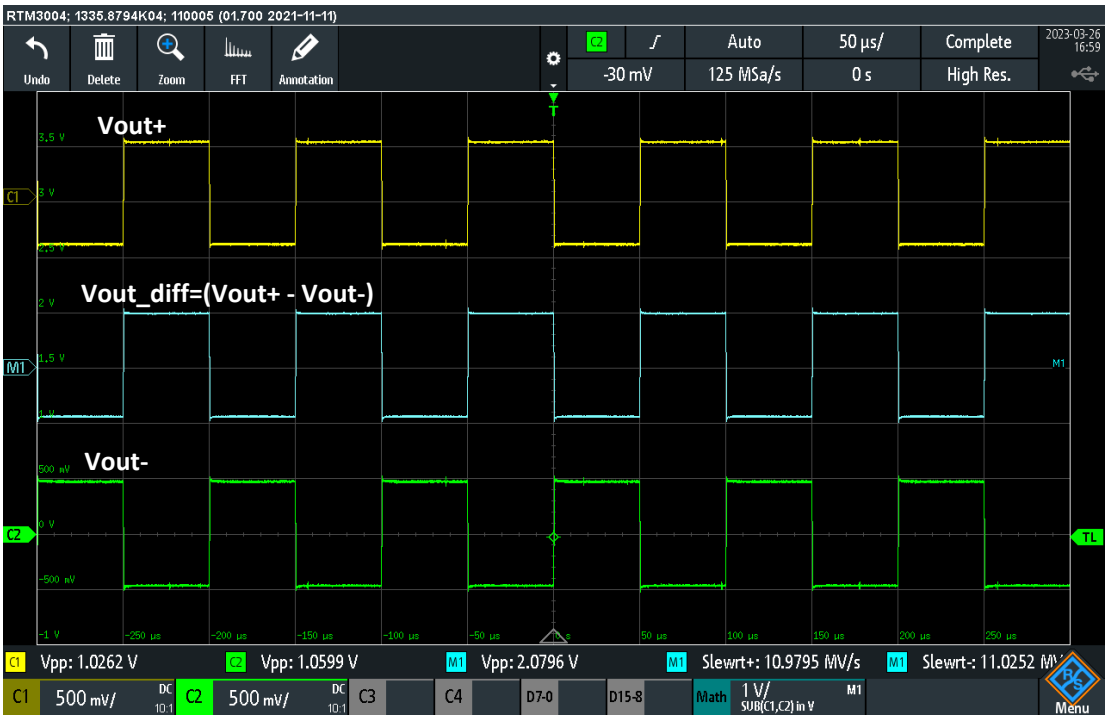

Figure 4.20: Large signal-step response of the CFIA after the optimization.

programmed gain settings were used to evaluate the AC response of the system, as depicted in Figure 4.22. However, it is important to note that the graph shows a gain 6 dB lower than the expected real value. This difference is not problematic and can be ascribed to the test setup, which involves capturing a single-ended output during the

Bode plot measurement.

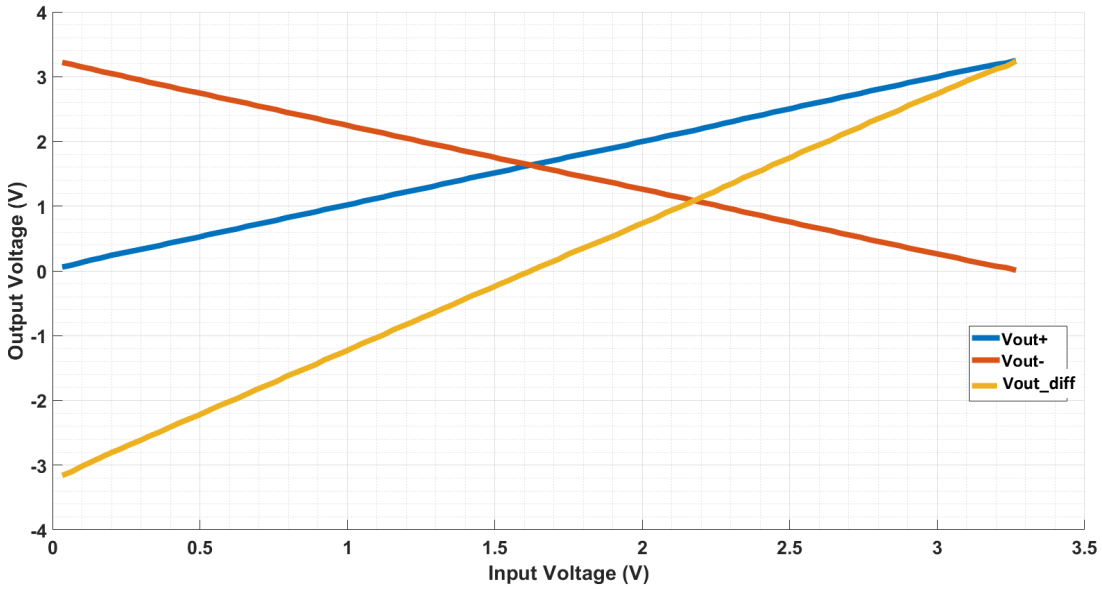

Figure 4.21: Output DC characteristics of the stable CFIA under unity gain configuration after the optimization.

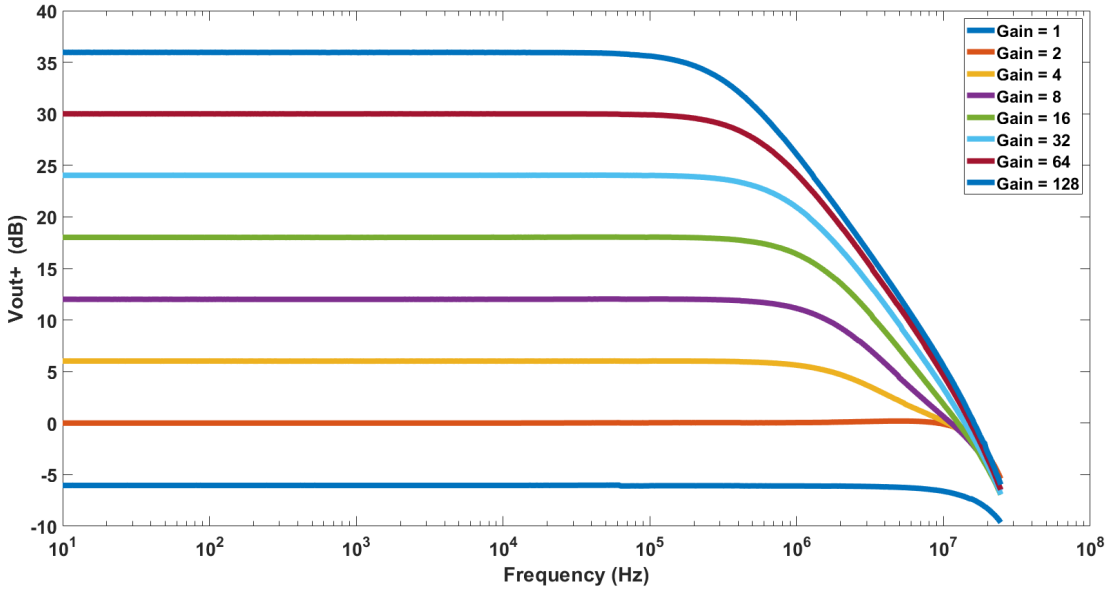

Figure 4.22: Small-signal frequency response of the optimized CFIA under all configurable gain settings

Featuring a class-AB-complementary output stage, the CFIA circuit demonstrated an output common-mode range near the supply rails, as shown in Figure 4.23. This test used a smaller sinusoidal signal with 250 mVp-p amplitude and 1 kHz frequency, with the CFIA gain set at 16. Note that the limitation on the output signal is due to the output stage, and not the input characteristics

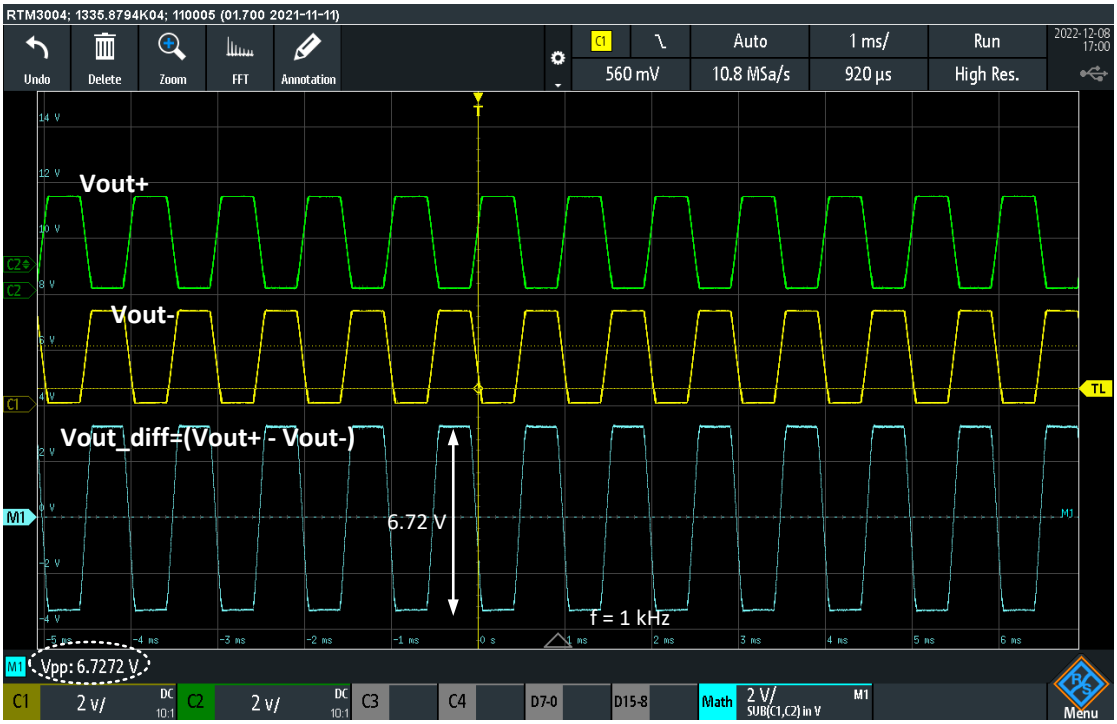

Figure 4.23: Output dynamic range of the CFIA showing the rail-to-rail properties of the class-AB output stage.

The differential input range is evaluated by varying the amplitude of a differential sine input, keeping the frequency low at 100 Hz to isolate the output stage test from the input constraints. Determination of the THD value reveals that a $2\,V_{p-p}$ input range, centered around $V_{CM} = 1.65\,V$, offers optimal linearity, as illustrated in Figure 4.24. Again, this linearity is comparable to the THD quality of the test signal.

The following discussion implies that the nonlinearity of a CFIA or any CMOS amplifier can be inferred from the THD measurements. This correlation is largely due to the statistical relationship among various CFIA performance metrics. For example, in Figures 4.10 and 4.11, the CFIA showed oscillatory output behavior with a completely nonlinear input range. This led to a significantly high THD, as shown in Figure 4.12, owing to the harmonic distortion. However, after the self-X performance optimization loop, the THD improved significantly, suggesting a linearized output response, including step and sinusoidal responses, and stable frequency response, as shown in Figures 4.17, 4.19, 4.20, 4.22, and 4.23. Thus, the THD-based optimization approach has been practically proven to effectively enhance various performance aspects of the CFIA concurrently.

Table 4.2 contrasts the performance of the CFIA between its extrinsic and intrinsic evolutions. The intrinsic differential DC gain is inferred from the closed-loop gain

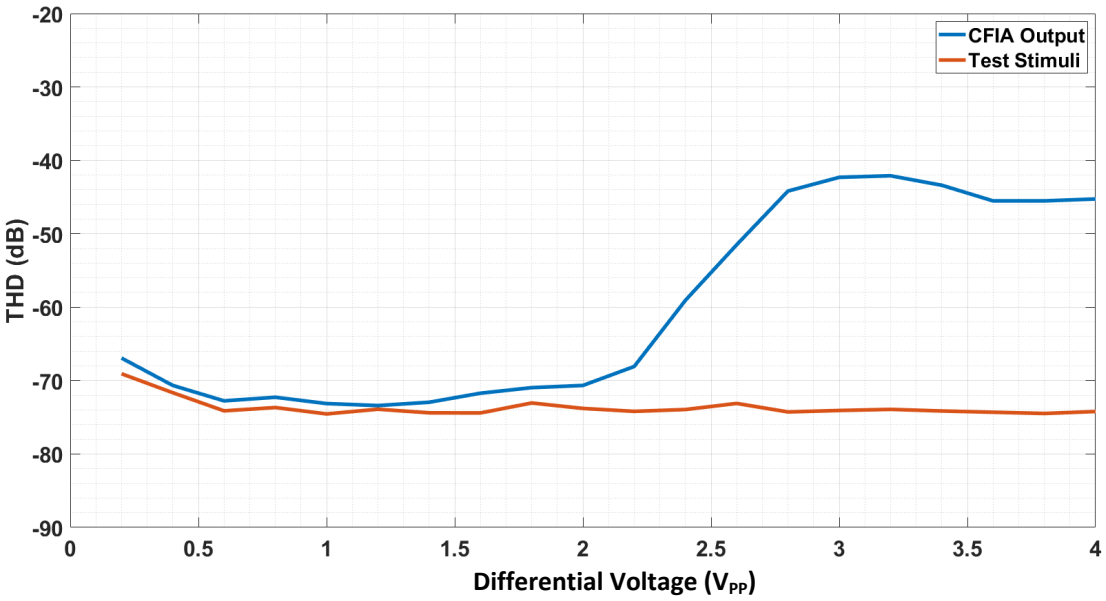

Figure 4.24: Dynamic input range of the CFIA after the optimization at $T = 25\,°\mathrm{C}$ and $V_{DD} = 3.3\,\mathrm{V}$.

error, because the detachment of the feedback network from the amplifier core is unfeasible. The comparison reveals noticeable differences between the extrinsic and intrinsic results, which are attributed to changes in post-manufacturing. One potential cause is the inductance effect from the package leads and bonding wires, potentially leading to oscillations, especially considering that this is our first prototype using XFAB technology. The fourth column of the table shows the performance of the CFIA using the default configuration from the extrinsic optimization. Owing to the inherent instability and oscillation in this setting, precise characterization of the CFIA performance is challenging. However, optimization using our proposed method successfully determined an optimal configuration, significantly improved the CFIA performance. This different configuration also explains the variance between simulated and actual power, as the algorithm stabilizes the system by shifting the first nondominant pole in the CFIA driver stage using increased currents. The output stage, with fixed-size transistors, alters its poles by boosting transconductance (g_m) via higher current. Additionally, the algorithm augments the compensation capacitor, thereby contributing to a reduced slew-rate measurement. This capacitor varies from 0.35 pF to 2.35 pF in 0.25 pF steps. The extrinsic evaluation's average was 0.850 pF, while the intrinsic assessment yielded an average of 2 pF. Notably, this research primarily aimed to develop a software and hardware concept for reconfigurable electronics, enabling the restoration of degraded circuits with minimal

system performance setup cost.

Table 4.2: CFIA characteristics based on extrinsic and intrinsic optimization solutions ($V_{DD} = 3.3\ V$, $V_{CM} = 1.65\ V$, $T_{simulation} = 27\ °C$, $T_{measurement} = 22\ °C$).

CFIA Design Parameter	**Schematic Level**	**Post-Layout Level**	**Chip Level Before Optimization**	**Chip Level Mean of 10**
Differential DC gain (A_{VD})	94.80 dB	94.73 dB	N/A	$>$ 80 dB
Gain–bandwidth product (GBW)	47.75 MHz	39.41 MHz	N/A	$>$ 10 MHz$*$
Phase margin (PM)	73.22°	60.47°	$<$ 0°	$>$ 60°
Slew rate (SR)	$\pm$63.38 V/μs	$\pm$60.34 V/μs	N/A	$\pm$11 V/μs
PMM output frequency (f_{ck})	347.18 kHz	377.48 kHz	700 kHz	3.1 MHz
Static power dissipation (P_D)	4.17 mW	4.16 mW	9.9 mW	53 mW
Input Dynamic Range	Rail-to-rail	Rail-to-rail	N/A	Rail-to-rail
Output Dynamic Range	Rail-to-rail	Rail-to-rail	N/A	Rail-to-rail

* The Bode plot capability of the utilized MSO (Rohde & Schwarz 3004) is limited to 10 MHz due to its signal generator; therefore, the CFIA's gain bandwidth is expected to be higher.

Repeating the optimization process without power monitoring revealed an average CFIA power consumption of 80 mW to achieve the same THD value of -72 dB. This underscores that integrating power monitoring yielded a 34% increase in power efficiency, which is a critical benefit for power-sensitive applications such as sensor nodes reliant on energy harvesting or batteries. Additionally, lowering the current enhances device longevity by mitigating current-density limitations in chip interconnections, where excessive current can lead to failure due to electromigration.

To confirm the differences between the designed and fabricated chips, a configuration from the intrinsic optimization was applied to the extrinsic evaluation. This revealed a clear disparity in power consumption: 15 mA for intrinsic runs and 24 mA for extrinsic runs. Table 4.3 compares the CFIA performance with this configuration with the data in Table 4.2 data.

Notably, the extrinsic evaluation is conducted at the typical mean corner of the processing module, which differs from the actual fabrication conditions. A Monte Carlo simulation around this solution was conducted for a more accurate comparison; however, the deviation still fell outside the intrinsic region, as illustrated in Figure 4.25 for the recorded power dissipation.

Table 4.3: Extrinsic evaluation of the intrinsically optimized configuration showing the deviation between the simulated and fabricated chip under the same measurement conditions ($V_{DD} = 3.3\ V$, $V_{CM} = 1.65\ V$, $T = 22\ °C$).

CFIA Design Parameter	**Intrinsic Evaluation**	**Extrinsic Evaluation**
Differential DC gain (A_{VD})	> 80 dB	100 dB
Gain–bandwidth product (GBW)	> 10 MHz	39.5 MHz
Phase margin (PM)	$> 60°$	82°
Slew rate (SR)	$\pm 10.4\ V/\mu s$	$\pm 71\ V/\mu s$
PMM output frequency (f_{ck})	2.98 MHz	5.72 MHz
Static power dissipation (P_D)	49 mW	79.2 mW
Input Dynamic Range	Rail-to-rail	Rail-to-rail
Output Dynamic Range	Rail-to-rail	Rail-to-rail

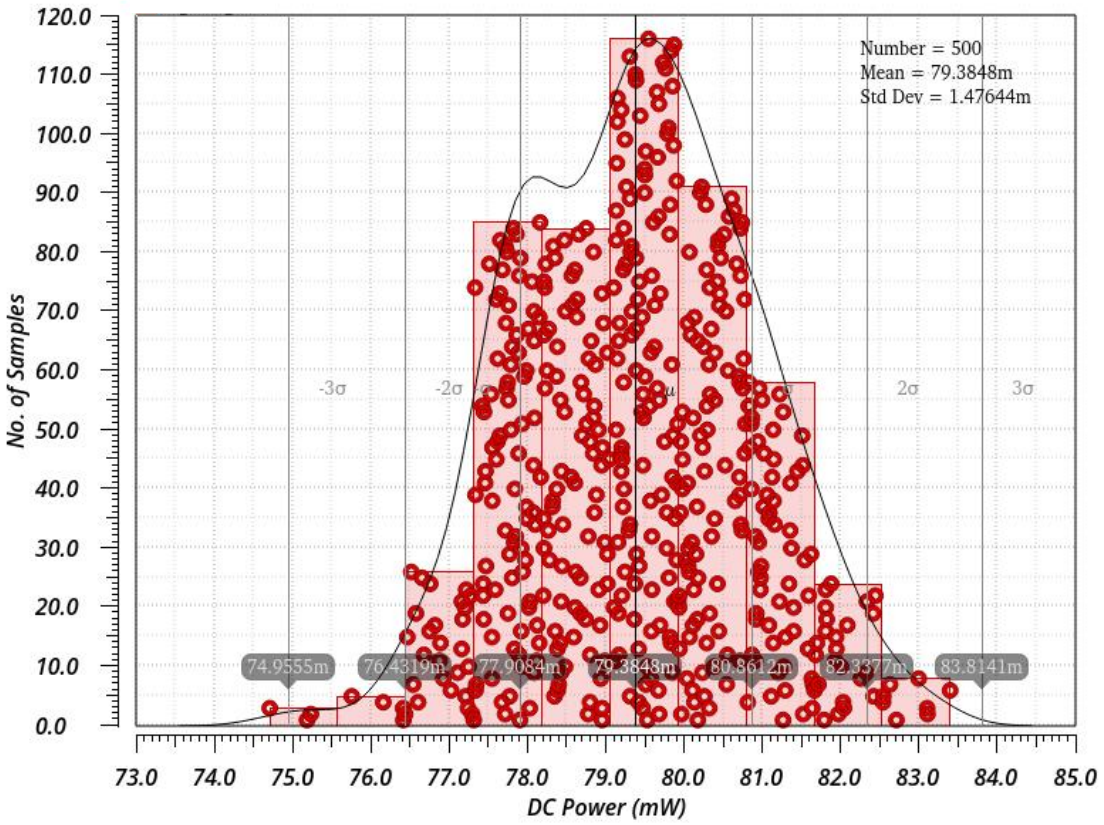

Figure 4.25: MC simulation around the optimization configuration imported from the intrinsic evaluation.

In the realm of recent developments, a fully differential CFIA circuit for biomedical impedance-spectroscopy applications was introduced in [355], using 180 nm CMOS technology. This circuit, with a fixed gain of four, reached a -3 dB bandwidth of 5.83 MHz and a slew rate of 8.3 V/µs, driving a 1.33 pF capacitive load. Its THD is measured at -38 dB with a 60 mVp-p differential signal at 10 kHz, and performance degradation was noted at a 100 mVp-p differential range. Running on a single 1.8 V supply, it consumed

4.795 mW.

In our study, the CFIA achieved a THD of -72 dB at 1 Vp-p and 1 MHz. As depicted in Figure 4.22, it has a −3 dB bandwidth of approximately 3 MHz at a gain of four, a slew rate of 11 V/µs with nearly 15 pF load, and offers eight programmable gains. However, it requires 53 mW on a 3.3 V supply and occupies a larger layout area of 1.6 mm × 0.38 mm, compared to the 119.5 µm × 254.6 µm in [355].

Comparatively, the commercial LMP8358 CFIA by Texas Instruments features an 8 MHz bandwidth at a gain of 10, driving 10 pF and 10 kΩ loads. It provides seven programmable gains (20 to 1000) and uses a parallel SPI protocol. The device automatically adjusts the compensation capacitor for bandwidth optimization, handles a ±100 mVp-p differential signal, and consumes 6.27 mW. It is particularly suitable for low-frequency differential sensor signals because of its high gain and low offset-voltage correction.

The MCP6N11 CFIA by Microchip, another commercial option, offers five gain levels (1, 2, 10, and 100), a 500 kHz unity gain bandwidth, and operates on 1.8 V to 5.5 V supply. At 3.3 V, it consumes 2.64 mW and supports a rail-to-rail input differential range.

4.1.3.4 Dynamic Performance Optimization

To carry out dynamic in-field optimization, the optimization is performed by considering the change in temperature and supply voltage variation [356]. Figure 4.26 depicts the LAB demonstration setup. The Binder MK53 climate chamber is employed for temperature modulation, while the PeakTeck 6181 programmable power supply is utilized to vary the supply voltage. The FPGA boards are situated within the chamber, acknowledging the uncertainty inherent to the optimization system, specifically regarding the test stimuli and ADC as an observer device.

The same stimuli signal that was previously used in the optimization under static conditions is used in this experiment. to address the impact of dynamic operating conditions on the CFIA performance, the chip temperature in the first investigations is varied in a range from $T = -20\,^{\circ}\mathrm{C}$ to $T = 40\,^{\circ}\mathrm{C}$. Additionally, the supply voltage is dropped from 3.3 V to 2.6 V. Each optimization process is replicated three times to avoid the lucky shot solutions.

The experimental results, illustrated in Figure 4.27 through the error bar graph and

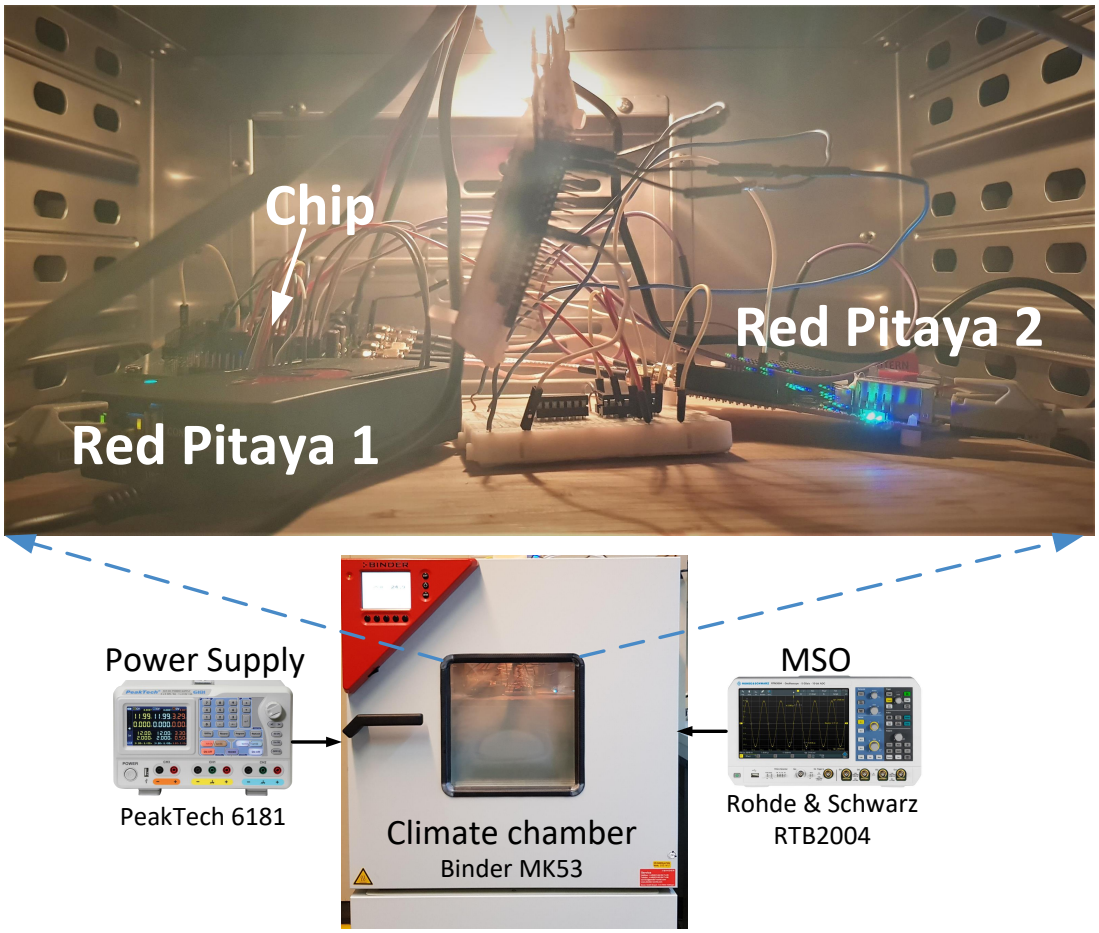

Figure 4.26: The dynamic optimization setup using Binder climate chamber.

in Figure 4.28 via optimization convergence curves, demonstrate the effectiveness of in-field optimization. This approach effectively tunes CFIA settings to optimize THD values while reducing power consumption. The results highlight the robustness and adaptability of the optimization method under dynamic environmental conditions.

In the next experiment, the input offset voltage digital-autozeroing is evaluated at three distinguished temperatures $T = -20\,°C$, $T = 25\,°C$ and $T = 40\,°C$ with V_{DD}= 3.3 V. The corresponding results are shown in Figures 4.29, Figure 4.30 and Figure 4.31, respectively. The slew rate distortion in the clock signal is attributed to the sampling rate of the DSO for the selected recording time. The EOC signal marks the start and end periods of the offset calibration. Twelve clock periods are required to reach to the final value as explained in Chapter 3, where in this test, the clock frequency is set to 1 kHz. The in-amp inputs are tied to V_{CC}=0.5 V_{DD}, while the outputs reflect the offset voltage at a gain set to 128. The results are summarized Table 4.4.

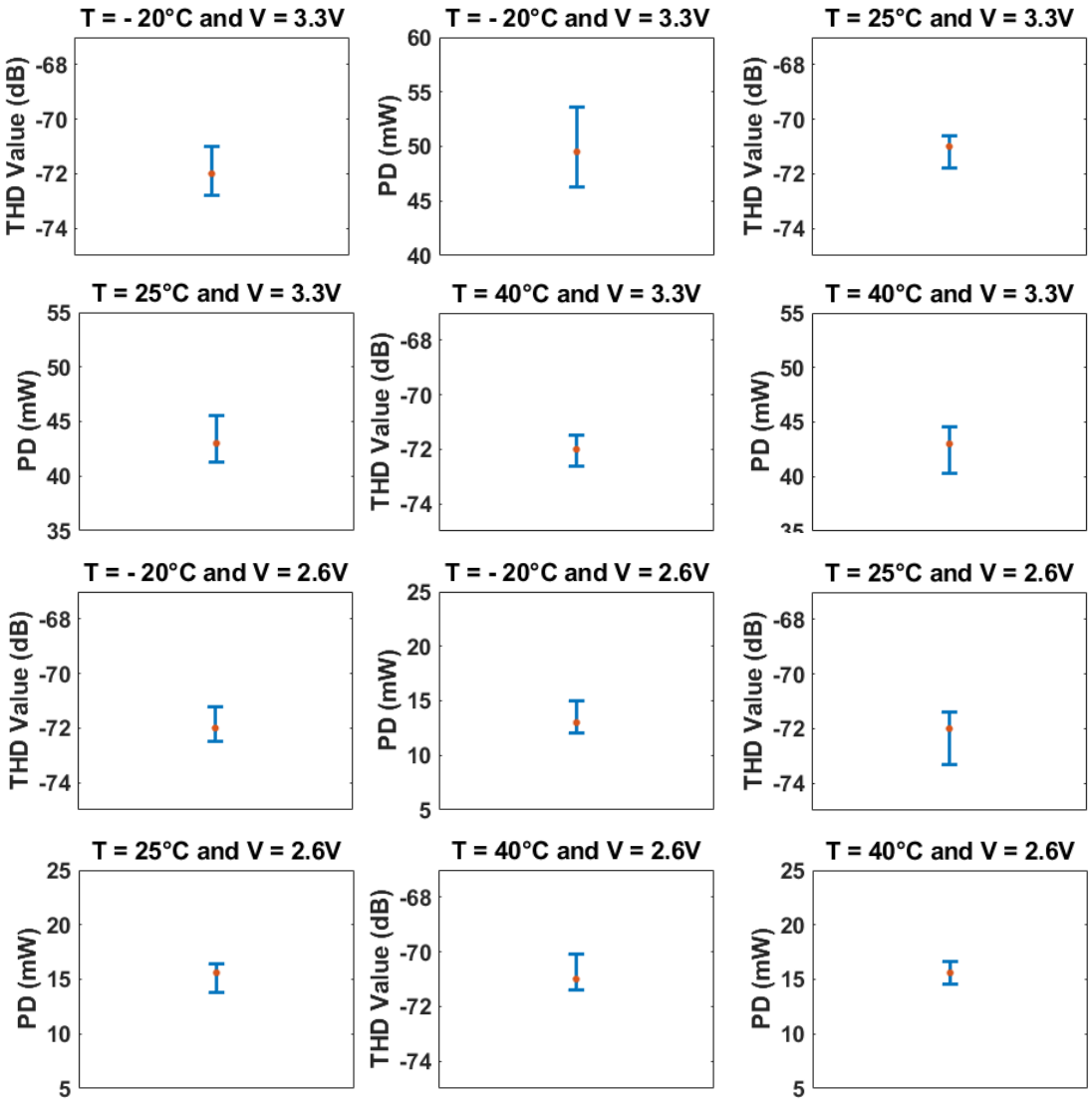

Figure 4.27: Error paragraph for dynamic optimization.

Temperature	V_{os} **Before Compensation**	V_{os} **After Compensation**
−20 °C	2.979 mV	0.231 mV
25 °C	2.818 mV	0.0882 mV
40 °C	2.832 mV	0.0788 mV

Table 4.4: Temperature vs. voltage offset (Vos) before and after compensation at $V_{DD} = 3.3V$

4.1.3.5 CFIA Optimization Summary

An efficient and cost-effective method is employed for the intrinsic evolution of the configurable CFIA, with the aim of simplifying the performance evaluation setups for AFEs with self-X properties. Preliminary tests, based on post-layout simulations with extrinsic optimization configurations revealed the degraded performance and instability of the

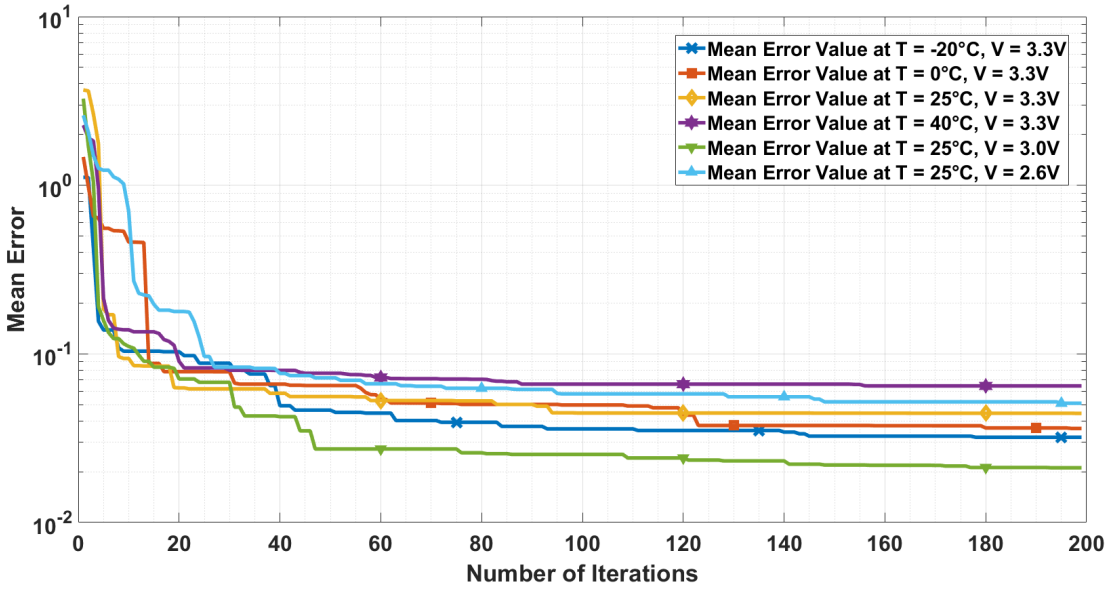

Figure 4.28: Optimization conversion error under dynamic operating conditions

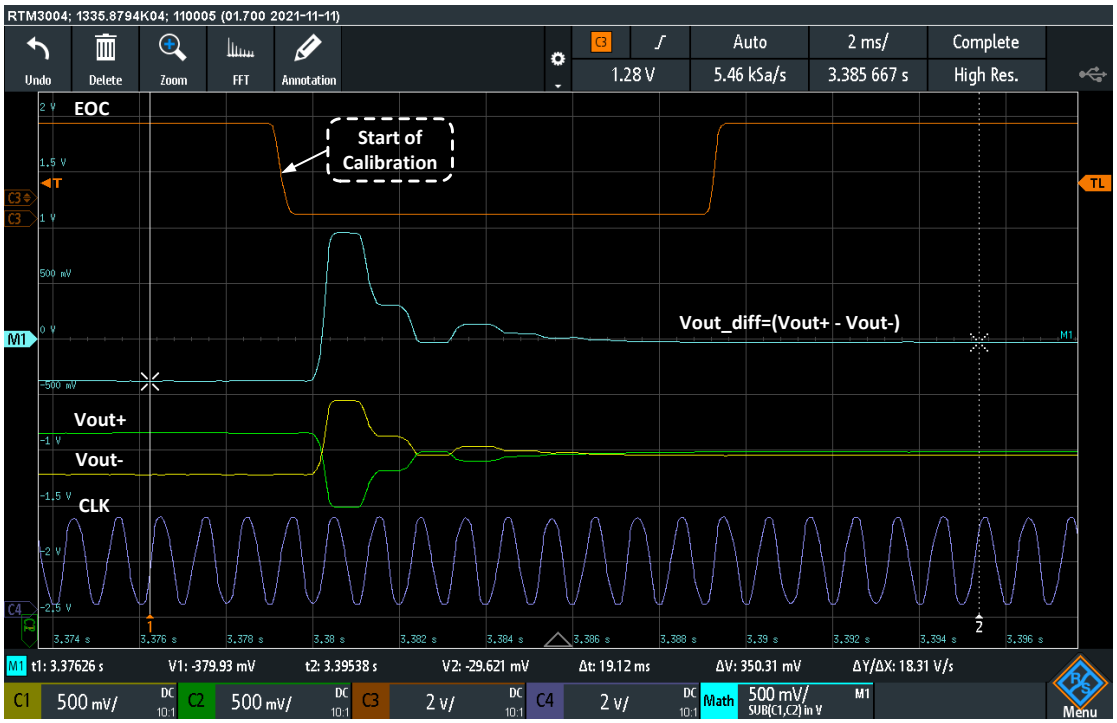

Figure 4.29: Offset voltage autozeroing at $T = -20\,^{\circ}\mathrm{C}$ and $V_{DD} = 3.3V$

CFIA. Subsequent in-field optimization, utilizing THD and power monitoring with the ERPSO algorithm, identified the optimal configuration for the CFIA linear operation. This highlights the advantages of the self-X properties in sensory electronics for yield enhancement. Without self-X capabilities, this batch may have been discarded, thereby incurring high fabrication costs. The ERPSO algorithm, executed on Red Pitaya FPGA boards, leverages the boards' DACs and ADCs for data acquisition and assessment of

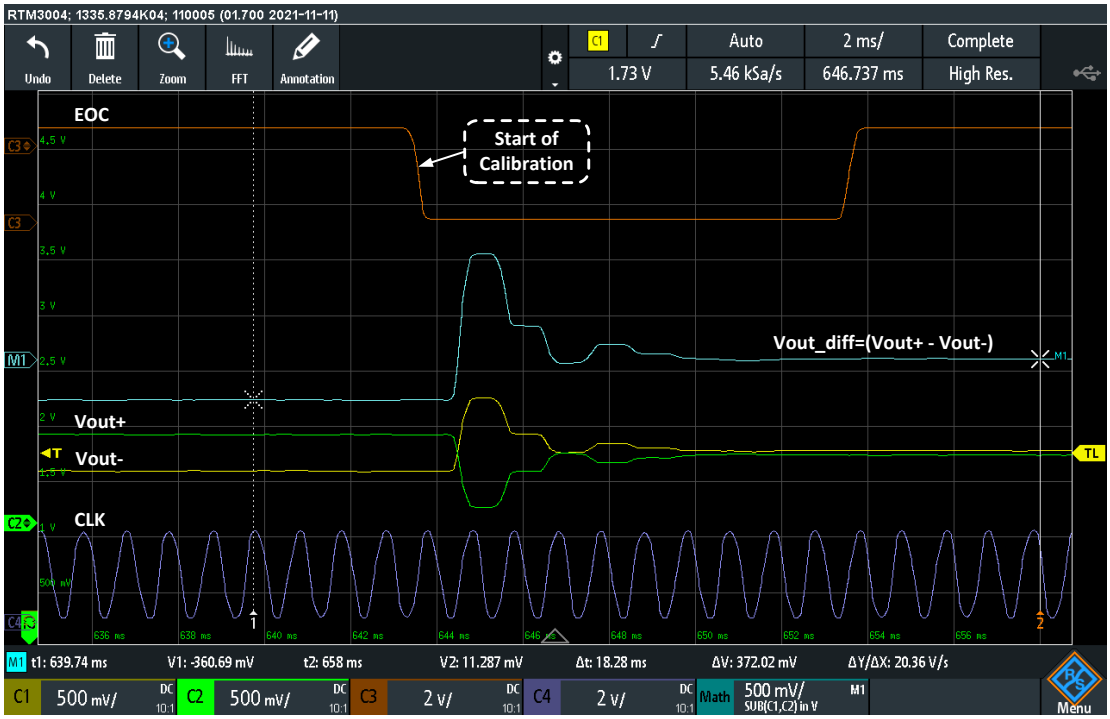

Figure 4.30: Offset voltage autozeroing at $T = 25\,^{\circ}\mathrm{C}$ and $V_{DD} = 3.3V$

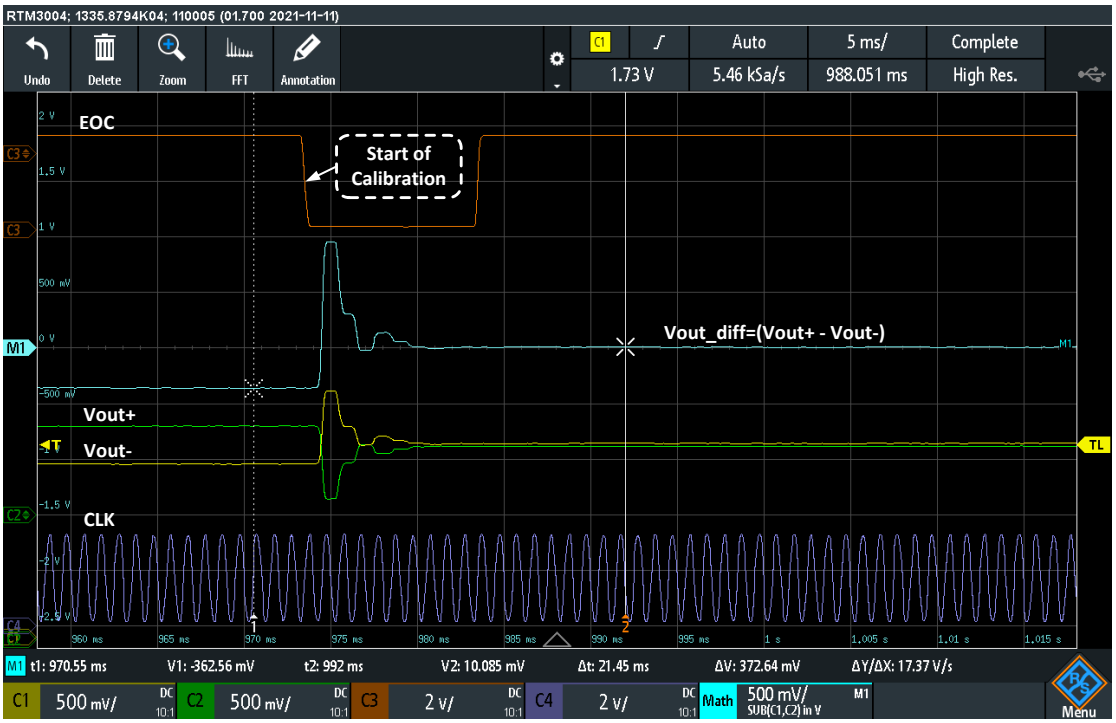

Figure 4.31: Offset voltage autozeroing at $T = 40\,^{\circ}\mathrm{C}$ and $V_{DD} = 3.3V$

the CFIA. Due to the correlation between various amplifier characteristics and THD, the THD-based optimization effectively streamlined the number of assessment units needed for performance tuning. The stability is confirmed using a pulse test after the optimization. A single sinusoidal signal stimulus was predominantly used, which proved to

be efficient for the amplifier enhancement. The power monitoring aided the ERPSO in finding power-efficient solutions, enhancing power efficiency by 34% compared with non-monitored methods, and contributing to extended device longevity and energy efficiency. Optimized for a 1 MHz, 1 Vp-p range, the CFIA achieved an average THD of -72 dB. Its dynamic input range and transient capabilities suit various sensors and measurement applications, including impedance spectroscopy and TMR sensors. The offset voltage autozeroing capability could be a useful tool not only for compensating the in-amp inherent offset voltage but also for correcting the offset voltage of the sensor bridge without extra effort on the sensor side.

Optimization tests are conducted under static and dynamic conditions, by altering the supply voltage and temperature within the limits of the FPGA board specifications. The self-X properties in sensory electronics are key to their reliability and adaptability, aligning with the demands of Industry 4.0. The best intrinsic solutions for the nominal supply operation are listed in Table A.1.

4.2 Active Filter Testing

4.2.1 Initial Test

The block diagram of the filter test setup is illustrated in Figure 4.32. Initially, the shadow register of the filter is examined, as shown in Figure 4.33. It is important to note that the filter memory lacks externally accessible pins from the chip. Instead, the data is serially transferred from the preceding memory block of the in-amp. This test is critical for ensuring the safe arrival of the configuration data.

In the subsequent test, the filter is configured using the data obtained from the post-layout extrinsic evaluation. This configuration sets the cut-off frequency at 2.6 MHz. A sinusoidal signal, characterized by a 1 kHz frequency and a 1 Vp-p amplitude, is applied to the filter under typical operating conditions (laboratory temperature = 24 °C and V_{DD} = 3.3 V). The resulting output is presented in Figure 4.34. As observed in the figure, the output amplitude demonstrates a true unity gain within the pass band region of the designed filter. It also exhibited an excellent match in the output differential stage, with a 179.49° phase shift.

The filter, incorporating two amplifier stages, with each stage consuming 13 mA, has

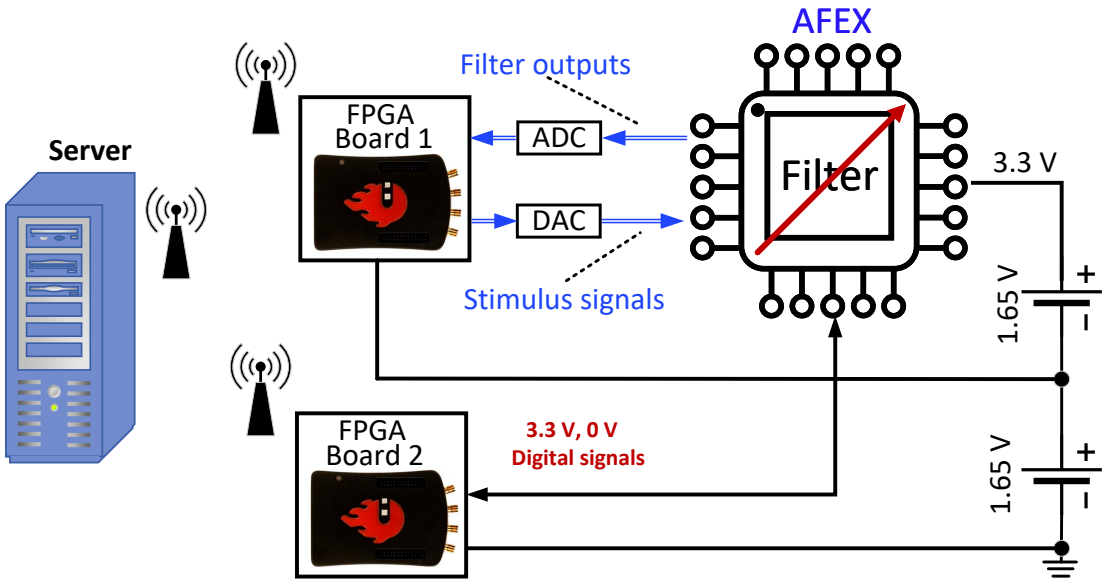

Figure 4.32: Block diagram of the LAB filter test.

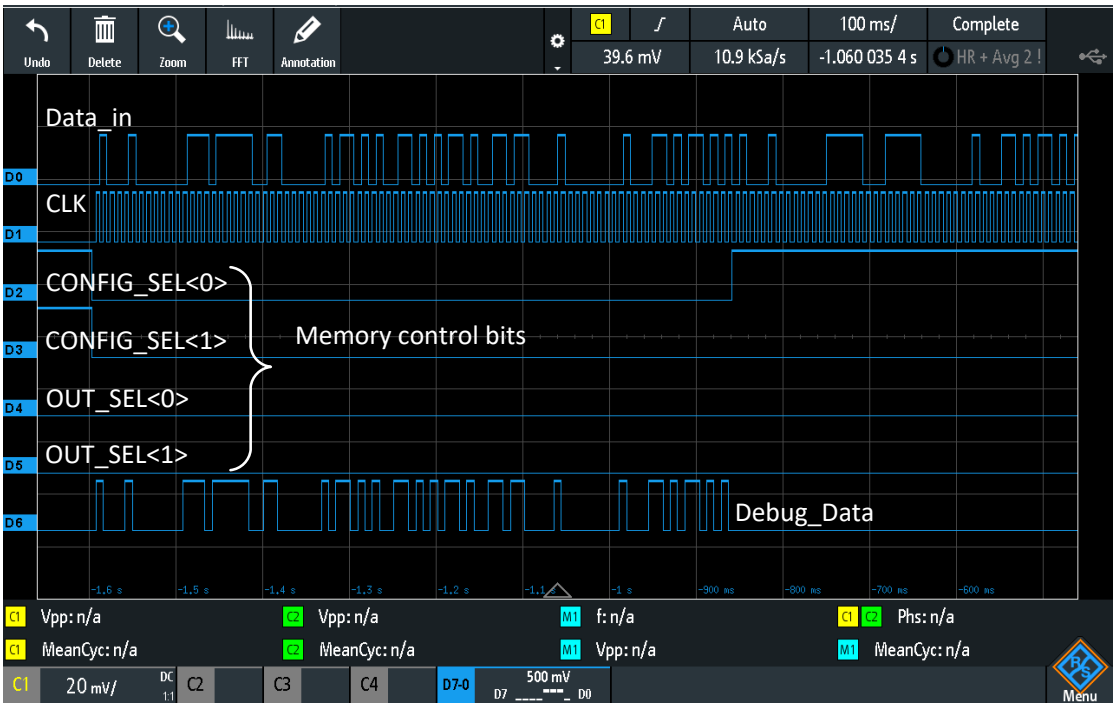

Figure 4.33: Verification test for the filter shadow register memory.

a total current draw of approximately 26 mA at 24 °C. By utilizing the programmable current source, practical experiments have shown that the total current consumption can be effectively reduced to 11 mA, without affecting the filter's operational functionality.

The small-signal AC response is always evaluated using a sinusoidal signal with an amplitude of 100 mV. The results are depicted in Figure 4.35, showing a roll-off of less than -80 dB. This indicates an effective filter order of less than four, aligning with

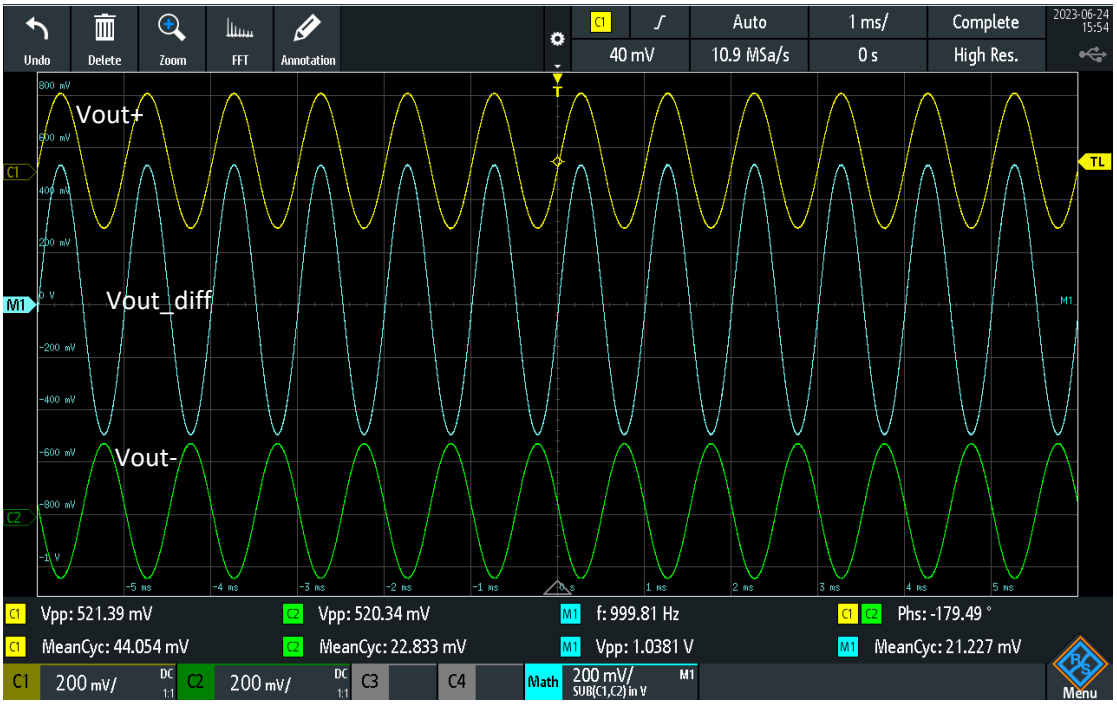

Figure 4.34: Sinusoidal transient response of the filter

post-layout simulation outcomes. Notably, the observed low-frequency gain of -6 dB is attributable to the utilization of a single output during measurement, corresponding to the filter's 0 dB linear differential gain (unity gain).

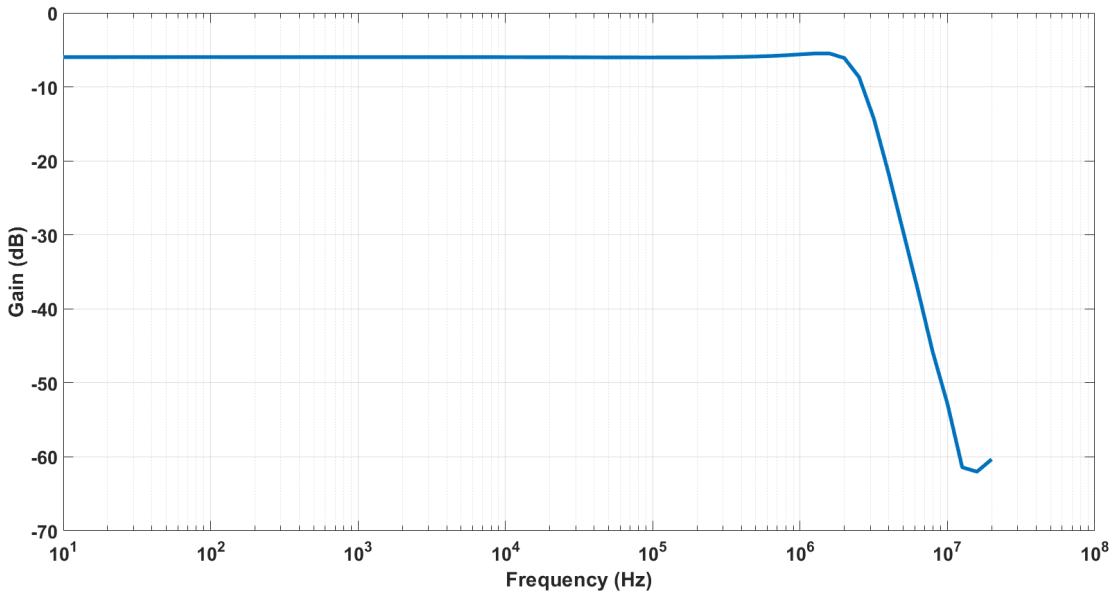

Figure 4.35: Small-signal AC response of the filter using one of the extrinsic patterns at typical operation condition: T= 22 °C and V_{DD}= 3.3 V.

Given the importance of the designed filter stability under unity-gain conditions, the impulse response is verified by applying a square signal. While stability predictions

are feasible based on the peaking observed in the small signal AC response, it remains a standard practice to excite the filter/amplifier with a sharp-edged pulse signal to empirically confirm the stability. As depicted in Figure 4.36, the results ensure the stability of the filter and validate its Butterworth performance, as evidenced by a smooth transition to the settling region.

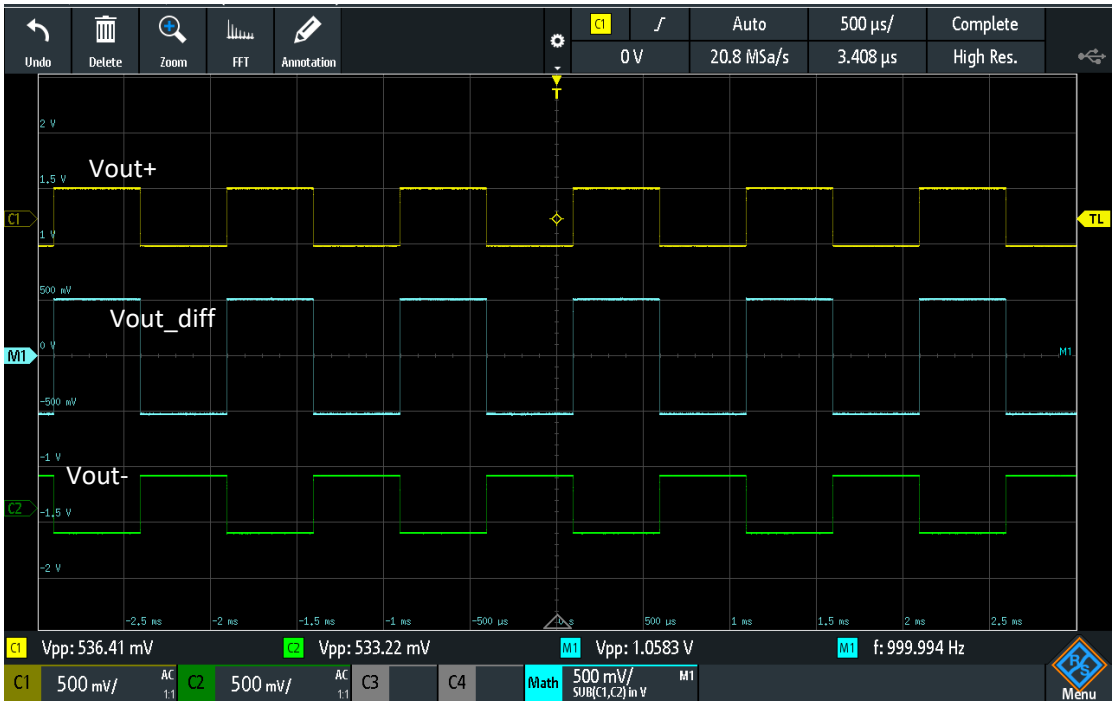

Figure 4.36: Impulse response of the filter confirming the stability using one of the extrinsic patterns at typical operation condition: T = 22 °C and V_{DD}= 3.3 V.

As introduced in Chapter 3, two non-intrusive sensors, NIS1 and NIS2, utilize the same filter configuration as the temperature sensor. These sensors have been tested at T=24 °C, and the results are displayed in Figures 4.37, 4.38, and 4.39, respectively. The outcomes reveal the anticipated quasi-digital output form; the frequency-modulated signal facilitates straightforward conversion to a digital equivalent weight (F/D) using the Red Pitaya board. In addition, all sensors are equipped with an enable control signal to optimize power consumption.

The correlation between the filter bandwidth and non-intrusive sensors (NISs) is investigated across various filter configuration settings. As illustrated in Table 4.5, there is a proportional, albeit nonlinear, correlation between the NIS frequencies and the filter bandwidth. This nonlinearity can be addressed by employing a regression model to estimate the cutoff frequency indirectly. Notably, it is observed that below 1 kHz, Sensor1

Figure 4.37: The signal output from non-intrusive sensor1 using one of the extrinsic patterns at typical operation condition: T = 24 °C and V_{DD}= 3.3 V.

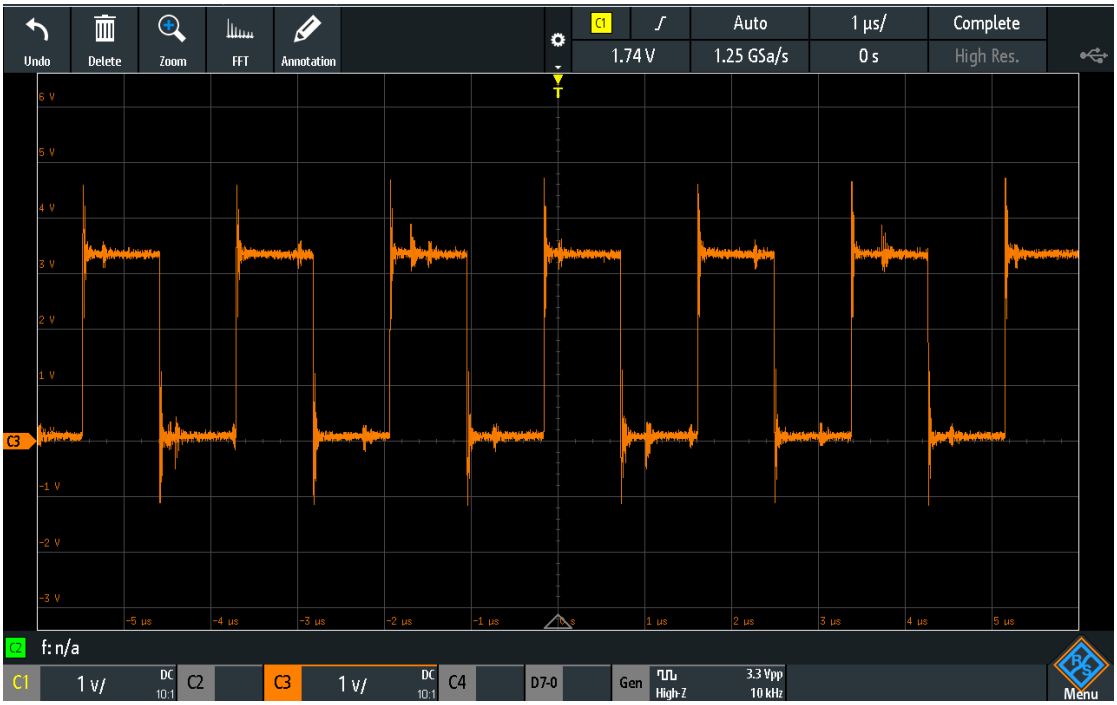

Figure 4.38: The output signal from non-intrusive sensor2 using one of the extrinsic patterns at typical operation condition: T = 24 °C and V_{DD}= 3.3 V.

exhibits saturation in its readings, whereas Sensor2 continues to vary proportionally. Additionally, the on-chip temperature sensor proves valuable in validating the regression model, enabling indirect prediction of the filter frequency under dynamic operating

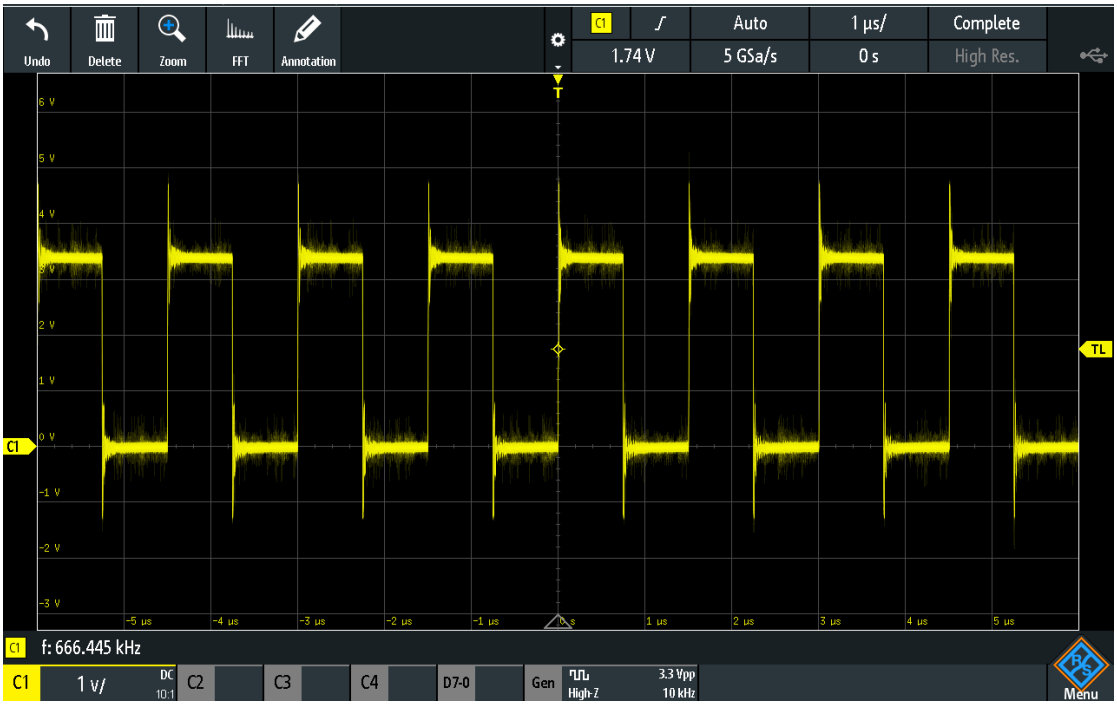

Figure 4.39: The temperature sensor output signal at T = 24 °C and V_{DD}= 3.3 V.

conditions.

Table 4.5: Filter bandwidth and non-intrusive sensors outputs at T = 24 °C and V_{DD}= 3.3 V.

Filter Bandwidth	Sensor1	Sensor2
10 MHz	24.6 MHz	6.37 MHz
6.7 MHz	7.51 MHz	5.44 MHz
2.6 MHz	5.03 MHz	4.49 MHz
234 kHz	761.3 kHz	1.66 MHz
140 kHz	515.26 kHz	1.29 MHz
37.2 kHz	185.5 kHz	562.5 kHz
1.7 kHz	26.62 kHz	80.5 kHz
427 Hz	33.71 kHz	66.7 kHz
276 Hz	33.03 kHz	30.91 kHz

4.2.2 Filter Dynamic Performance

In this experiment, the effect of temperature on the AC performance of the filter is assessed. Initially, the filter's configuration pattern is intrinsically set at T = 24 °C, to establish the cutoff frequency at specific points: minimum (67 Hz), 1 kHz, 10 kHz, 100 kHz, 1 MHz, 5 MHz and 10 MHz. Subsequently, the filter assembly is placed within a climate chamber, as depicted in Figure 4.40, where the temperature is systematically varied from T = −20 °C to T = 40 °C.

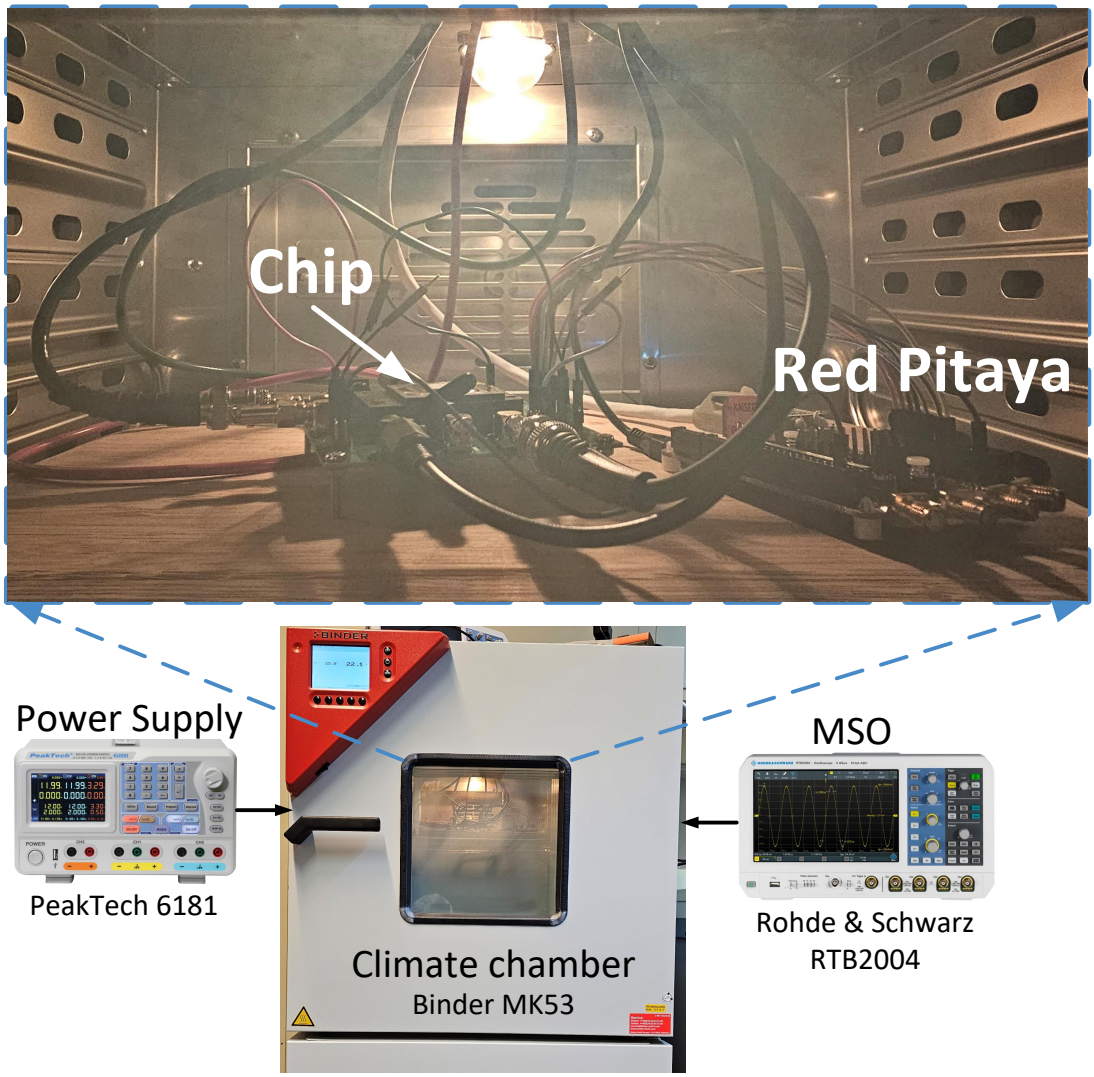

Figure 4.40: Dynamic test of the filter using the climate chamber.

As shown in Figure 4.41, the filter bandwidth exhibits a temperature-dependent shift. However, due to the design tunability, it can be recentered by reprogramming the MOS resistors. This can be achieved by updating the configuration pattern that controls the weight of the MOS resistors. The results of this recalibration are shown in Figure 4.42. It is evident that the cut-off frequencies are realigned to their nominal values, except for T = 40 °C of a bandwidth of 67 Hz. This suggests that the recoverable filter range at T = 40 °C spans approximately 100 Hz to 10 MHz. Notably, the spectral range is limited to 25 MHz, as constrained by the DSO used in these experiments.

Table 4.6 summarizes the filter bandwidth results before and after the correction, indicating a maximum error of 3% within the recovered range.

Finally, the temperature sensor is tested across a range from −20 °C to 70 °C, with

Table 4.6: The filter cut-off frequency under dynamic temperature test comparing the results before and after tuning

Cutoff Frequency	Cutoff Frequency Deviations		Recentered Cutoff Frequency		Error Before Tuning		Error After Tuning	
	-20 °C	40 °C	-20 °C	40 °C	-20 °C	40 °C	-20 °C	40 °C
67 Hz	28 Hz	89 Hz	66 Hz	89 Hz	58%	33%	1.5%	n.a
1 kHz	478 Hz	1.48 kHz	0.97 kHz	1 kHz	52%	48%	3.0%	0.0%
10 kHz	5.6 kHz	10.7 kHz	9.81 kHz	9.87 kHz	44%	7%	1.9%	1.3%
100 kHz	87 kHz	116 kHz	98 kHz	100 kHz	13%	16%	2.0%	0.0%
1 MHz	800 kHz	1.1 MHz	1 MHz	1.01 MHz	20%	10%	0.0%	1.0%
5 MHz	5.9 MHz	4.85 MHz	5.01 MHz	5.01 MHz	18%	3%	0.0%	0.0%
10 MHz	11.8 MHz	9.8 MHz	10.2 MHz	9.8 MHz	18%	2.0%	2.0%	2.0%

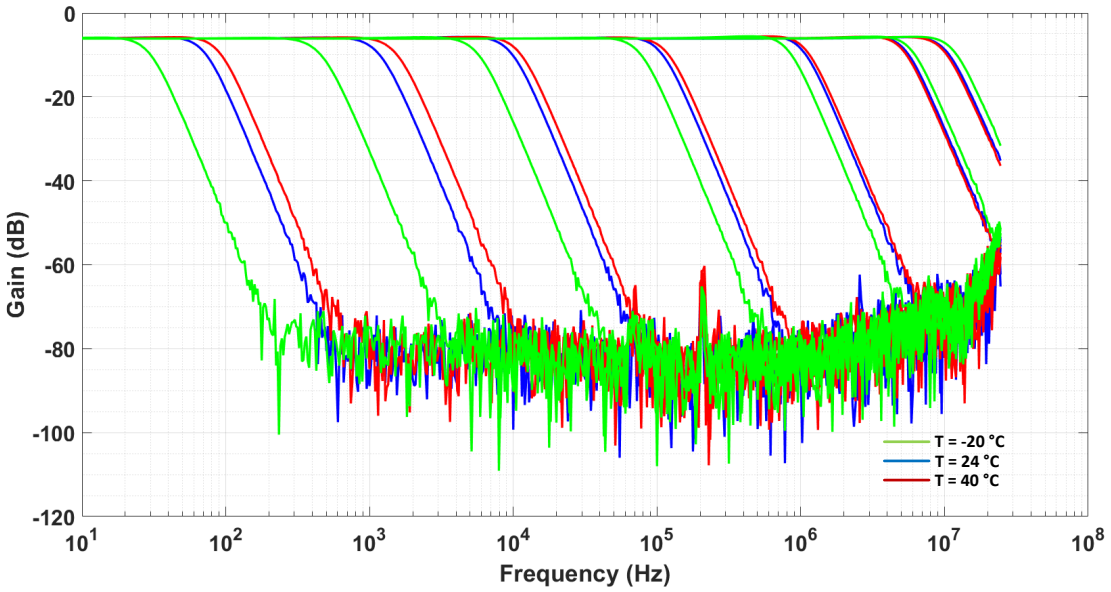

Figure 4.41: The filter small-signal AC response under dynamic temperature change at different cut-off frequencies

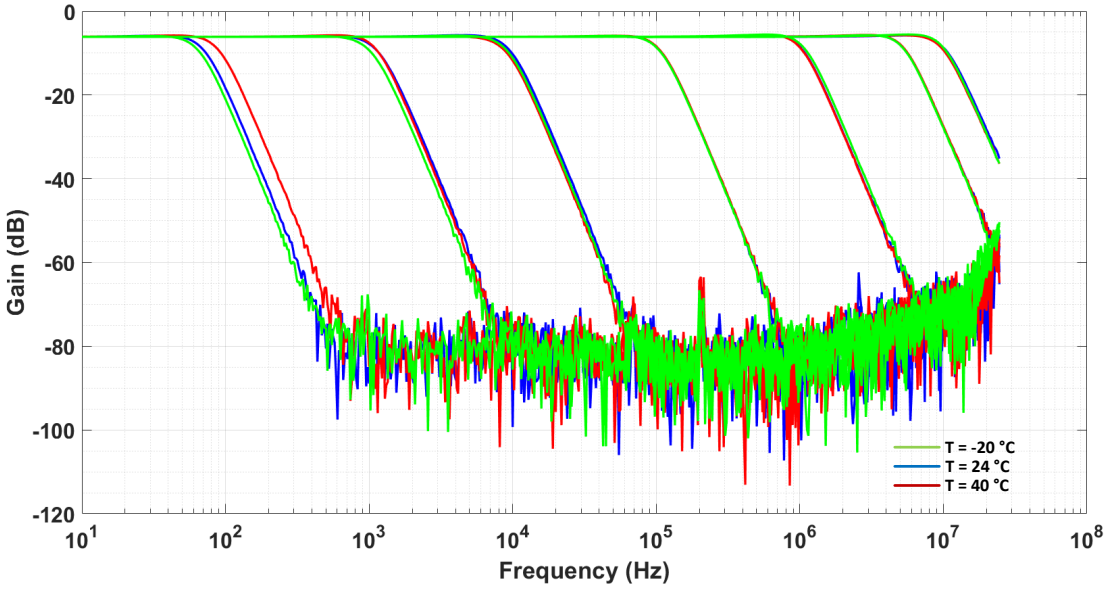

Figure 4.42: The filter small-signal AC response performance under dynamic temperature after bandwidth recovery

increments of 5 °C. The results are presented in Figure 4.43. While the frequency is observed to change proportionally to the temperature, the duty cycle remains consistently approximately 50%.

4.2.3 Summary of the Filter Test

The tested filter demonstrated Butterworth characteristics with an order of less than four. Within the tested temperature range of −20 °C to 40 °C, the effective tunable

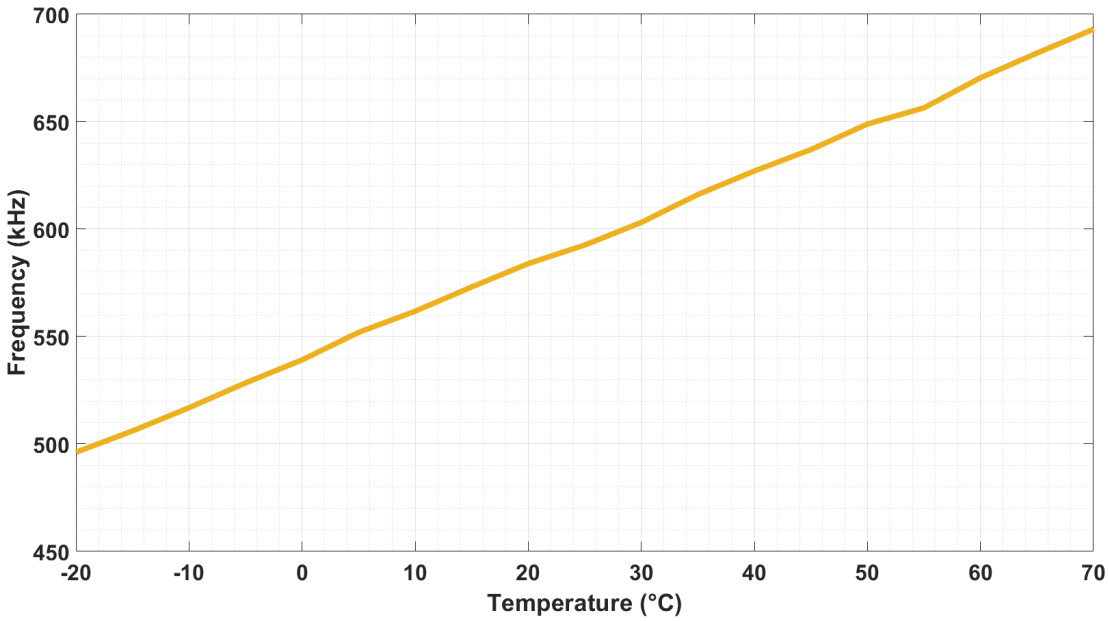

Figure 4.43: Temperature sensor test at V_{DD}= 3.3 V using the climate chamber

range extends from 100 Hz to 10 MHz. This range corresponds to a resolution of 1024 points per decade, aligned with the 10-bit configurable MOS resistor that defines the pole frequency of the filter. Within this specified range, the maximum deviation from the targeted cut-off frequency did not exceed 3%. Additionally, the wide input dynamic range, which is capable of accepting up to a 2 Vp-p differential input signal, makes it suitable for driving the next ADC without further amplification. It can also accommodate an amplified signal from the preceding amplifier. It is important to note that the output stage of the amplifier used for the filter employs a push-pull class AB driver circuit. This configuration endows the filter with a robust driving capability to handle the ADC input load on the filter outputs.

Owing to time constraints, the optimization method using indirect measurements and a regression model has not yet been practically evaluated. Nevertheless, the established correlation found by measurements between the output of non-intrusive sensors and the filter bandwidth offers a promising indication for the application of the proposed methodology. Table A.2.

Chapter 5

System Sensor Application

This chapter introduces a prototype demonstration that demonstrates the integration of the proposed AFEX system with a TMR sensor. The primary objective of this chapter is to validate the functionality of the electrical interface of the proposed AFEX system in actual sensor applications. At the same time, another PhD student at our institute is delving into the exploration of self-X concepts applied to sensor systems across various levels; in this context, the angular decoder is utilized as a complete case of study, giving the opportunity to join self-X work from sensors and sensor electronics to abstract software level [357].

5.1 Experimental Setup

In this experiment, the TMR sensor from Sensitec is employed. Figure 5.1 [358] depicts the functional LAB setup. This TMR sensor, excited by a 3.3 V DC voltage, features two balanced, fully-differential (full-bridges) signals, producing two differential signals offset by 90° (sine and cos) and a common mode voltage centered around 1.65 V. For signal acquisition, two FPGA Red Pitaya boards with two 14-bit ADC in each board are utilized, each processing the amplified and filtered signals from the sensor using two fabricated AFEX chips. In addition, a third FPGA is dedicated to the AFEX configuration.

Although using only two FPGAs for signal acquisition and system configuration is feasible, their ground level is shifted to the common mode voltage of the bridge, whereas the AFEX is referenced to 0V. An alternative solution involves using a DC-level shifter,

which allows the employment of only two FPGA boards. The server unit coordinates the self-X algorithm for the angle computation and anomaly detection. The TMR sensor, mounted on the front of the rotary shaft of the DC motor, is also sourced from Sensitec.

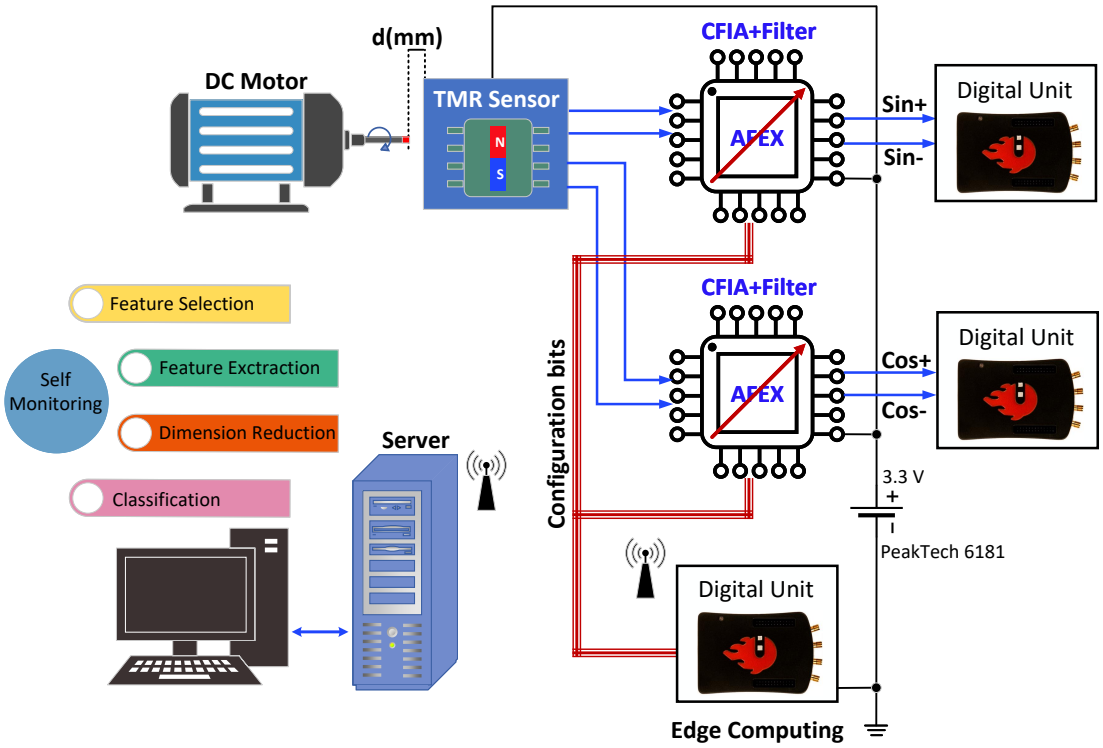

Figure 5.1: Functional setup of the proposed TMR sensor interface.

The details of the TMR readout circuit are presented in Figure 5.2. As mentioned in Chapter 3, the in-amp offset voltage autozeroing feature can be employed for self-compensation of the offset voltage of the bridge sensor rather than altering the sensor bridge, as the work presented in [359]. Comparable techniques include chopper-type amplifiers, as discussed in [360, 361], and the implementation of capacitive coupling techniques, as reported in [362].

The lab setup is depicted in Figure 5.3, demonstrating the complete TMR sensor interface.

5.2 Measurement Results

The filter cutoff frequency is set at 1 kHz, tenfold higher than the maximum frequency anticipated from the DC motor at its highest speed. This configuration ensures that there is no signal attenuation in the TMR outputs. The TMR sensor is initially positioned

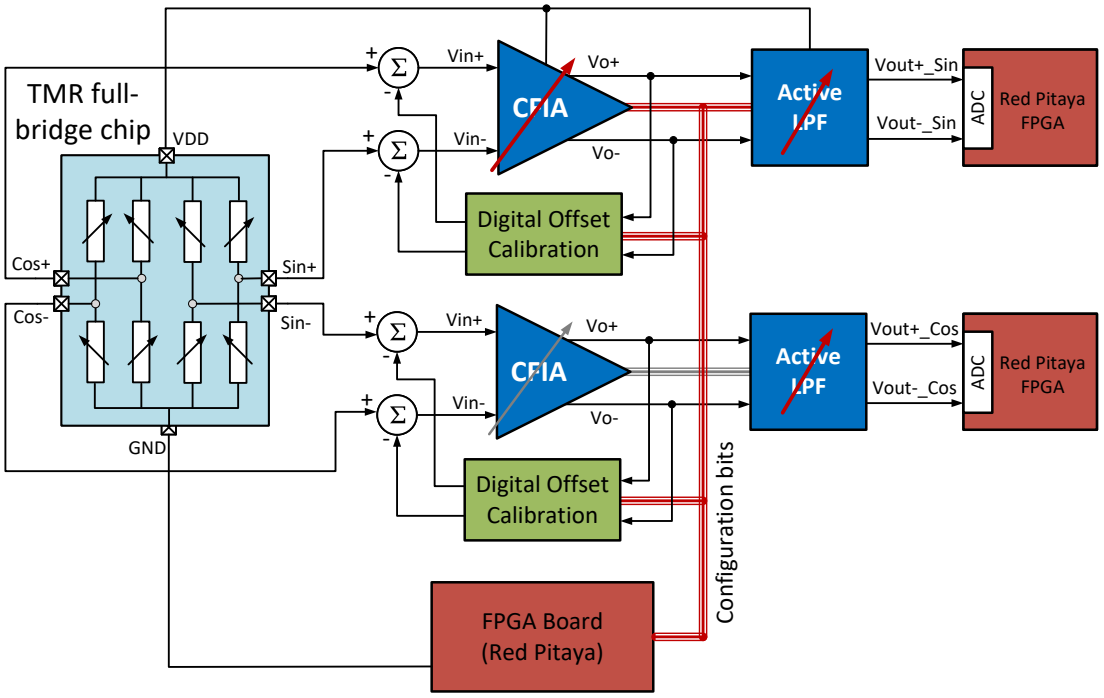

Figure 5.2: Schematic diagram of the proposed TMR readout circuit.

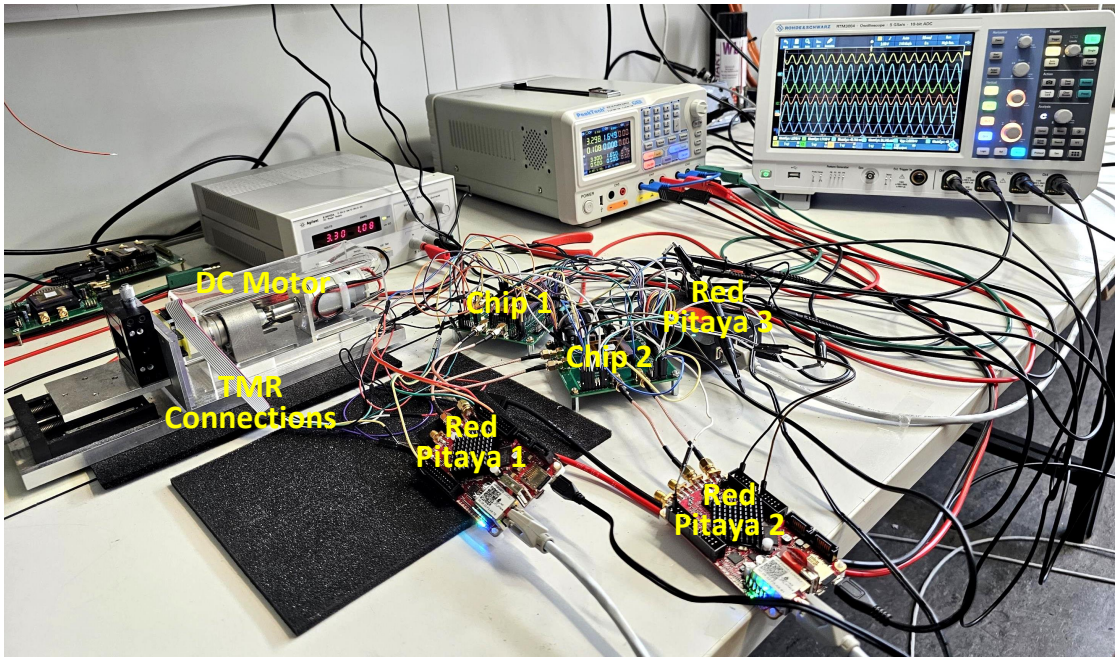

Figure 5.3: LAB setup for TMR interface using the proposed AFEX chip.

at 4 mm from the front of the magnetic detector to the motor shaft. The in-amp gain is initially set to unity to observe the TMR signal without amplification. The in-amp and filter are configured using the patterns obtained from the intrinsic optimization. As depicted in Figure 5.4, the differential outputs are approximately 0.5 Vp-p with a phase shift of 90° indicating true sine and cos signals, whereas the full-scale voltage of the

ADC is 2 Vp-p. Consequently, the gain is adjusted to 4 at this distance and the results are shown in Figure 5.5.

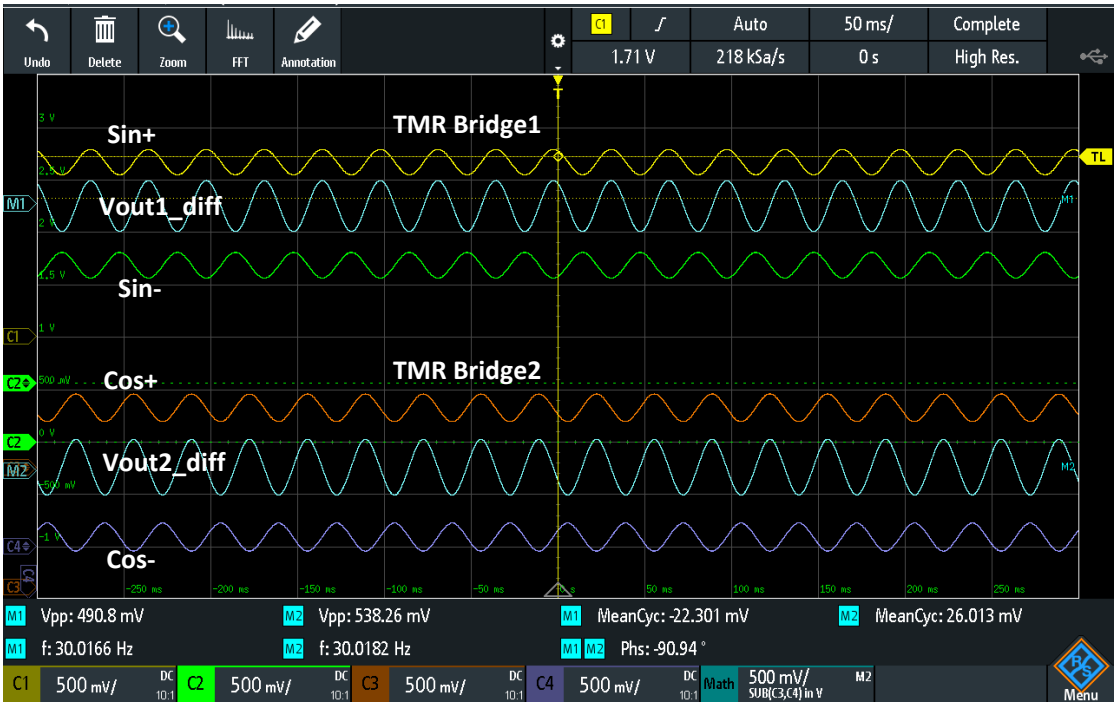

Figure 5.4: TMR sensor outputs at the in-amp gain of unity and distance of 4 mm.

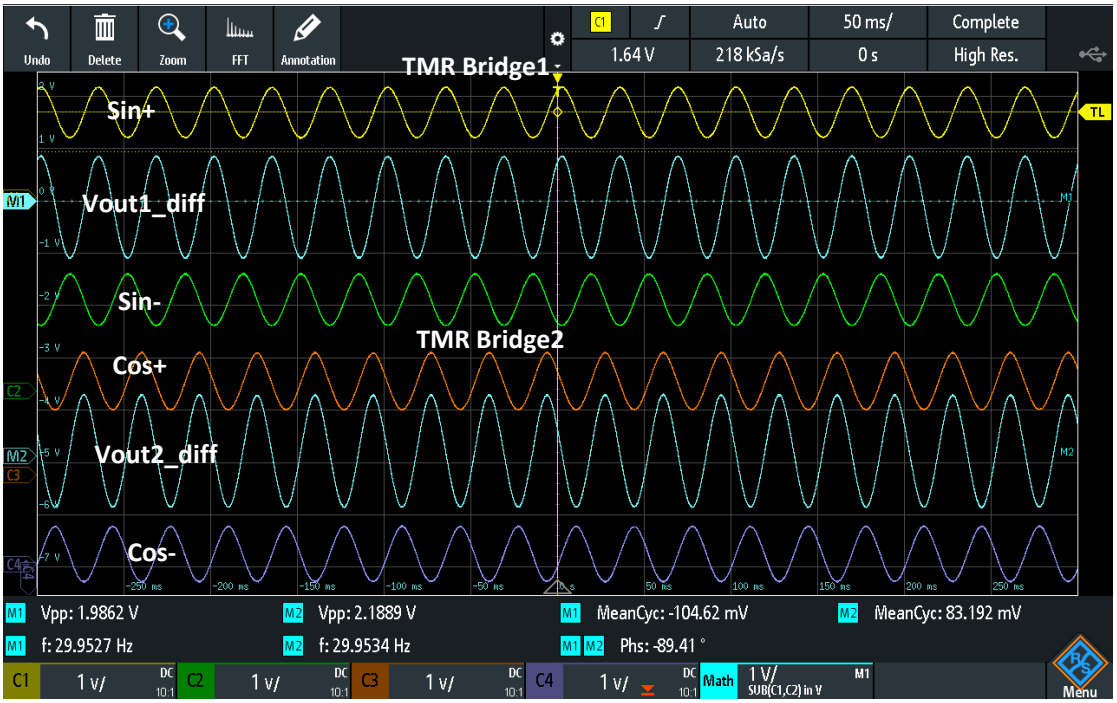

Figure 5.5: TMR sensor outputs at the in-amp gain of 4 and distance of 4 mm.

However, it is observed that the offset voltage, representing the combined effect of the sensor and the in-amp, is also amplified by a factor of 4, as indicated by the mean

cycle measurement. Given its unity gain amplifier configuration, it is assumed that the contribution of the offset voltage of the filter is negligible. The autozeroing scheme is evaluated to nullify the amplified offset voltage. The results, depicted in Figure 5.6, demonstrate a reduction in the offset voltage to below 10 mV.

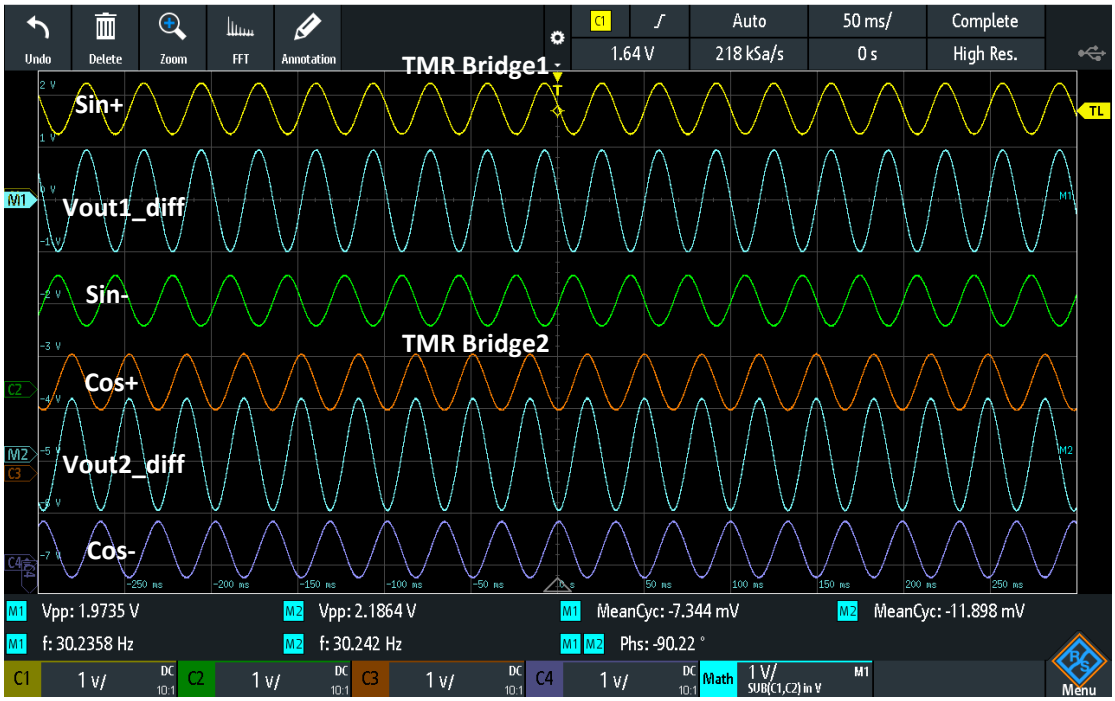

Figure 5.6: TMR sensor outputs at the in-amp gain of 4, distance of 4 mm and with offset voltage autozeroing.

To emphasize the impact of the offset voltage, the TMR sensor distance was increased to 11 mm, necessitating a gain adjustment to 32, as illustrated in Figure 5.7. This figure reveals that the offset voltage is approximately 250 mV in this configuration. After the application of the autozeroing scheme, the offset voltage is effectively reduced to approximately 16 mV, as evidenced in Figure 5.8.

It is worth noting that the offset voltage limits the reading resolution by consuming the full-scale voltage headroom of the ADC. More critically, it influences the accuracy of the angle computation as given by the equation [358]:

$$\theta = \arctan\left(\frac{2A_{sin}\sin(\alpha+\varphi) + \text{offset}_{sin}}{2A_{cos}\cos(\alpha) + \text{offset}_{cos}}\right) \tag{5.1}$$

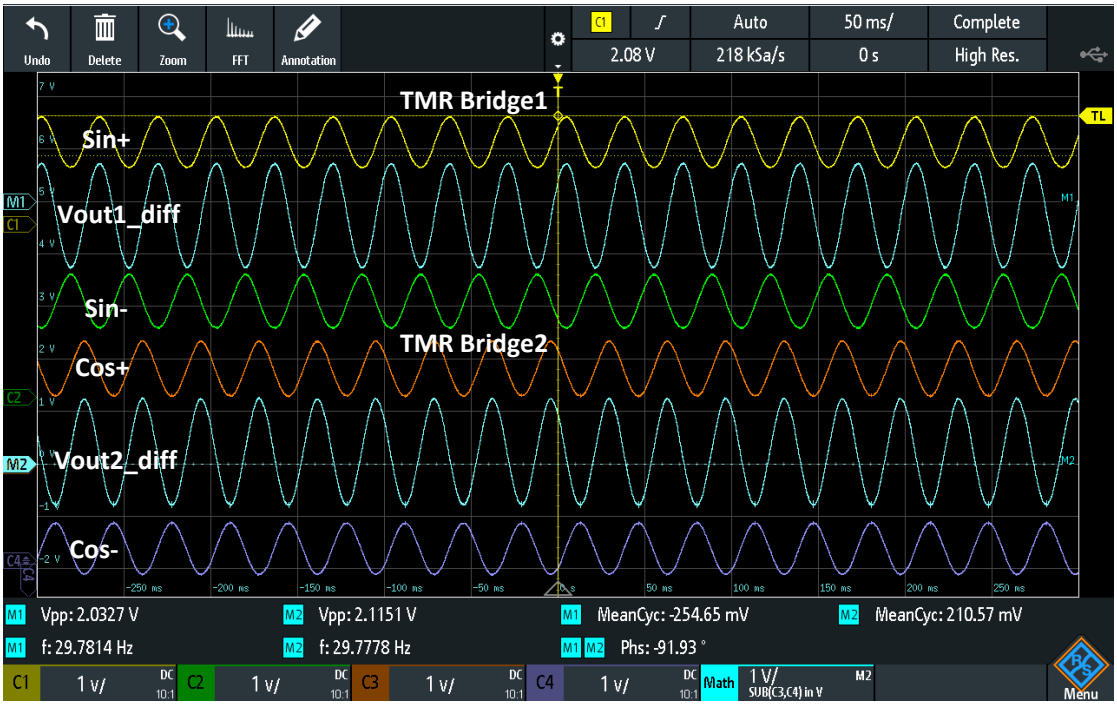

Figure 5.7: TMR sensor outputs at the in-amp gain of 32 and distance of 11 mm.

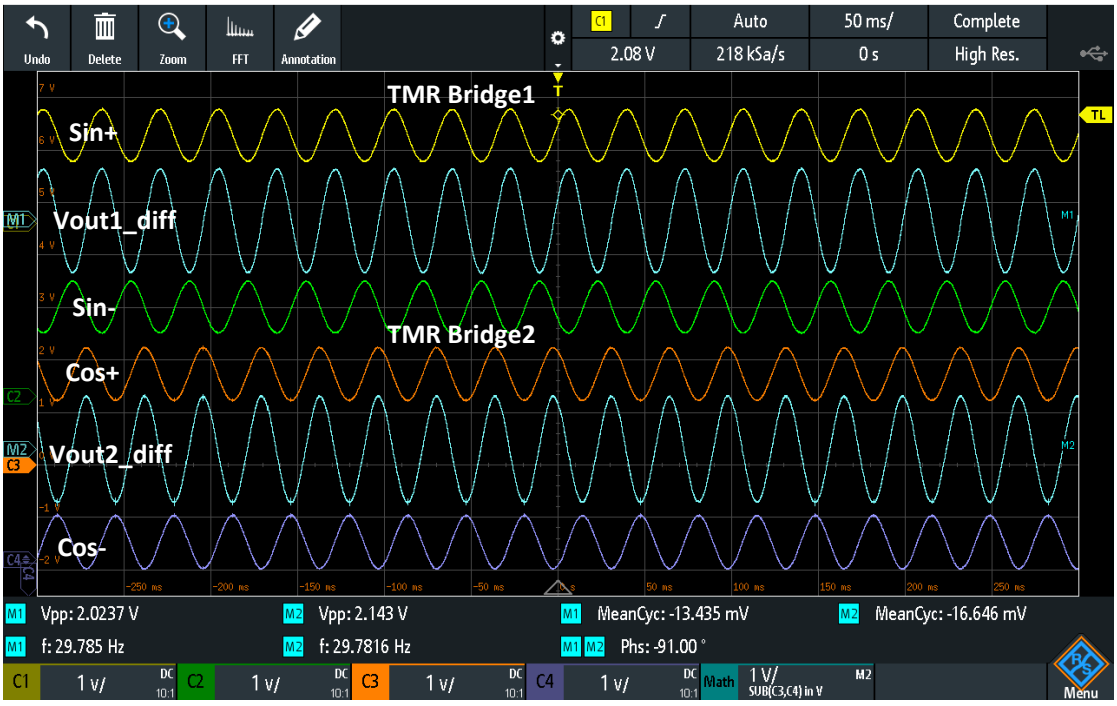

Figure 5.8: TMR sensor outputs at the in-amp gain of 32, distance of 11 mm and with offset voltage autozeroing.

Chapter 6

Conclusions and Future Work

This Ph.D. thesis contributes to the field of sensor electronics within Industry 4.0, focusing on the integration and application of smart sensory electronics (SSE) endowed with self-X properties (self-adaptive, self-optimization). By adopting an interdisciplinary approach that combines bio-inspired systems, evolvable hardware, and advanced signal processing techniques, this research introduces a suite of novel design methodologies and implementations for analog front-end (AFE) systems. It should be noted that the author was responsible for the design of the circuits and chip physical realization, whereas another Ph.D. candidate, working concurrently on the same project [112], was responsible for implementing the optimization algorithm at the software and hardware levels for both the extrinsic and intrinsic realization.

The work presented in this thesis contributes to the following areas:

1. **Improved CFIA Design with self-X properties**

   This research initially embarked on a low-cost and energy-efficient approach to intrinsically optimize the configurable current-feedback instrumentation amplifier (CFIA), aiming to simplify the otherwise complex performance evaluation setups needed for AFE systems enhanced with self-X properties during in-field optimization.

   This CFIA shows improved performance in terms of the input dynamic range and power efficiency, incorporating advanced features such as input-offset voltage autozeroing and fully-differential signal handling. The ERPSO algorithm's deployment at the hardware level was facilitated through Red Pitaya FPGA boards,

utilizing DACs and ADCs for data evaluation and acquisition from the CFIA circuit. The THD optimization has emerged as a key method for reducing the need for numerous evaluation units to fine-tune the performance of the CFIA or similar linear circuits, which is attributed to the statistical correlation between the amplifier performance metrics and THD values. Notably, circuit instability conditions were also correlated with the lower THD values. To ensure stability, a pulse test was conducted at the end of the optimization phase, with the bulk of the optimization employing a singular sinusoidal signal stimulus as an efficient method for amplifying the performance.

2. **Innovative Fully-Differential Filter Design with self-X Properties**

   Following the CFIA, another contribution is the development of a fourth-order fully-differential anti-aliasing and anti-imaging filter. The core amplifier topology of the filter is similar to that of the CFIA except for the bandwidth and current requirements, which resulted in different circuit sizes. The evaluated filter exhibits Butterworth characteristics. Across a temperature spectrum ranging from -20°C to 40°C, it has a tunable frequency span from 100 Hz to 10 MHz, with a resolution of 1024 points for each decade. This precision is facilitated by a 10-bit configurable linearized MOS resistor, which determines the pole frequency of the filter.

   The dynamic test of the filter proved the possibility of recovering the cutoff frequency and maintaining the maximum variance from the intended cutoff frequency within 3% of the error. Furthermore, the filter's broad input dynamic range, capable of processing up to a 2 Vp-p differential input signal, renders it suitable for direct connection to the subsequent ADC without the need for additional amplification. Notably, the filter incorporates a push-pull class AB driver circuit in its output stage, which provides substantial driving power to effectively manage the ADC input load on the filter outputs.

   The inclusion of non-intrusive sensors (NIS) for filter tuning, leveraging a neural network approach by creating a regression model of the filter, although constrained by time for practical measurements, has been validated through simulation results. The functionality of the non-intrusive sensor, confirmed through testing, marks a step towards realizing adaptive filter tuning in practical scenarios. The post-

layout simulation yielded a maximum error of approximately 9%. However, the error can be further minimized by taking more training points. The innovative concept introduced in this thesis is the indirect application of optimization to non-intrusive sensors (NIS), mirroring the tuning parameters of the primary filter circuit without halting its operation. Similar to the power-monitoring module, the NIS utilizes straightforward oscillators to produce a quasi-digital output signal with a fixed duty cycle and variable frequency. Consequently, a basic measurement setup is required to interpret sensor signals.

The temperature sensor is a part of the implemented NIS; however, it has additional functionality for monitoring the chip junction temperature for safe operation.

3. **Chip Area Optimization of the Reconfigurable Circuits**

   A major problem of reconfigurable circuits for supporting self-X SSEs is the cost increase owing to the required chip area due to the use of scalable elements and the associated memory for saving the configuration pattern. On the other hand, it reduces the chip-integrated functions for the specified areas. In this thesis, our approach is to configure only sensitive elements in the circuit that have been found to impact the design performance or tunability and to leave the other elements fixed to their optimum values achieved through the design phase and verification. Therefore, the optimization time required to find the optimum weight of the configurable elements is straightforwardly reduced, particularly by considering that the circuit topology is fixed, and the optimization algorithm does not need to start from scratch. At the same time, the design preserves flexibility and robustness to tackle PVT variation. Furthermore, the reduction in the switch resources required for configuring the analog circuits enhanced the dynamic performance.

4. **In-Field Optimization**

   The optimization of evolvable hardware (EHW) was established since the 1990's. However, what makes it still not an attractive solution for industrial applications is the need for the assessment unit to verify the optimization solution, which adds design complexity, time, and cost depending on the number and complexity of the test circuit. The optimization approach followed in this thesis relies on indirect measurements utilizing an integrated simple and cost-effective NIS with the help

of AI and neural network capabilities. Making the presented approach a valid solution for in-field optimization.

Initial testing of the CFIA with default configurations imported from the extrinsic optimization showed unsatisfactory performance and discrepancy from the post-layout simulation results. However, the CFIA performance is recovered following optimization, highlighting the effectiveness of the proposed method. Incorporating self-X properties into sensory electronics is crucial for their reliability and adaptability in diverse operational contexts, thus aligning this approach with the requirements of Industry 4.0. The lack of self-X capabilities may have necessitated discarding the batch, thus incurring significant manufacturing costs and poor yields.

5. **Improved Power efficiency**

   The introduction of a power-monitoring technique guided the ERPSO algorithm to identify the most power-efficient solution, significantly enhancing the energy efficiency and contributing to a prolonged device life-cycle and optimized efficiency. The CFIA, optimized for a 1 MHz signal frequency and a 1 Vp-p dynamic input range, attained an average optimized THD of -72 dB, showcasing a 34% increase in power efficiency over optimization processes without power monitoring. The rail-to-rail output dynamic was achieved using a push-pull output stage, demonstrating the success of the optimization.

   The intrinsic optimization is validated across varying temperatures from -20°C to 40°C and at reduced supply voltage down to 2.7 V. This revealed again in a 34% reduction in power dissipation and satisfactory THD levels across different temperatures where (THD) is $-71.93\,\mathrm{dB}$ at $T = 25\,^{\circ}\mathrm{C}$, $-69.95\,\mathrm{dB}$ at $T = -20\,^{\circ}\mathrm{C}$, and $-74.01\,\mathrm{dB}$ at $T = 40\,^{\circ}\mathrm{C}$, relative to signal stimuli with THD of $-74.49\,\mathrm{dB}$.

6. **Practical Application and Validation**

   The chip is developed and fabricated using Cadence design tools and XFAB's 0.35 μm CMOS NWELL technology and supported by the Europractice program. The chip covers a total area of $10.89\mathrm{mm}^2$ and includes 100 input/output pads consisting of 62,921 transistors housed with the CPGA100 package type. The sensor application involves a fully-differential Tunnel Magnetoresistance (TMR)

sensor, chosen for its high dynamic output range. In this application, the gain of the CFIA and the filter cutoff frequency is adjusted according to the motor speed and imported from the optimization run. The digital offset autozeroing found a useful application to null the offset voltage from the sensor level, thereby improving the angle measurement accuracy.

Future Work:

- moving toward small-node technology, such as CMOS 40 nm.
- on chip ADC
- on-chip BIST, which involves signal generation and synthesis of the optimization algorithm. A Direct digital synthesis (DDS) has been implemented [363] to generate a fully-differential sinusoidal signal ranging from 100 Hz to 3 MHz, however, this was not planned for this chip fabrication.
- Application in Electrical Impedance Spectroscopy.

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Appendix A

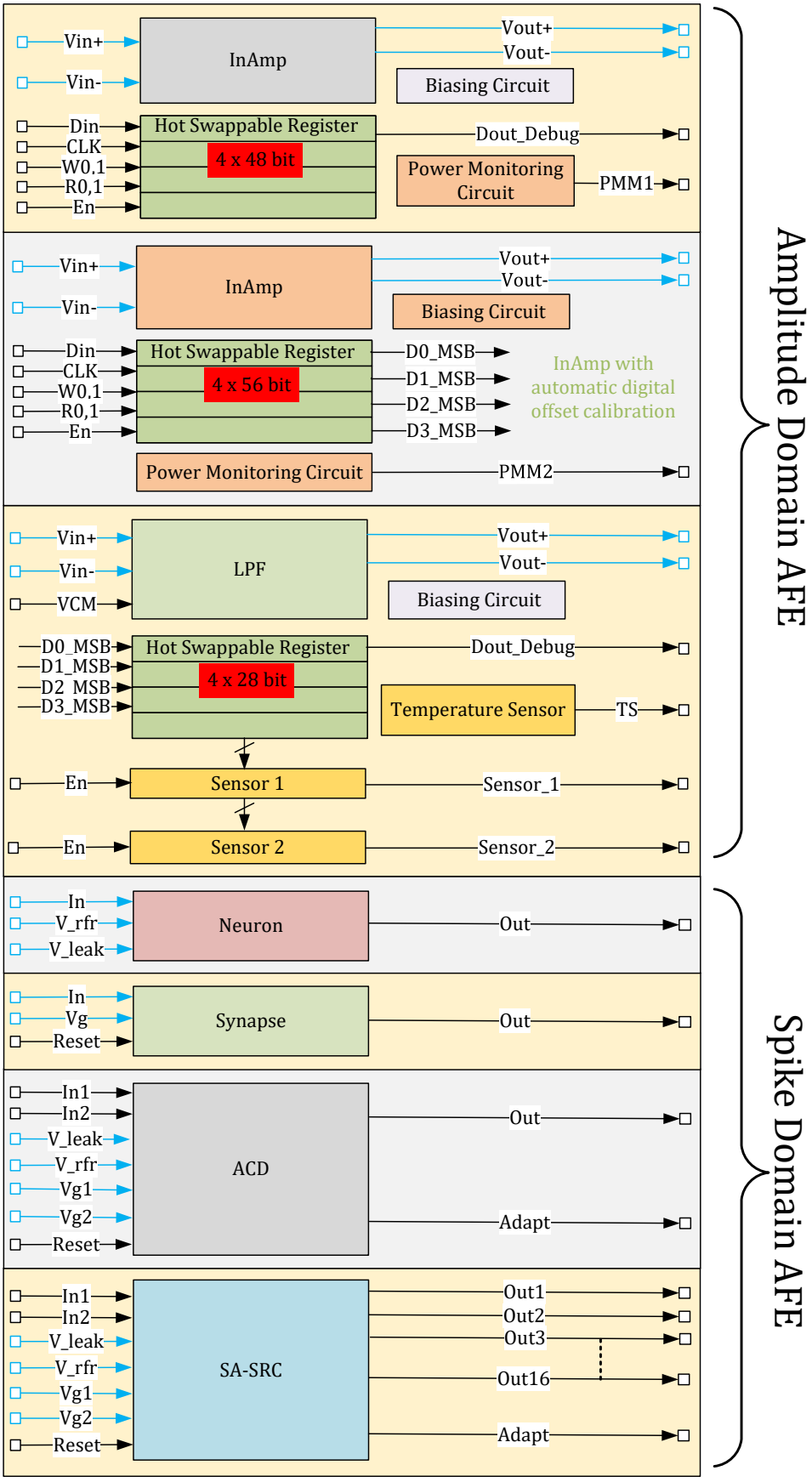

Figure A.1: Simplified chip functional diagram containing the designed CFIA and filter cells, in addition to the other Ph.D. work.

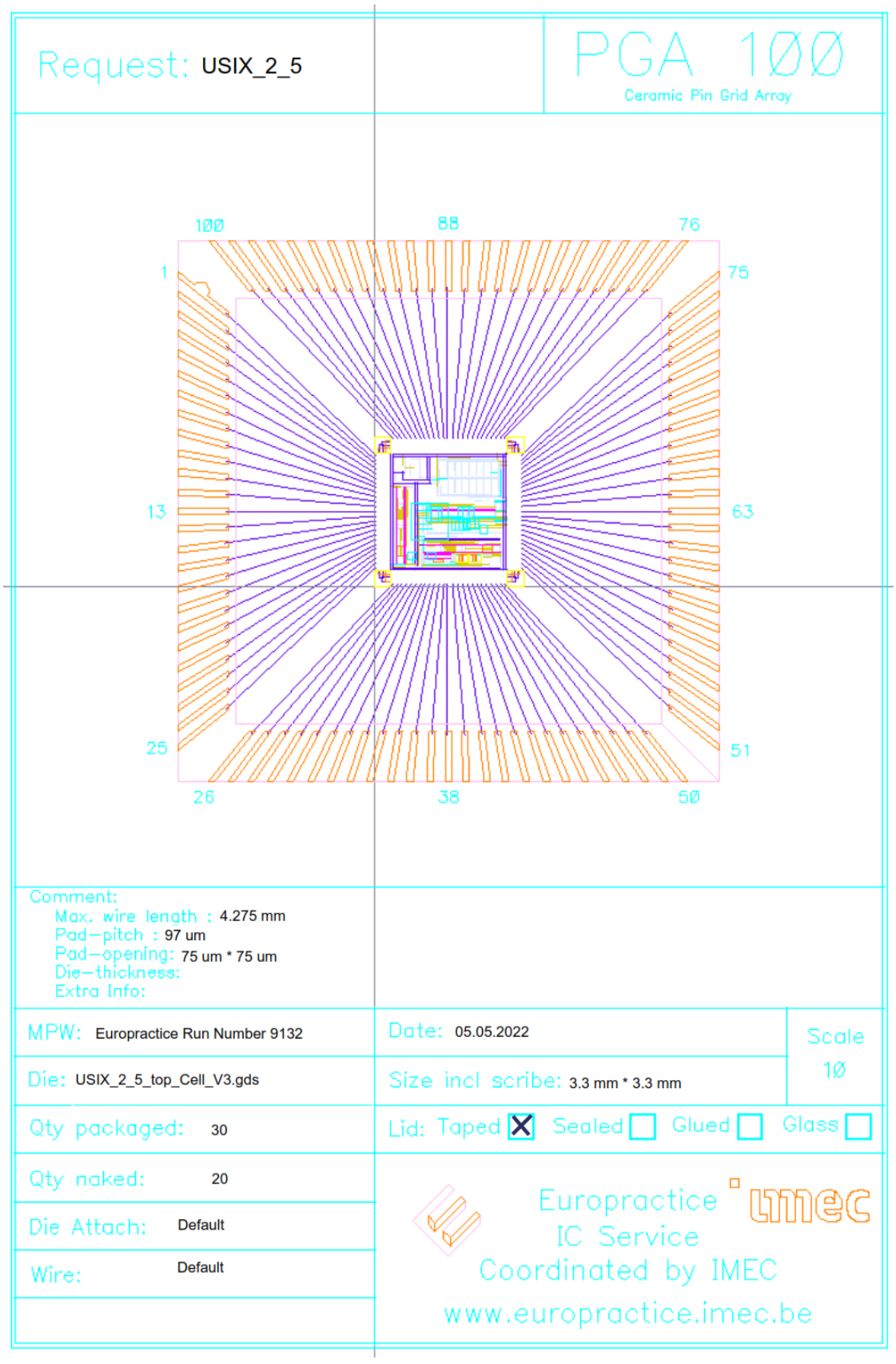

Figure A.2: The chip bonding diagram using CPGA100 package type fabricated via Europractice program.

Closed-loop gain (A_{CL})	**Temperature**	**Configuration Pattern (binary)**
1	24 °C	000100000000000110001111110101010000100001000011111111
	-20 °C	000100000000000111110110101001000010000100000100011100
	40 °C	000100000000000111010010110111000011001000000100011011 0
2	24 °C	001100000000000110001111110101010000100001000011111111
	-20 °C	001100000000000111110110101001000010000100000100011100
	40 °C	001100000000000110001111110101010000100001000011111111
4	24 °C	010100000000000110001111110101010000100001000011111111
	-20 °C	010100000000000111110110101001000010000100000100011100
	40 °C	010100000000000111010010110111000011001000000100011011 0
8	24 °C	011100000000000110001111110101010000100001000011111111
	-20 °C	011100000000000111110110101001000010000100000100011100
	40 °C	011100000000000111010010110111000011001000000100011011 0
16	24 °C	100100000000000110001111110101010000100001000011111111
	-20 °C	100100000000000111110110101001000010000100000100011100
	40 °C	100100000000000111010010110111000011001000000100011011 0
32	24 °C	101100000000000110001111110101010000100001000011111111
	-20 °C	101100000000000111110110101001000010000100000100011100
	40 °C	101100000000000111010010110111000011001000000100011011 0
64	24 °C	110100000000000110001111110101010000100001000011111111
	-20 °C	111100000000000111110110101001000010000100000100011100
	40 °C	110100000000000111010010110111000011001000000100011011 0
128	24 °C	111100000000000110001111110101010000100001000011111111
	-20 °C	111100000000000111110110101001000010000100000100011100
	40 °C	111100000000000111010010110111000011001000000100011011 0

Table A.1: CFIA best configuration patterns across different temperatures

Cutoff-frequency (f_c)	**Temperature**	**Configuration Pattern (binary)**
67 Hz	24 °C	01000100100000011110000000001
	-20 °C	01000100100000011110000000011
	40 °C	01000100100000011110000000001
1 kHz	24 °C	01000100000000111110000000001
	-20 °C	01000100000000111110000000011
	40 °C	01000100100000011110000001111
10 kHz	24 °C	01000100000000100010000000001
	-20 °C	01000100000000100010000000010
	40 °C	01000100000000100100000000010
100 kHz	24 °C	01000100000100111000000110001
	-20 °C	01000100000100111000001101000
	40 °C	01000100000100111000000100111
1 MHz	24 °C	01000100011000110000011100001
	-20 °C	01000100011000110000101100001
	40 °C	01000100011000110000011000000
5 MHz	24 °C	01000100011100000011111000100
	-20 °C	01000100011100000010001110000
	40 °C	01000100011100000010010011111
10 MHz	24 °C	01000100011111100011111111111
	-20 °C	01000100011111100011111111010
	40 °C	01000100011111100011111111111

Table A.2: Filter best configuration patterns across different temperatures

Appendix B

Curriculum Vitae

Senan Alraho

Education

- **Ph.D. in Electrical Engineering**, RPTU, Kaiserslautern, Germany (2018 – 2025)
- **M.Sc in Electrical Engineering**, Technische Universität Chemnitz / Germany (2010 – 2013)
- **B.Sc in Electronics Engineering**, Mosul University, Iraq (2002 – 2006)

Areas of Interest

- Analog Integrated Circuit Design
- Integrated Circuit Layout Engineering
- Electrical Measurement and Instrumentation
- Mixed-Signal Integrated Circuit Design
- Electronic Circuit Design
- Multi-Layer PCB Design