

Contributions to the Design and Application of Integrated Spiking Multi-Sensor Electronics with Self-X Properties for Future Robust Integrated Intelligent Systems

Beiträge zum Entwurf und zur Anwendung von integrierter Spiking-Multisensor-Elektronik mit Self-X-Eigenschaften für zukünftige robuste integrierte intelligente Systeme

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Abstract

The rapid evolution of micro and nano-scale technologies has propelled advancements in sensory systems, driving their adoption across IoT, Industry 4.0, autonomous vehicles, healthcare, and robotics. However, conventional amplitude-based sensory systems struggle with adaptability, energy efficiency, and reliable performance under fluctuating environmental and operational conditions. This thesis introduces a Neuromorphic Adaptive Spiking Analog-Front-End with Self-X Capabilities for Sensors (SAFEX), offering a novel and comprehensive design inspired by neuromorphic principles to overcome these limitations.

The proposed system combines two key components: the Adaptive Sensor Signal-to-Spike Converter (ASSC) and the Self-Adaptive Spike-to-Digital Converter (SA-SDC), working in tandem to deliver a highly flexible and efficient sensory interface. The ASSC transforms analog signals into spike timings, employing adjustable synaptic weights to ensure alignment of the sensor's input span with subsequent processing stages. This design eliminates the need for external level-shifting and amplification circuits, streamlining the signal-conditioning process. By leveraging the time domain for signal processing, the ASSC achieves a compact and adaptive implementation suitable for a variety of operating conditions. The transfer function of the ASSC was obtained using measurement processes for various gains. Adjustments in gain extended the duration of the ASSC, increasing the number of bits resolved by the SA-SDC to 11.98 bits. An offset of 77.6 LSB was observed in the transfer function due to specific synapse weights, which was rectified through synaptic weight adjustments.

Benchmarking against SoA sensory systems, the Neuromorphic Spiking Sensory System demonstrates superior adaptability and resource efficiency. Initial tests showed that the automatic adaptation mechanism reduced Differential Non-Linearity (DNL) from 0.6 to 0.34 LSB (a 43% improvement) and Integral Non-Linearity (INL) from 2.07 to 0.53 LSB (a 74% improvement) at nominal conditions. Under reduced power supply (from 3.3 V to 2.4 V), the system corrected eight missing codes, improving DNL from 1.53 to 0.4 LSB (a 74% reduction) and INL from 4.4 to 0.46 LSB (a 90% reduction). These performance enhancements surpass those reported in recent SoA designs, which often struggle to mitigate errors without extensive manual recalibration or complex error

correction algorithms. Furthermore, the system’s intrinsic self-adaptation at the hardware level directly contributes to yield improvement by automatically compensating for process variations, ensuring that each instance of the SAFEX system continuously self-optimizes without any supervision or external handling. This eliminates the need for manual recalibration and post-fabrication calibration, effectively lowering production costs.

Real-world validation using Tunnel Magnetoresistance (TMR) sensors for angle measurements further emphasized the system’s robustness. When the TMR sensor’s output decreased from 0.225 Vp-p to 0.104 Vp-p due to repositioning from 4 mm to 7 mm, the ASSC adapted by adjusting synapse weights, reducing the angle error from 24.95° to 12.72° a 49% improvement. This level of autonomous correction sets the system apart from traditional sensory interfaces, which lack adaptability and require manual recalibration.

In summary, this thesis introduces a transformative Neuromorphic Spiking Sensory System, bridging analog signal processing and time-domain techniques with self-X capabilities self-calibration, self-compensation, self-optimization, and self-repair. The design not only addresses the core technical and industrial challenges faced by existing sensory systems but also establishes a scalable, energy-efficient framework tailored to modern applications. This work takes a step towards dynamic adaptability, robust performance, and yield improvement through hardware-level self-adaptation, building on existing developments in neuromorphic engineering and sensory technology.

Future research will focus on extending system resolution, broadening application domains, and integrating higher-level self-X functionalities. With these advancements, the Neuromorphic Spiking Sensory System is well-positioned to meet the evolving demands of edge computing and intelligent, resource-constrained environments.

Kurzfassung

Die rasante Entwicklung von Technologien im Mikro- und Nanomaßstab hat den Fortschritt bei sensorischen Systemen vorangetrieben und deren Einsatz in den Bereichen IoT, Industrie 4.0, autonome Fahrzeuge, Gesundheitswesen und Robotik gefördert.

Herkömmliche amplitudenbasierte Sensorsysteme haben jedoch Probleme mit der Anpassungsfähigkeit, Energieeffizienz und zuverlässigen Leistung unter schwankenden Umwelt- und Betriebsbedingungen. In dieser Arbeit wird ein neuromorphes adaptives Spiking-Analog-Front-End mit Self-X-Fähigkeiten für Sensoren (SAFEX) vorgestellt, das ein neuartiges und umfassendes, von neuromorphen Prinzipien inspiriertes Design bietet, um diese Einschränkungen zu überwinden.

Das vorgeschlagene System kombiniert zwei Schlüsselkomponenten: den adaptiven Sensor-Signal-zu-Spike-Wandler (ASSC) und den selbstadaptiven Spike-zu-Digital- Wandler (SA-SDC), die im Tandem arbeiten, um eine hochflexible und effiziente sensorische Schnittstelle zu schaffen. Der ASSC wandelt analoge Signale in Spike-Timings um und nutzt einstellbare synaptische Gewichte, um die Eingangsspanne des Sensors mit den nachfolgenden Verarbeitungsstufen abzugleichen.

Dieses Design macht externe Pegelverschiebungs- und Verstärkungsschaltungen überflüssig und rationalisiert den Signalaufbereitungsprozess. Die Integration neuromorpher Konstruktionsprinzipien in sensorische Systeme trägt zu einem Paradigmenwechsel in der Signalverarbeitung bei. Durch die Kodierung von Informationen in der zeitlichen Abfolge von Spikes anstelle von absoluten Spannungswerten verbessert das SAFEX-System die Robustheit. Dieser Ansatz im Zeitbereich entspricht biologischen Prozessen und ahmt nach, wie neuronale Schaltkreise sensorische Eingaben effizient verarbeiten. Infolgedessen verbessert die vorgeschlagene Architektur nicht nur die Anpassungsfähigkeit, sondern ermöglicht auch den Betrieb in dynamischen Umgebungen, was sie zu einem vielversprechenden Kandidaten für Edge-Computing-Anwendungen macht. Durch die Nutzung des Zeitbereichs für die Signalverarbeitung erreicht der ASSC eine kompakte und anpassungsfähige Implementierung, die für eine Vielzahl von Betriebsbedingungen geeignet ist. Energieeffizienz und Flächenoptimierung sind entscheidende Vorteile des vorgeschlagenen Systems, insbesondere für Edge Devices, Wearables und autonome Systeme, bei denen die Energieressourcen begrenzt sind. Der adaptive Sensorsignal-

zu-Spike-Wandler (ASSC) verbessert die Systemeffizienz, indem er die synaptischen Gewichte anpasst und die Sensorspannen mit den Spannen des SA-SDC abgleicht. Diese Anpassung gewährleistet die volle Nutzung des Eingangsumwandlungsbereichs des SA-SDC und ermöglicht eine 4-Bit-Binärdatendarstellung anstelle von 3 Bits, wenn die Sensorspanne reduziert wird. Ohne den ASSC müsste die SA-SDC-Spanne erheblich größer sein, um alle möglichen Sensorspannen abzudecken, was sowohl die Fläche als auch den Stromverbrauch erhöht. Wenn die Sensorspanne die SA-SDC-Spanne überschreitet, käme es ohne die adaptiven Anpassungen des ASSC zu Informationsverlusten. Der ASSC reduziert also nicht nur die Rechenlast, sondern optimiert auch die Energie- und Flächeneffizienz, indem er die Sensor- und Verarbeitungsspannen ausgleicht.

Die Übertragungsfunktion des ASSC wurde mit Hilfe von Messverfahren für verschiedene Verstärkungen ermittelt. Anpassungen der Verstärkung verlängerten die Dauer des ASSC und erhöhten die Anzahl der vom SA-SDC aufgelösten Bits auf 11,98 Bits. In der Übertragungsfunktion wurde ein Offset von 77,6 LSB beobachtet, der auf spezifische Synapsengewichte zurückzuführen ist und durch Anpassungen der synaptischen Gewichte korrigiert wurde.

Beim Vergleich mit SoA-Sensorsystemen zeigt das neuromorphe Spiking-Sensorsystem eine überlegene Anpassungsfähigkeit und Ressourceneffizienz. Erste Tests zeigten, dass der automatische Anpassungsmechanismus die differentielle Nicht-Linearität (DNL) von 0,6 auf 0,34 LSB (eine Verbesserung um 43%) und die integrale Nicht-Linearität (INL) von 2,07 auf 0,53 LSB (eine Verbesserung um 74%) unter Nennbedingungen reduzierte. Bei reduzierter Stromversorgung (von 3,3 V auf 2,4 V) korrigierte das System acht fehlende Codes und verbesserte die DNL von 1,53 auf 0,4 LSB (eine Reduzierung um 74%) und die INL von 4,4 auf 0,46 LSB (eine Reduzierung um 90%). Diese Leistungsverbesserungen übertreffen die von neueren SoA-Designs, bei denen es oft schwierig ist, Fehler ohne umfangreiche manuelle Neukalibrierung oder komplexe Fehlerkorrekturalgorithmen zu minimieren. Darüber hinaus trägt die systemeigene Selbstanpassung auf Hardware-Ebene direkt zur Ertragsverbesserung bei, indem sie Prozessschwankungen automatisch kompensiert und sicherstellt, dass sich jede Instanz des SAFEX-Systems kontinuierlich selbst optimiert, ohne dass eine Überwachung oder externe Handhabung erforderlich ist. Dadurch entfällt die Notwendigkeit einer manuellen Nachkalibrierung und einer Kalibrierung nach der Fertigung, was die Produktionskosten effektiv senkt. Die Integration von

Self-X-Funktionen - Selbstkalibrierung, Selbstkompensation und Selbstoptimierung - verleiht der Zuverlässigkeit des Systems eine neue Dimension. Diese Funktionen ermöglichen eine kontinuierliche, automatische Korrektur von Prozess-, Spannungs- und Temperaturschwankungen (PVT), so dass eine manuelle Nachkalibrierung nicht mehr erforderlich ist. Diese integrierte Anpassungsfähigkeit erhöht die Ausbeute bei der Herstellung und sorgt für eine stabile Leistung über den gesamten Lebenszyklus des Produkts, wodurch sowohl die Produktions- als auch die Betriebskosten gesenkt werden. Dieser Automatisierungsgrad fügt sich nahtlos in die Anforderungen von Industrie 4.0 ein und unterstützt die Entwicklung intelligenter und belastbarer sensorischer Schnittstellen.

Die Validierung unter realen Bedingungen mit Tunnelmagnetowiderstandssensoren (TMR) für Winkelmessungen unterstrich die Robustheit des Systems. Die erfolgreiche Implementierung eines SAFEX - Prototypen in praktischen Sensoranwendungen unterstreicht sein Potenzial bei entsprechender Skalierung als vielversprechender Ansatz in der neuromorphen Technik. Als das Ausgangssignal des TMR-Sensors aufgrund einer Neupositionierung von 4 mm auf 7 mm von 0,225 Vp-p auf 0,104 Vp-p abfiel, passte sich das ASSC an, indem es die Synapsengewichte anpasste und so den Winkelfehler von $24,95^\circ$ auf $12,72^\circ$ reduzierte - eine Verbesserung von 49%. Dieses Maß an autonomer Korrektur unterscheidet das System von herkömmlichen sensorischen Schnittstellen, die nicht anpassungsfähig sind und eine manuelle Neukalibrierung erfordern.

Zusammenfassend lässt sich sagen, dass in dieser Arbeit ein transformatives neuromorphes Spiking-Sensor-System vorgestellt wird, das analoge Signalverarbeitung und Zeitbereichstechniken mit Self-X-Fähigkeiten, Selbstkalibrierung, Selbstkompensation, Selbstoptimierung und Selbstreparatur verbindet. Das Design geht nicht nur auf die zentralen technischen und industriellen Herausforderungen ein, mit denen bestehende sensorische Systeme konfrontiert sind, sondern schafft auch einen skalierbaren, energieeffizienten Rahmen, der auf moderne Anwendungen zugeschnitten ist. Die Arbeit geht einen Schritt in Richtung dynamischer Anpassungsfähigkeit, robuster Leistung und Ausbeutesteigerung durch Selbstanpassung auf Hardwareebene und setzt dabei auf bestehende Entwicklungen in der neuromorphen Technik und Sensorik auf.

Künftige Forschungsarbeiten werden sich auf die Erweiterung der Systemauflösung, die Ausweitung der Anwendungsbereiche und die Integration von Self-X-Funktionen auf höherer Ebene konzentrieren. Mit diesen Fortschritten ist das Neuromorphic Spiking

Sensory System gut positioniert, um die sich entwickelnden Anforderungen des Edge Computing und intelligenter, ressourcenbeschränkter Umgebungen zu erfüllen.

Erklärung

Hiermit versichere ich, dass ich die vorliegende Arbeit selbst angefertigt und verfasst habe und alle benutzen Hilfsmittel in der Arbeit angegeben habe.

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Unterschrift

Hamam Abd

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List of Figures

1.1	Electronic systems incorporate self-adaptive features alongside the integrated sensing element. [54].	6
2.1	The Proposed Architecture of the DDPM ADC. [161].	22
2.2	The Architecture of a Two-Step ADC [165].	24
2.3	Hopfield Neural Network-Based 4-Bit Analog-to-Digital Converter [188]. .	28
2.4	Synthesized Binary-Coded ADC [193].	30
2.5	Neural Model of an ADC [194].	32
2.6	Neural Network-Based ADC Correction Scheme [195].	33
2.7	The Proposed ADC Based on Artificial Spiking Neurons [197].	34
2.8	The Proposed Architecture of a Pipeline Memristive ADC [62].	37
2.9	Circuit Diagram of RPU and 4-bit mADC Sub-Block [62].	37
2.10	Block diagram of NeuADC [64].	38
2.11	ADC Finite State Machine (FSM) with Two States per Operational Stage [63].	40
2.12	Conventional and neuromorphic design	42
4.1	Sound localization and system overview	52
4.2	Optimized LIF neuron circuit	54
4.3	Schematic of adaptive synapse	56
4.4	Range corrections for sensor and SA-SDC	57
4.5	Schematic of the ASSC	58
4.6	Self-Adaptive Spike-to-Rank Coding	60
4.7	Achievable delay range versus the output counter for different V_g	61
4.8	ASRC operation modes	62

4.9	The control schematic of the adaptive coincidence detection (ACD) system utilizes a self-adaptive approach to modify synaptic weights and stores these values in up_counters.	63
4.10	Timing diagram of the adaptive synapse	64
4.11	Flowchart of adaptation layers	65
4.12	Adaptive coincidence detection system	66
4.13	State machine diagram for WTA	68
4.14	The rank code decoding algorithm is used to transform rank codes into binary formats.	69
5.1	MPC USIX chip: (a) After fabrication, the chip showcases bonding wires and a sealing ring, highlighting the integration of essential elements for operation and connection. (b) The layout features a pad frame, reflecting its well-structured design.	72
5.2	Experimental setup and system design	73
5.3	Hardware prototype block diagram	74
5.4	The flow diagram of the control module in the programmable logic utilizes the versatile GPIO pins of the Red Pitaya to directly interface with the chip's neuron, synapse cells, and SA-SRC. These GPIO pins are also linked to TMUX1102DBVR chips.	75
5.5	Red Pitaya board 2 executes the module architecture, integrating the Winner-Takes-All (WTA) mechanism and the algorithm simultaneously for seamless functionality.	76
6.1	The ASSC produces an output when 0.9 V is applied to V1, while V2 remains at 0 V.	78
6.2	Highlights the effectiveness of the ASSC in correcting offset deviations. The synaptic weights were modified to compensate for this error.	79
6.3	The ASSC system's response is evaluated using a measurement method designed for low-gain conditions.	79
6.4	The ASSC system's response is evaluated using a measurement method designed for high-gain conditions.	80

6.5	Adaptation process measurement outcomes for the SA-SRC cell on the chip.	80
6.6	Presenting an SA-SRC block-on-chip test setup using a supporting PCB and Red Pitaya.	81
6.7	On-chip measurement results of the SA-SRC, where in2 follows in1 with a 120 ns delay.	82
6.8	On-chip measurement results of the SA-SRC, where in1 follows in2 with a 15 ns delay.	82
6.9	SA-SRC measurements show that the on-chip signal in1 advances in2 by 15 ns. The order of output spikes shifts as the voltage decreases from 3.3 V to 3 V	83
6.10	SA-SRC transfer function: actual vs. ideal curves. Adaptation transitions from reset to the target synapse weight upon powering the chip. Post-adaptation measurements at $V_{dd} = 3.3$ V.	84
6.11	DNL and INL curves were recorded for the measured response in Figure 6.10 under ambient conditions at $V_{dd} = 3.3$ V.	84
6.12	SA-SRC transfer functions: ideal, pre-adaptation, and post-adaptation. Pre-adaptation measurements follow a V_{dd} shift from 3.3 V to 3 V, while post-adaptation measurements reflect the final state at $V_{dd} = 3$ V.	85
6.13	SA-SRC transfer functions: ideal, pre-adaptation, and post-adaptation. Pre-adaptation measurements follow a V_{dd} shift from 3.3 V to 2.4 V, while post-adaptation measurements reflect the final state at $V_{dd} = 3$ V.	85
6.14	The SA-SRC output was recorded with ASSC inputs V1 at 0 V and V2 at 0.2 V.	87
6.15	The SA-SRC output was recorded with ASSC inputs V1 at 0.55 V and V2 at 0 V.	87
6.16	The transfer function of the neuromorphic spiking sensory system with self-X features for actual and ideal cases.	89
6.17	The measured DNL and INL curves align with the curve shown in Figure 6.16	90

6.18	The neuromorphic spiking sensory system's response to a sinusoidal signal is analyzed, featuring a 0.8 Vp-p amplitude, 3 kHz frequency, and 0.4 V DC offset. V2 receives the input, while V1 remains at zero.	91
6.19	The image shows fully differential sinusoidal inputs applied to V1 and V2, with a 0.8 Vp-p amplitude, 1 kHz frequency, and 0.4 V DC offset.	92
6.20	The neuromorphic spiking sensory system's response to fully differential sinusoidal inputs at V1 and V2 was analyzed, featuring a 0.8 Vp-p amplitude, 1 kHz frequency, and 0.4 V DC offset.	93
6.21	The FFT output reveals the neuromorphic spiking sensory system's response to fully differential sinusoidal inputs at V1 and V2, as shown in Figure 6.19	94
6.22	System configuration showcasing the TMR interface integration with the proposed neuromorphic spiking sensory system.	94
6.23	Block Diagram illustrating the TMR interface integration with the proposed neuromorphic spiking sensory system.	95
6.24	Experimental setup for TMR interface	96
6.25	The TMR sensor outputs were captured from a 4 mm distance.	97
6.26	The neuromorphic spiking sensory system's functionality was tested by applying the TMR sensor's differential outputs to V1 and V2, with recordings taken at a 4 mm sensor distance.	98
6.27	Angle calculation with TMR sensor	99
6.28	The TMR sensor outputs were captured from a 7 mm distance.	100
6.29	Angle calculation with TMR sensor at 7 mm	101
6.30	Angle calculation with adjusted TMR sensor setup	102
7.1	The Neuromorphic Spiking Sensory System, or SAFEX, incorporates a proposed second level of adaptivity, combined with an optimization unit working alongside the 5-bit Neural DAC.	110
A.1	Simplified chip block diagram featuring the custom Amplitude Domain AFE and Spike Domain AFE.	A-1
A.2	Chip bonding layout with a CPGA100 package, manufactured through the Europractice program.	A-2

A.3	The chip index layout of a CPGA100 package.	A-3
A.4	The pin list of the neuron cell and its description.. . . .	A-3
A.5	The pin list of the synapse cell and its description.. . . .	A-4
A.6	The pin list of the ACD cell and its description.. . . .	A-4
A.7	The pin list of the SA-SRC cell and its description.	A-5
A.8	Block diagram of the ASSC	A-6
B.1	Block diagram of the ASSC	B-2
B.2	Block diagram of the ASSC	B-4
B.3	Block diagram of the ASSC	B-6
B.4	Block diagram of the ASSC	B-7
B.5	Block diagram of the ASSC	B-7
B.6	Block diagram of the ASSC	B-11
B.7	Block diagram of the ASSC	B-14
B.8	Block diagram of the ASSC	B-15
B.9	Block diagram of the ASSC	B-16
B.10	Block diagram of the ASSC	B-17
B.11	Block diagram of the ASSC	B-18

List of Tables

2.1	Comparisons of state-of-the-art ADC designs (Part 1).	42
2.2	Comparisons of state-of-the-art ADC designs (Part 2).	43
2.3	Comparisons of state-of-the-art ADC designs (Part 3).	43
3.1	Comparison of state-of-the-art memristor circuits.. . . .	49
B.1	Interaural time difference (ITD) and coincidence detector (CD) response in Jeffress Model	B-3
B.2	Showing the output spike order corresponding to Figure B.5, where in2 precedes in1. The Table indicates the sequence of firing outputs to identify which output occurred first, second, and so on.	B-8
B.3	Output spike order corresponding to the design presented in the thesis, where in2 precedes in1. The numbers in the Table indicate the spike order relative to the other outputs.	B-9
B.4	Output spike order corresponding to the design presented in the thesis, where in2 precedes in1. The numbers in the Table indicate the spike order relative to the other outputs.	B-9
B.5	Output spike order corresponding to the design presented in the thesis, where in1 precedes in2. The numbers in the Table indicate the spike order relative to the other outputs.	B-10
B.6	Output spike order corresponding to the design presented in the thesis, where in1 precedes in2. The numbers in the Table indicate the spike order relative to the other outputs.	B-10
B.7	Comparison of Area, Power, and Stage Resource Requirements for 4-Bit Resolution	B-13

Contents

Abstract	ii
Kurzfassung	iv
Erklärung	viii
Acknowledgements	ix
List of Figures	xiv
List of Tables	xv
List of Abbreviations	xx
1 Introduction	1
1.1 Advanced Sensory Integration and AI Technology in Industry 4.0	1
1.2 Challenges in Sensor Signal Interface Systems for Advanced CMOS Nodes	2
1.3 Self-X Sensor Signal Interface Systems	5
1.4 Neuromorphic Sensor Signal Interface Systems	7
1.5 The Goals of the Thesis	9
1.5.1 Development of a Robust and Technology-Agnostic Signal Inter- face System	9
1.5.2 Adaptation of Natural Neural Coding Principles	10
1.5.3 Methodology	10
1.6 Thesis Structure	10
1.6.1 Chapter 1: Introduction	11
1.6.2 Chapter 2: State of the Art	11
1.6.3 Chapter 3: Biological Foundations of Neuromorphic Spiking System	11
1.6.4 Chapter 4: Neuromorphic Spiking Sensory System	11
1.6.5 Chapter 5: Integration of Neuromorphic System Components . . .	12
1.6.6 Chapter 6: Neuromorphic Chip Characterization and Application .	12

1.6.7	Chapter 7: Conclusions	12
2	State of the Art	13
2.1	Techniques for Tackling Sensor Signal Interface Challenges	14
2.1.1	Layout Matching for Process Variations	14
2.1.2	Design Automation for Circuit Optimization	14
2.1.3	Trimming Techniques for Post-Production Adjustments	14
2.1.4	Dynamic Calibration and Compensation	15
2.1.5	Evolvable Hardware and Self- capabilities	15
2.1.6	On-Chip Measurement and Built-In Self-Test (BIST)	15
2.2	Evolvable Hardware for Addressing Sensor Interface Challenges	15
2.2.1	Introduction to Evolvable Hardware (EHW)	15
2.2.2	Analog Evolvable Hardware	16
2.2.3	Advancements in Field Programmable Transistor Arrays (FPTAs)	16
2.2.4	Applications of Evolvable Hardware in Space and Autonomous Systems	17
2.2.5	Challenges and Limitations of EHW	17
2.2.6	Hybrid Granularity Approaches	17
2.2.7	Evolutionary Algorithms and Optimization Techniques	18
2.2.8	Built-in Self-Test (BIST) for In-Field Optimization	18
2.2.9	Universal Sensor Interface Systems	18
2.2.10	Future Directions, Open Challenges, and Conclusion	19
2.3	Conventional Design for Scaling Challenges	19
2.3.1	Flash ADC Techniques	20
2.3.2	Stochastic ADCs	21
2.3.3	Synthesizable ADC Architectures	22
2.3.4	Delta-Sigma and Hybrid ADC Architectures	23
2.4	Neuromorphic Design for Scaling Challenges	27
2.4.1	Hopfield Network-Based ADCs	27
2.4.2	Neural Network-Based ADCs	30
2.4.3	Spiking Neuron ADCs	33
2.4.4	Memristive Neural ADCs	36

2.5	Summary	40
3	Biological Foundations of Neuromorphic Spiking System	44
3.1	Insights Drawn from Biological Sensory Systems	44
3.2	Biological Neuron Model	45
3.3	Synapse	46
3.4	Sensor-to-Spike Concepts	48
4	Neuromorphic Spiking Sensory System	51
4.1	Neuron model	53
4.2	Synapse	55
4.3	Adaptive Sensor Signal-to-Spike Converter (ASSC)	56
4.4	Self-Adaptive Spike-to-Digital Converter (SA-SDC)	59
5	Integration of Neuromorphic System Components	71
5.1	Chip Design and Demonstration Board	71
5.2	Implementation and Architecture	75
6	Neuromorphic Chip Characterization and Application	77
6.1	Characteristics of ASSC on Chip	77
6.2	Characteristics of SA-SDC on Chip	78
6.3	Characteristics of a Neuromorphic Sensory System on Chip	86
6.4	Neuromorphic System in Real-World Application	92
7	Conclusions	103
7.1	Development of a Robust and Technology-Agnostic Signal Interface System	103
7.2	Adaptation of Natural Neural Coding Principles	104
7.3	Implementation of Self-X Capabilities	106
7.4	Enhancement of Power Efficiency	108
7.5	Future Work	109
	Bibliography	126
A		A-1

B	B-1
B.1 Architectures for Sound Localization	B-3
B.1.1 Jeffress model	B-4
B.1.2 Jeffress-One-Side Modell	B-4
B.1.3 Kammara's model	B-5
B.1.4 Hybrid Model	B-5
B.1.5 Thesis Model	B-7
B.2 Quantitative Comparison of the Jeffress, Hybrid, and Thesis Models . . .	B-8
B.2.1 Hardware Requirements for 4-bit Resolution	B-9
B.2.2 Comparative Advantages and Efficiency of the Thesis Model . . .	B-11
B.2.3 Resource Composition per Processing Stage	B-12
B.2.4 Summary and Practical Implications	B-12
B.3 Scalability of the ACD Chain for Extended Temporal Resolution in SA- SRC Architecture	B-13
B.3.1 Extension of the Design to a 6-bit	B-13
C Curriculum Vitae	B-1

List of Abbreviations

ACD Adaptive Coincidence Detector

ADC Analog-to-Digital Converter

AFE Analog Front End

AI Artificial Intelligence

ANN Artificial Neural Network

ASRC Adaptive Sensor Response Circuit

ASSC Adaptive Sensor Signal-to-Spike Converter

BIST Built-In Self-Test

CAB Configurable Analog Block

CBTA Current Backward Transconductance Amplifier

CCII Second-Generation Current Conveyor

CFIA Configurable Feedback Instrumentation Amplifier

CMOS Complementary Metal Oxide Semiconductor

CPGA100 Ceramic Pin Grid Array with 100 pins

CT-IDSM Continuous-Time Incremental Delta-Sigma Modulator

DAC Digital-to-Analog Converter

DDPM Dyadic Digital Pulse Modulation

DEM Dynamic Element Matching

DSP Digital Signal Processing

EHW Evolvable Hardware

ENOB Effective Number of Bits

EP Evolutionary Processor

FIR Finite Impulse Response

FPA Field Programmable Analog Array

FPGA Field Programmable Gate Array

FPMA Field Programmable Medium-Granular Mixed-Signal Array

FPTA Field Programmable Transistor Array

FS Full-Scale

FSTD Full-Scale Time Difference

FSM Finite State Machine

GA Genetic Algorithm

GP Genetic Programming

H-H Model Hodgkin-Huxley Model

I/O Input/Output

IC Integrated Circuit

IIoT Industrial Internet of Things

IIR Infinite Impulse Response

IoT Internet of Things

IR Drop Voltage Drop due to Internal Resistance

IRDS International Roadmap for Devices and Systems

ITD Interaural Time Difference

ITRS International Technology Roadmap for Semiconductors

JK Flip-Flop Jack Kilby Flip-Flop

LIF Leaky Integrate-and-Fire

LSB Least Significant Bit

M Transistor (e.g., M1, M2, etc.)

ML Machine Learning

MLP Multilayer Perceptron

MNoB Maximum Number of Bits

MNoL Maximum Number of Levels

MPC Multi-Project-Chip

MSB Most Significant Bit

NEF Neural Engineering Framework

NN Neural Network

NOB Number of Bits

NUS Nonuniform Sampling

OSR Oversampling Ratio

PCB Printed Circuit Board

PLA Programmable Logic Array

PL Programmable Logic

PVT Process-Voltage-Temperature

RNG Random Number Generator

RPU Random Perturbation Unit

RRAM Resistive Random-Access Memory

SA-SDC Self-Adaptive Spike-to-Digital Converter

SA-SRC Self-Adaptive Spike-to-Rank Coding

SAR Successive Approximation Register

SNN Spiking Neural Network

SQNR Signal-to-Quantization Noise Ratio

SSDC Sensor-to-Spike-to-Digital Converter

STF Signal Transfer Function

STP Short-Term Plasticity

TDS Time Difference Span

TMUX1102DBVR Texas Instruments Precision CMOS Switch

TMR Triple Modular Redundancy

USI Universal Sensor Interface

USIX Universal Sensor Interface with Self-X Features

VCO Voltage-Controlled Oscillator

VRFR Variable Refractory Firing Rate

VTC Voltage Transfer Curve

WA Winner Algorithm

WTA Winner-Take-All

XFAB Foundry for Analog/Mixed-Signal ICs and MEMS

ZIC Zoom-Incremental-Counting

Chapter 1

Introduction

1.1 Advanced Sensory Integration and AI Technology in Industry 4.0

Over the past decade, the realm of micro and nano technologies has witnessed a remarkable proliferation, instigating a substantial upswing in the advancement of sensory technologies. This burgeoning domain finds its foundation in the continuous and expeditious progress made in the sphere of micro and nano-scale integration and packaging technologies, which encompass systems-on-chip (SoC) and system-in-package (SiP) [1–3]. This growth is further bolstered by the advent of novel sensory concepts. Simultaneously, the field of sensor technology and sensory systems is undergoing rapid expansion and diversification, with a broad spectrum of practical applications [4, 5]. As novel sensory concepts and physical transduction elements continue to evolve, coupled with significant strides in integration technology, both newly developed and pre-existing components are steadily diminishing in size [6]. This dynamic evolution underscores the ever-advancing landscape and the profound impact of miniaturization in sensor technology. Together with sophisticated information processing technology, often referred to as Artificial Intelligence (AI), this has facilitated the creation of intelligent systems suited for diverse applications, encompassing the Internet of Things (IoT) as well as the Industrial Internet of Things (IIoT) [7].

Industry 4.0, a widely recognized term for this transformative shift, marks the onset of a new era in industrial progress [7–10]. Central to the essence of Industry 4.0 lies the seamless correlation between the collection, meticulous analysis, and insightful interpre-

tation of data, a process driven by the proliferation of IIoT devices. These devices are increasingly permeating various sectors, including manufacturing, transportation, and logistics.

This pivotal transformation stems from the intricate interplay of machine learning (ML) and AI with a constellation of cutting-edge technologies, among them cloud computing, big data analytics, and IIoTs [9, 11–14]. It serves as the driving force behind the fourth industrial revolution, Industry 4.0 [9, 11–13], fostering a myriad of current applications spanning wearable electronics, automation [15], autonomous driving [16], healthcare assistance systems [17], and various other sectors.

The achievement of Industry 4.0 is inextricably linked to the imperative advancement of precise, dependable, and advanced sensory electronics and reliable sensors [14, 18]. These indispensable components assume the pivotal role of acquiring, processing and transmitting data, constituting the linchpin for further procedural operations. They are instrumental in capturing a spectrum of chemical, physical, biological, and environmental information, thereby facilitating informed choices and the optimization of processes. As technology undergoes continual evolution, particularly within the environment of industrial transformation, its progress is fundamentally underpinned by the acquisition, analysis, and interpretation of data sourced from smart sensors and IIoT devices [19–21]. Consequently, the creation of accurate, versatile, robust, and flexible sensory electronics becomes paramount, ensuring the efficient collection, processing, and transmission of data to the central processing unit [22, 23].

1.2 Challenges in Sensor Signal Interface Systems for Advanced CMOS Nodes

The ongoing evolution of CMOS node technology, in harmony with the 'More Moore' expansion, as articulated in both the 2015 International Technology Roadmap for Semiconductors (ITRS) [2] and the intervening 2021 Edition of the International Roadmap for Devices and Systems (IRDS) [24], plays a pivotal role in bolstering the performance metrics of digital systems. Conversely, mixed-signal and analog circuits, especially those engaged in sensor signal interfacing [18], frequently encounter delays in the adoption of the most recent node, primarily attributable to an array of intricate technical obsta-

cles [25–30]. Numerous scholarly investigations have underscored the nuances of these challenges [25–30]. In [27, 28, 31, 32], it becomes evident that circuit design is confronted with a multitude of intricate challenges. These challenges encompass a spectrum of complexities, ranging from the dwindling intrinsic device gain, exacerbated noise levels, increased device mismatch, diminished supply voltage, reduced signal swing, and manufacturing deviations. Collectively, these hurdles illuminate the dynamic and demanding landscape that confronts contemporary analog design practitioners.

The scalability of analog circuits stands in stark contrast to that of their digital counterparts, as the dimensions of their components are intrinsically tied to specific circuit parameters, including but not limited to noise, amplification, and bandwidth. Moreover, the pursuit of satisfactory device matching necessitates the utilization of larger devices, a strategic choice aimed at mitigating the impact of both systematic and random process errors—an undertaking that grows increasingly challenging in the wake of smaller node technologies [33]. Consequently, the spatial requirements for analog circuits do not undergo automatic reduction in proportion to the diminishing structural dimensions, adding another layer of complexity to the intricate art of analog design. As the supply voltage decreases and the threshold voltage fails to follow a comparable reduction route, conventional analog circuit topologies encounter practical challenges. This disparity between voltage parameters further leads to a reduction in the overall signal dynamic range of the Analog Front End (AFE), which contrasts with the prevailing trends in sensor technology especially where dynamic ranges typically exhibit an upward route. Implementing techniques to counteract the short-channel effect, such as employing cascoded mirrors to enhance circuit matching or augmenting intrinsic gain, may prove unattainable due to the constraints imposed by limited voltage headroom.

The functionality of sensor interface electronics is significantly influenced by both static and dynamic variations, which include the irreversible dynamic effects stemming from aging, as documented in previous studies [34, 35]. These variations play a critical role in shaping the operational capabilities of sensor interface circuits, underscoring the importance of comprehensive analysis and mitigation strategies within the realm of electronic design and engineering.

Amidst the rapidly evolving landscape of semiconductor technology, it is essential to acknowledge that static discrepancies, especially within highly miniaturized and intri-

cately designed next-generation complementary metal oxide semiconductors (CMOS), stem from both local random/stochastic as well as global systematic variations across chip components [25, 36]. These variations can be directly ascribed to manufacturing process imperfections, encompassing constraints in lithography resolution which result in deviations in device dimensions, variations in gate oxide thickness profiles influencing transistor threshold voltages, and differences in electron and hole mobility that consequently affect MOS I-V features [37]. Amidst these challenges, it's essential to note that the imposition of mechanical stress on the chip throughout the delicate die molding process, caused by the meticulous packaging and assembly techniques employed in the fabrication of integrated circuits (ICs), exacerbates these static disparities [38]. These manufacturing-induced variations underscore the intricacies and challenges faced by modern semiconductor design and fabrication, emphasizing the need for meticulous attention to detail and comprehensive analysis to mitigate the impact of these discrepancies on-chip performance.

Dynamic fluctuations, particularly the reversible kind, are the consequence of environmental changes, shifts in voltage supply, and the influence of thermal drift induced by self-heating and temperature differences that result from non-uniform power consumption characteristics within integrated circuits (ICs) [39, 40]. This effect is more pronounced in densely packed transistors within advanced node technology and SoC designs [41, 42].

To address these reversible dynamic variations and the accompanying static process fluctuations, semiconductor process design kits (PDK) serve as effective modeling tools. They enable the evaluation of these variations via circuit simulations, employing electronic design automation (EDA) software, over a spectrum of process corners and changes in voltage and temperature, also known as Process-Voltage-Temperature (PVT) variation. Nevertheless, the complex task of accurately modeling and predicting the aging impact on circuit functionality and long-term dependability persists as a challenge [43, 44]. This challenge holds paramount significance when evaluating and deploying reliable and sturdy circuits designed for essential practical applications during the entire lifespan of the integrated circuit (IC) [45].

1.3 Self-X Sensor Signal Interface Systems

In the realm of system design, factors beyond the initial design goals take center stage, emphasizing the critical facets of long-term system reliability, precision, dependability, and the assurance of consistent performance. However, a distinct challenge arises when venturing into harsh industrial environments, where the implementation of sensor systems encounters significant impediments. In these settings, extreme ambient conditions, such as elevated functioning temperatures and chemically harsh surroundings, cast a shadow over the reliable performance of delicate electronic devices. As a result, conventional electronics and established manufacturing processes, along with their packaging solutions, prove inadequate and impractical for deployment [46–48].

Moreover, the rise of Industry 4.0 has redefined the requisites for adaptable systems, demanding the capacity to swiftly adapt to evolving needs in a manufacturing landscape characterized by its dynamism. Consequently, in this dynamic landscape, electronic systems can no longer rely on rigid, fixed designs tailored to mass-produced products and predictable demand. The shift necessitates the adoption of flexible systems that enable efficient reconfiguration with minimal disruption to operations and capital expenditure [49]. This transformative evolution underscores the intricate intersection of reliability, adaptability, and technological prowess in contemporary industrial applications.

Significant research efforts have been dedicated to finding an optimal balance among circuit characteristics, recognizing that the pursuit of excessively wide performance margins may not be practically and economically feasible in all cases. In response to the challenges posed by extreme environmental conditions across various domains, including space exploration [50], the notion of evolvable hardware (EHW) has emerged as a resilient strategy. EHW pertains to adaptable electronic systems capable of autonomous self-configuration through the utilization of machine learning (ML) and AI-inspired techniques [51, 52]. A critical component within this framework, the evolutionary processor (EP) [53], facilitates the autonomous adaptation of EHW, granting it self-X properties encompassing self-calibration, self-monitoring, self-repair, self-trimming, self-optimization, and self-configuration [54–56]. Furthermore, the sensor and technology developments roadmaps published by the Association for Sensors and Measurement (AMA) as well as the User association of automation technology in process industries

(NAMUR) [18, 57]. They have underlined the significance of incorporating sensor electronics infused with self-X capabilities. This approach holds promise in addressing the complex challenges posed by demanding and unpredictable environmental conditions.

The incorporation of this integration is fundamental to ensure robustness, reliability, and adaptability over a wide spectrum of applications, especially in challenging scenarios like Industry 4.0 and other environments known for their extreme conditions [53, 58]. It serves as a pivotal element in improving management and synchronization across the complete supply network, guaranteeing the seamless operation and longevity of electronic systems [53, 58]. This integration allows the system to respond effectively to both static and dynamic anomalies, encompassing reversible and aging issues, that may arise during the service life of the electronics, further underscoring its indispensable role in modern technological landscapes.

This method can be implemented by utilizing the adjustable components within the circuit and the performance evaluation setup [54, 59]. These adaptable elements serve as tuning mechanisms for design, allowing for periodic calibration to maintain and control circuit performance. As a result, this approach enables the design to evolve and adapt over the entire system life cycle.

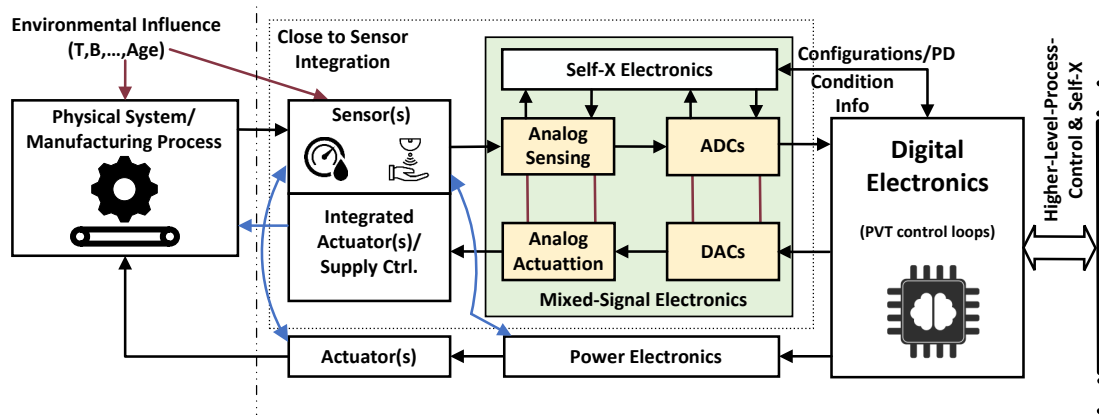


Figure 1.1: Electronic systems incorporate self-adaptive features alongside the integrated sensing element. [54].

The incorporation of Self-X Capabilities can span multiple hierarchical levels in sensor systems, extending from the individual sensor components as demonstrated by authors in [60, 61]. As illustrated in Figure 1.1, the power electronics connected to the actuator/DAC chain are conventionally employed for control functions [54]. This entails integrating the sensor into the optimization loop to rectify and fine-tune its performance.

These advanced capabilities are rooted in adaptive and optimization techniques applied across various levels of abstraction. One notable instance from the industrial landscape is Synopsys, a prominent company that, subsequent to its acquisition of Moortec, has demonstrated how these methods can be effectively applied in practical applications.

1.4 Neuromorphic Sensor Signal Interface Systems

Neuromorphic sensor signal interface systems represent a cutting-edge approach to signal processing and adaptation, drawing inspiration from the remarkable capabilities observed in natural beings. These systems aim to replicate the robustness and adaptivity seen in living organisms, allowing them to thrive in noisy, hostile, and ever-changing environments. Engineers have long been captivated by the ability of natural organisms to function effectively on both an individual and population level and neuromorphic sensor signal interface systems seek to harness these coveted properties to enhance technology and its performance. Through the integration of bio-inspired design and advanced sensory interfaces, these systems hold the potential to revolutionize various fields, from robotics to healthcare, by enabling devices to operate more intelligently and autonomously.

Leading-edge designs are committed to tackling the challenges, with a multitude of configurations having been proposed in scholarly literature. An exemplar in this field, the study presented in reference [62], introduced an innovative architecture known as the pipelined Hopfield neural network memristive ADC. The primary objective of this approach was to harness the inherent advantages of memristors, particularly in terms of area and power efficiency, thus offering a potential solution to the conventional limitations often encountered with traditional ADCs.

In their research documented in reference [63], the researchers introduced an innovative artificial neural network (ANN) analog-to-digital converter (ADC). This ADC design integrates subranging and nonuniform memristors to effectively tackle the challenge of device mismatch. The solution lies in the utilization of a trainable memristor weight, capable of adaptive adjustments, thereby enhancing the performance and reliability of the ADC.

Moreover, a study conducted by the researchers in [64, 65] revealed a synthesizable

ADC that sought to overcome the challenges encountered in conventional ADC designs. This ADC's architecture comprises three distinct hardware layers, mirroring the structure of a conventional neural network: the input layer, the hidden layer, and the output layer.

Nonetheless, the engineers employing adaptive and optimization techniques as discussed in section 1.3, in conjunction with those presented in references [62–65], opt for amplitude-coded signals. However, this choice poses specific challenges in the context of modern CMOS technology nodes.

Conversely, fine-tuning the dimensions of transistors and manipulating the supply voltage in CMOS technology leads to a reduction in gate delay within digital circuits. This progress in CMOS scaling translates to enhanced time resolution, thereby kindling increased enthusiasm for exploring the time domain, as highlighted in references [66]. This incentive spurred researchers to develop systems that leverage spike or time-coded signals, characterized by their technology-agnostic nature, ensuring resilience even as technology evolves, as substantiated by the studies cited [67–69], as exemplified in applications like light sensing [70] or the Dynamic Vision Sensor (DVS) introduced by Delbrück et al. in 2005 [71].

The process of translating analog input signals into input pulse frequencies by utilizing a significant number of spikes can result in an increase in power consumption, particularly when dealing with larger and more intricate spiking neural network (SNN) structures. In this context, it is crucial to find a balance between achieving high performance and minimizing power consumption. Consequently, these attributes may not align with the prerequisites for power-efficient and robust devices in the context of edge computing, a topic explored in-depth in references [72–74].

In response to these challenges, a previous iteration of the sensor-to-spike-to-digital converter (SSDC α) chip was developed to utilize spike timing, simulating acoustic localization [75, 76]. Nevertheless, this initial design fell short in terms of adaptability, a fundamental aspect for ensuring the system's continuous operation in the face of factors like aging, drift, lesions, or damage. The ability to conceive a robust, precise, resilient, and adaptable design becomes of utmost significance in ensuring the overall success of the application system. Achieving this intricate balance is an ongoing pursuit, demanding continuous innovation and refined engineering.

1.5 The Goals of the Thesis

The primary goal of this thesis is to develop an efficient and resilient sensor signal interface system that addresses the challenges of modern CMOS technology while aligning with Industry 4.0 standards. Additionally, the developed system aims to be applicable in other fields, such as automotive, space, aviation, and robotics, where highly robust and adaptive solutions are critical. The system is designed to be technology-agnostic, ensuring that it remains effective across various technological platforms, especially as new technologies emerge. The system aims to achieve the following specific goals:

1.5.1 Development of a Robust and Technology-Agnostic Signal Interface System

Objective: Create a sensor interface system that demonstrates high reliability, precision, and adaptability, capable of maintaining consistent performance despite technological advancements and manufacturing variations. The system will be technology-agnostic, allowing it to be effectively implemented in the most recent technologies where traditional amplitude-mode designs encounter significant challenges.

Sub-goals:

1. **Design of Time-Coded Signal Architectures:** Develop architectures that leverage the enhanced time resolution offered by advanced CMOS scaling, while addressing the limitations of amplitude-coded signals. The design will ensure that the system is technology-agnostic, enabling it to adapt seamlessly across different technology nodes.
2. **Implementation of Self-X Capabilities:** Integrate self-calibration, self-compensation, and self-adaptation mechanisms to ensure the system's longevity and robustness, particularly in demanding fields like automotive, space, aviation, and robotics.
3. **Enhancement of Power Efficiency:** Design the system to minimize energy consumption, particularly in complex signal processing applications, by utilizing time-coded signals with fewer spikes.

1.5.2 Adaptation of Natural Neural Coding Principles

Objective: Employ time-based neural codes inspired by natural nervous systems to create a resilient signal conditioning system that adapts to varying conditions, akin to biological systems. The system will be designed to be technology-agnostic, ensuring its robustness across various technology platforms, including those used in automotive, space, aviation, and robotics.

Sub-goals:

1. **Replication of Biological Robustness:** Design signal conditioning systems that mimic the adaptability and resilience seen in nature, focusing on compensating for both static and dynamic variations, including aging effects.
2. **Integration with Existing Systems:** Ensure the developed system can replace or seamlessly interface with current sensor systems, enhancing yield without requiring labor-intensive "pick-and-place" processes like single-device calibration or trimming.

1.5.3 Methodology

To achieve these goals, the following methods will be employed:

1. **System Architecture Design:** The design process will focus on developing time-coded signal architectures that address the identified challenges in modern CMOS nodes. Simulation will be used to refine the design and validate its performance.
2. **Prototype Development and Testing:** A prototype sensor interface system will be developed, incorporating the proposed time-coded signal approach. The prototype will undergo testing to evaluate its adaptability, power efficiency, and resilience.

1.6 Thesis Structure

This thesis is organized into seven chapters, each addressing a distinct aspect of the research. The first chapter introduces the fundamental concepts of advanced sensory integration and AI technology in Industry 4.0, setting the stage for the subsequent

discussions. The following chapters explore the state of the art, biological inspirations, system design, integration, characterization, and conclusions. Below is a summary of each chapter:

1.6.1 Chapter 1: Introduction

This chapter lays the groundwork for the thesis by discussing the advancements in micro and nano technologies that have driven the development of sensory technologies. It highlights the challenges in sensor signal interface systems, the significance of neuromorphic approaches, and the overarching goals of the thesis in the context of Industry 4.0.

1.6.2 Chapter 2: State of the Art

This chapter provides an overview of the current advancements in sensor technology and sensory systems. It discusses various techniques to address sensor signal interface challenges, including layout matching, design automation, trimming methods, and calibration techniques. Additionally, it covers evolvable hardware and conventional as well as neuromorphic design approaches for scaling challenges.

1.6.3 Chapter 3: Biological Foundations of Neuromorphic Spiking System

The third chapter delves into the biological underpinnings of neuromorphic computing. It examines the sensory systems in living organisms, biological neuron models, and synapses, drawing insights that inform the design and functionality of neuromorphic spiking systems.

1.6.4 Chapter 4: Neuromorphic Spiking Sensory System

This chapter introduces the proposed neuromorphic spiking sensory system with self-X capabilities. It discusses its advantages, such as low-voltage operation, robustness in noisy environments, and minimal power consumption. The core components of the system, the Adaptive Sensor Signal-to-Spike Converter (ASSC) and the Self-Adaptive Spike-to-Digital Converter (SA-SDC), are described in detail.

1.6.5 Chapter 5: Integration of Neuromorphic System Components

Chapter 5 focuses on the integration of neuromorphic system components into an integrated circuit. It discusses the Universal Sensor Interface with Self-X features (USIX), designed to support both amplitude and spike-domain representation. The chapter also details the design process using Cadence tools and XFAB CMOS technology and provides insights into the prototyping and fabrication of the system.

1.6.6 Chapter 6: Neuromorphic Chip Characterization and Application

This chapter presents the experimental characterization of the neuromorphic spiking sensory system. It evaluates the performance of its key components (ASSC and SA-SDC) and describes their integration into a functional system. Additionally, the chapter discusses real-world applications and the role of TMR integration in enhancing the system's capabilities.

1.6.7 Chapter 7: Conclusions

The final chapter summarizes the contributions of the thesis, evaluating the research outcomes against the initial objectives. It highlights the novelty of the proposed neuromorphic spiking sensory system and suggests directions for future research and development in this domain.

Chapter 2

State of the Art

The field of sensor technology and sensory systems is rapidly growing and diversifying, finding applications in various domains [4]. A key aspect of ensuring the overall effectiveness of application systems is the development of reliable analog front ends (AFE) [23]. Figure 1 illustrates the standard sensor signal interface chain [77], which performs key tasks such as signal conditioning, anti-aliasing filtering, and analog-to-digital conversion (ADC). After the in-amp, the small sensor signal may undergo further amplification via programmable gain amplifiers (PGAs) based on operational amplifiers (op-amps) to align with the ADC's full-scale input voltage. The anti-aliasing filter reduces noise to meet the ADC's resolution needs. When an active filter is employed, it can offer additional amplification and act as the ADC driver, managing its high input load and aligning the signal to the ADC's common-mode voltage. Finally, the ADC converts the conditioned analog signal into digital format for further processing. For optimal performance, sensor systems require AFEs characterized by high accuracy, robustness, and adaptability. This chapter provides an in-depth review of techniques for resolving challenges in the sensor signal interface chain and analog evolvable hardware (EHW). Additional challenges faced by complex mixed-signal systems, such as analog-to-digital converters (ADCs), become more pronounced as they transition to smaller technology nodes [32, 78–80]. In this chapter, conventional designs and neuromorphic systems addressing scaling challenges are reviewed, offering insights for designing and fabricating high-performance and reliable AFEs.

2.1 Techniques for Tackling Sensor Signal Interface Challenges

Sensor signal interface systems face multiple challenges, including process variations, environmental stress, and long-term aging effects. Various strategies such as layout matching, design automation, trimming methods, and advanced calibration techniques have been developed to mitigate these issues. Below is a concise overview of these key techniques.

2.1.1 Layout Matching for Process Variations

Layout matching is a common strategy in analog design to reduce mismatches caused by manufacturing variations. Techniques like common centroid and interdigitated configurations, paired with dummy elements, ensure that components like transistors and current mirrors experience identical conditions, mitigating mismatches [81–85]. However, these methods only work for paired devices and cannot address specific deviations of individual components.

2.1.2 Design Automation for Circuit Optimization

Design automation tools, such as MUNEDA’s WiCkeD and ABSYNTH, optimize circuit element sizing to enhance performance and yield under PVT (process, voltage, and temperature) variations [86,87]. However, automating analog IC layout remains difficult, with manual design still being preferred for precision despite its time-consuming nature [88–90].

2.1.3 Trimming Techniques for Post-Production Adjustments

Trimming methods help fine-tune circuits after production. At the wafer level, Zener zapping and laser trimming are widely used to adjust resistor values, but they can be expensive and do not compensate for changes after packaging [91,92]. Post-packaging trimming techniques, like fuse trim links and electrically programmable fuses, allow for adjustments without the need for additional pads, as seen in DigiTrim by Analog Devices [93–98]. For more flexible trimming, EEPROM-based solutions enable multiple programming cycles, useful for correcting aging effects [99,100].

2.1.4 Dynamic Calibration and Compensation

Dynamic calibration techniques adjust circuit performance during operation, addressing both static and dynamic deviations. Techniques like chopping and auto-zeroing help correct offset and noise in operational amplifiers [101–103], while dynamic element matching (DEM) improves linearity in data converters through digital calibration [104, 105].

2.1.5 Evolvable Hardware and Self- capabilities

Evolvable hardware (EHW) uses bio-inspired algorithms to adjust circuits in real-time, enabling systems to self-configure and adapt throughout their lifecycle [106–108]. Self-X properties (self-calibration, self-repair, and self-optimization) are gaining traction, especially in Industry 4.0, where autonomous systems enhance manufacturing efficiency and reliability [54, 109]. These systems continuously monitor and optimize performance, reducing the need for manual recalibration.

2.1.6 On-Chip Measurement and Built-In Self-Test (BIST)

Real-time performance monitoring is critical for self-optimizing systems. Built-in self-test (BIST) units provide real-time feedback, either through direct or indirect measurement methods [110–112]. Non-invasive sensors can be used to measure performance without interacting with the main circuit, making them a cost-effective option for real-time evaluation [113].

2.2 Evolvable Hardware for Addressing Sensor Interface Challenges

2.2.1 Introduction to Evolvable Hardware (EHW)

Evolvable hardware (EHW) refers to systems capable of self-adaptation and optimization, especially in dynamic or unpredictable environments. The concept, introduced by Hugo de Garis in the early 1990s, leveraged Genetic Algorithms (GAs) and Genetic Programming (GP) to evolve complex systems autonomously, without human intervention [114, 115]. EHW systems aim to address the limitations of traditional hardware design, offering flexibility for applications where human design is too complex or ineffi-

cient. Early implementations involved evolving logic circuits using programmable logic arrays (PLAs), where the system's architecture and interconnections could adapt in real-time to changes in the environment or to hardware failures. This concept of "intrinsic evolution" was demonstrated in 1993 with the development of Darwin Machines on a PLA chip, which were capable of autonomously evolving circuits for fault tolerance and real-time environmental adaptability [116, 117].

2.2.2 Analog Evolvable Hardware

In addition to digital applications, the principles of EHW were extended into the analog domain, leading to the development of Field Programmable Analog Arrays (FPAAs). These systems enabled the reconfiguration of analog circuits such as filters and amplifiers, thus facilitating real-time adaptive functionality. Early FPAA systems allowed the dynamic adjustment of key parameters, like transconductance, to optimize performance under varying conditions [118–120]. The introduction of configurable analog blocks (CABs) further enhanced the capability of FPAAs, allowing for more complex functionalities such as the simulation of neural networks. These advancements were crucial for creating adaptive analog circuits that could evolve based on the system's needs [121].

2.2.3 Advancements in Field Programmable Transistor Arrays (FPTAs)

Another significant advancement in EHW was the development of Field Programmable Transistor Arrays (FPTAs). These systems enable evolution at the transistor level, offering flexibility in the design of custom circuit topologies. FPTAs, such as those developed by NASA's Jet Propulsion Laboratory (JPL), allowed the self-reconfiguration of circuits under extreme conditions, which is especially useful for applications like space exploration [122, 123]. FPTAs are composed of arrays of transistors interconnected via programmable MOS switches, enabling the creation of a variety of analog and digital circuits. However, this fine-grained approach presents challenges, such as non-linearity and parasitic capacitance in the switches, which can degrade performance, particularly in high-frequency applications [50, 124].

2.2.4 Applications of Evolvable Hardware in Space and Autonomous Systems

EHW's practical applications have been demonstrated in several high-stakes environments, including space missions and autonomous systems. The Stand-Alone Board Level Evolvable System (SABLES), developed by NASA, integrates evolvable hardware with a Digital Signal Processing (DSP) unit to execute real-time genetic algorithms (GAs) for circuit self-reconfiguration. This system, capable of operating in harsh environments, showcased EHW's potential for self-recovery and adaptation [125–128]. Autonomous robots have also benefited from EHW, where evolvable platforms have enabled real-time adjustment of sensor and control systems. These platforms demonstrate self-healing and self-adapting capabilities, essential for systems deployed in unpredictable and extreme conditions [129–132].

2.2.5 Challenges and Limitations of EHW

Despite its potential, EHW faces several challenges that hinder its widespread adoption. Fine-grained architectures, such as those used in FPTAs, are hindered by power consumption and performance limitations. These systems often experience issues with parasitic capacitance and switch non-idealities, leading to decreased dynamic performance and increased resource usage [133]. Moreover, evolving analog circuits from scratch presents another challenge, as it requires complex optimization algorithms that must explore vast search spaces. The process is often slow and computationally intensive, making it impractical for real-time applications in many cases [134–136].

2.2.6 Hybrid Granularity Approaches

To mitigate some of the limitations associated with fine-grained systems, hybrid granular approaches have been explored. The Field Programmable Medium-Granular Mixed-Signal Array (FPMA) is an example of this approach. It strikes a balance between flexibility and predictability, offering a more practical solution for real-time prototyping while maintaining compliance with industry standards. FPMA systems integrate pre-defined circuit topologies with the flexibility of fine-grained systems, thus allowing for adaptive reconfiguration without the overhead of purely fine-grained systems [137, 138].

2.2.7 Evolutionary Algorithms and Optimization Techniques

Optimization within EHW systems is predominantly driven by evolutionary algorithms like GAs and GP. These algorithms are for solving complex problems where optimal solutions cannot be easily determined through traditional design approaches. GAs, for example, are employed to fine-tune circuit parameters in analog filters [122,124]. Recent advancements have combined intrinsic and extrinsic evolution in what is called "mix-trinsic" optimization. This hybrid approach leverages both real-time on-chip evolution and off-chip simulations, which helps accelerate the process and achieve more accurate results [139].

2.2.8 Built-in Self-Test (BIST) for In-Field Optimization

One of the critical challenges in evolving hardware is the need for real-time performance assessment. Built-in Self-Test (BIST) systems provide an effective solution by incorporating self-calibration and performance monitoring within the hardware. BIST circuits can generate stimuli and measure circuit responses directly on-chip, thus reducing reliance on external equipment [140–142]. BIST solutions can be simple, using envelope detectors to generate low-frequency signatures that correlate with circuit performance. This method reduces testing costs and complexity while enabling efficient performance optimization [143]. More complex systems use advanced neural networks on-chip for self-calibration, improving yield and reliability in real-time applications [144].

2.2.9 Universal Sensor Interface Systems

Universal Sensor Interfaces (USIs) are critical for enabling adaptive sensor systems in EHW. These interfaces are capable of adapting to various sensor types, offering real-time reconfigurability and power management. USIs are especially useful in applications where sensors must operate under different environmental conditions, such as biomedical monitoring and industrial IoT systems [145–148]. The integration of self-X properties into USIs further enhances their robustness and reliability. These systems are increasingly designed with the flexibility to accommodate various physical quantities, such as current, voltage, and temperature, making them versatile for a wide range of applications [61, 149].

2.2.10 Future Directions, Open Challenges, and Conclusion

Evolvable hardware (EHW) holds great promise, but several key challenges remain. A primary issue is improving the dynamic performance of fine-grained systems, which currently suffer from non-linearity and power consumption problems, particularly in high-frequency applications. Optimizing power efficiency and addressing these non-idealities are essential for broader industrial use. Additionally, existing optimization algorithms, while powerful, are often too computationally intensive for real-time applications, limiting their practicality in environments requiring fast adaptation and scalability [61,150]. The integration of Built-in Self-Test (BIST) mechanisms with reconfigurable hardware is another critical area of development. BIST systems must effectively handle real-time variations in hardware performance while providing accurate, low-cost testing solutions for complex circuits. Achieving this would reduce the reliance on external testing equipment and enable more autonomous, real-time optimization, making EHW more viable in industrial settings [151,152]. Looking ahead, the combination of evolutionary algorithms and hybrid granular architectures offers a promising path forward. Hybrid systems strike a balance between the flexibility of fine-grained architectures and the efficiency of predefined topologies, enabling faster and more reliable optimization. As EHW evolves, focusing on reducing complexity, enhancing real-time capabilities, and improving adaptability will be crucial for its application in fields like space exploration, robotics, and industrial automation. In conclusion, while challenges such as improving dynamic performance and optimizing algorithms persist, the advancements in EHW present a strong foundation for future development. Continued research into scalable, adaptable hardware and more efficient optimization techniques will pave the way for robust, real-time, fault-tolerant systems that can autonomously adapt to changing environments [151,152].

2.3 Conventional Design for Scaling Challenges

Cutting-edge methods aim to tackle challenges associated with analog-to-digital converters (ADCs), and several designs have been proposed in academic literature. Conventional ADC circuits frequently demand substantial manual adjustments and redesigns to achieve the desired performance metrics in a new manufacturing process. Research in the past has delved into synthesizable and scalable ADC architectures to streamline this

costly and time-intensive design procedure. This section examines advancements in conventional analog-to-digital converter (ADC) designs that address scaling challenges. The content is organized into subsections, each focusing on key characteristics as suggested.

2.3.1 Flash ADC Techniques

Flash Analog-to-Digital Converters (ADCs) serve as pivotal components in signal processing, providing rapid and efficient conversion of analog signals to digital form. A fundamental challenge in the operation of these converters lies in the inherent input-related offset of their comparators, arising from random device mismatches. Minimizing this offset is paramount for achieving optimal precision in the conversion process. This becomes particularly crucial in the context of subranging flash ADCs, where the offsets of the subrange comparators play a central role in influencing the overall accuracy and reliability of the conversion [153].

Regardless of the regime, the precision of critical comparators must align with the converter's overall accuracy goals. Achieving this demands a considerable area footprint for each comparator to mitigate device mismatch or the adoption of offset-canceling circuit methods like storing offsets at the output, as outlined in [154]. However, the latter approach involves storing offset information on capacitors positioned at the output of gain stages, resulting in elevated power consumption, particularly when multiple cascaded gain stages are necessary [155]. Alternatively, rather than attempting to suppress comparator offset, an intriguing possibility arises by leveraging the random nature of the offset as an integral aspect of a stochastic ADC. Flash ADCs employ a reference ladder to establish comparator trip points for each digital code. The concept of a stochastic ADC, initially introduced in [156], leverages device mismatch to determine these trip points. In this approach, an array of comparators, all drawn identically, is considered. Each comparator comes with a random input-referred offset, and while individual offsets are unpredictable due to their randomness, the complete offset distribution can be characterized by its probability density function (PDF). It has been suggested in [157] that the identification of the offset for each comparator allows the selection of comparators with offsets aligning with a desired transfer function. A similar process of choosing the best among redundant comparators has been previously employed [158]. However, this approach necessitates a computationally intensive foreground calibration to establish a

transfer function. In the case of [157], the calibration logic occupied a substantial area, surpassing the combined space of the remaining components of the ADC, excluding the off-chip computation engine. Alternatively, if the comparator offset adheres to a nearly linear distribution, the resulting offsets can be utilized as the transfer function, eliminating the need for extensive calibration hardware.

2.3.2 Stochastic ADCs

The stochastic flash ADC in [78] introduces randomness in comparator thresholds, deviating from the deterministic design of a standard flash ADC. Each comparator exhibits a random offset, following a Gaussian distribution, which influences the stochastic ADC's behavior. Unlike the predictable output of a standard ADC, the stochastic version lacks a specific order due to random thresholds, necessitating additional decoding. The probability density function (pdf) of the random comparator offset approximates a Gaussian distribution, impacting the voltage transfer function. Achieving linearity in the transfer function requires a sufficient number of comparators in the stochastic flash ADC. In standard flash ADCs, $(2^N - 1)$ comparators are needed for N bits of quantization, but in the stochastic version, determining the required random levels becomes essential for achieving desired accuracy, posing challenges in achieving perfect linearity with a smaller set of comparators.

The stochastic flash ADC relies on a common reference voltage for its comparators, combining their outputs to generate a digital output. Achieving linearity in this setup involves using a significant number of comparators to ensure a Gaussian distribution of input offset. The transfer characteristic indicates optimal linearity for analog inputs below the standard deviation (σ) of comparator input offset. However, if the input offset surpasses σ , the output becomes irrelevant for determining the ADC digital output. Despite the need for numerous comparators, various strategies have been proposed to enhance linearity efficiently in stochastic flash ADCs.

In a study detailed in [159], an innovative approach is employed to enhance the linearity of a stochastic flash ADC equipped with two comparator groups. The technique involves dynamically swapping the reference voltages between the two groups of comparators. If the input offset of a comparator in one group falls outside the linear input range, its reference voltage is exchanged with that of a comparator in the other

group. This adaptive swapping of reference levels between the two groups contributes to the overall improvement in the linearity of the stochastic flash ADC, all achieved with straightforward hardware modifications.

2.3.3 Synthesizable ADC Architectures

Other researchers have endeavored to tackle the intricate design challenges posed by advanced nanometer-scale CMOS processes. In their pursuit, they introduced delta-sigma ADCs based on a synthesis-friendly ring voltage-controlled oscillator (VCO) [160]. The design adopts a decomposition strategy, breaking down the structure into digital gates and a concise set of custom cells integrated into the standard cell library. The closed-loop VCO-based ADCs in this design utilize feedback loops to mitigate nonlinearity. However, an issue arises when the main ADC block operates independently, causing the VCO to be affected by process variation. In essence, the performance of ADCs is compromised by process variations. Additionally, careful attention is required for passive devices to address mismatch concerns, whether in capacitors or resistors.

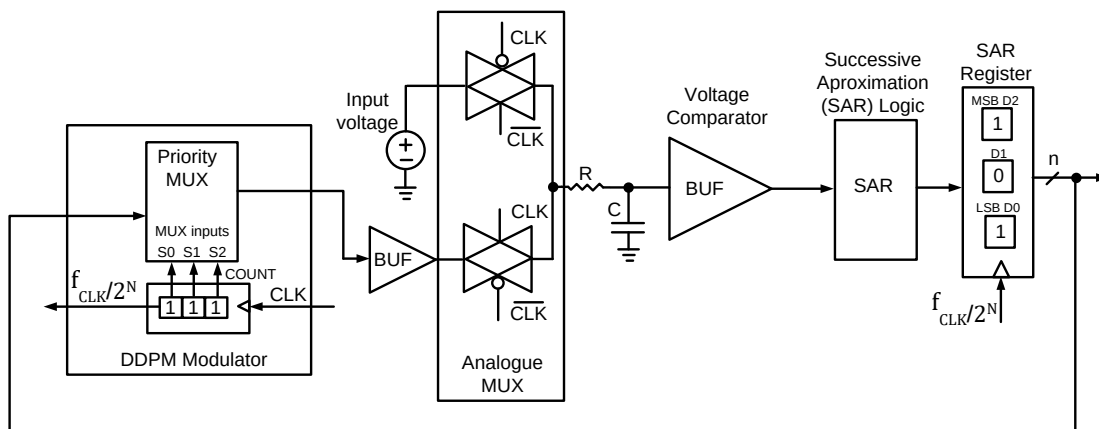


Figure 2.1: The Proposed Architecture of the DDPM ADC. [161].

In addressing the intricate challenges of advanced nanometer-scale CMOS processes, previous research has delved into the development of fully-synthesizable Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) [161]. Their focus involves creating ADC architectures amenable to synthesis with standard cells, streamlining integration with the digital sub-system. An innovative approach is introduced, wherein ADCs pivot away from traditional capacitive DACs, opting for a Dyadic Digital Pulse Modulation (DDPM) Digital-to-Analog Conversion methodology. Demonstrating performance, the ADC architecture achieves a 6.4-bit Effective Number of Bits (ENOB)

at a 2.8kS/s sampling rate. The DDPM ADC proposal aligns with the structure depicted in Figure 2.1. However, the sampling rate of their approach faces limitations due to the requirement for a high-speed clock in the control logic. To achieve a high sampling rate, an extensive number of channels is essential. Yet, adopting the pipeline architecture for the channel ADC poses a challenge, as it would consume significant power to meet the necessary performance criteria.

2.3.4 Delta-Sigma and Hybrid ADC Architectures

Concurrently, Semtech, a leading semiconductor industry, has introduced the groundbreaking Zooming ADC innovation, embodied in chips such as the SX8724, showcasing advanced digital reconfigurability. Their goal was to overcome the constraints typically associated with conventional ADCs. Zooming ADCs strive to synergistically leverage the advantages of different ADC architectures, aiming to achieve performance levels that cannot be attained by any single architecture [162–167]. In a similar vein, researchers have explored various ADC architectures to address the challenges posed by advanced nanometer-scale CMOS processes. While successive approximation register (SAR) ADCs are recognized for their energy efficiency, their resolution is commonly restricted to around 12 bits without extensive calibration and trimming [168, 169]. On the other hand, Delta-Sigma ($\Delta\Sigma$) ADCs can achieve enhanced resolution through oversampling and noise shaping, but the energy efficiency of high-order $\Delta\Sigma$ modulators ($\Delta\Sigma$ Ms) and multi-bit $\Delta\Sigma$ Ms is compromised due to a higher oversampling ratio (OSR) and the use of multiple integrators [167, 170–172]. In a similar vein, multi-stage noise-shaping (MASH) architectures can attain a substantial dynamic range (DR) with a low oversampling ratio (OSR). However, they frequently depend on ensuring alignment between internal analog and digital transfer functions, potentially necessitating extensive calibration [173–175].

Amid these diverse approaches, Incremental $\Delta\Sigma$ ADCs, frequently employed in high-dynamic-range (DR) applications, involve resetting the modulator at the initiation of each conversion. Due to the finite impulse response (FIR) nature of the modulators in incremental $\Delta\Sigma$ s, their corresponding decimation filters can adopt a simpler structure, often a cascade of integrators. This stands in contrast to $\Delta\Sigma$ counterparts utilizing infinite impulse response (IIR) decimation filters, showcasing a notable simplification.

Noteworthy advantages of incremental $\Delta\Sigma$ s include straightforward multiplexing, low latency [176–180], and reduced susceptibility to idle tones [179]. However, it is essential to acknowledge that incremental $\Delta\Sigma$ s come with a trade-off – their extended conversion time leads to diminished energy efficiency. As a consequence, their application is generally confined to very narrow bandwidths [176, 181]. This highlights the significance of innovations like ZoomingADC, as they aim to offer a comprehensive solution to the challenges across various ADC architectures. The fundamental idea behind the Zoom ADC involves a carefully devised two-step process. The general idea of a two-step ADC is depicted in Figure 2.2. It starts with a primary low-resolution ADC stage tasked with a broad conversion of the input signal. The output then undergoes processing through a Digital-to-Analog Converter (DAC). The difference between the original input and the DAC’s output forms the ‘residue,’ refined further in the second stage. This second stage employs a fine ADC with a limited conversion range.

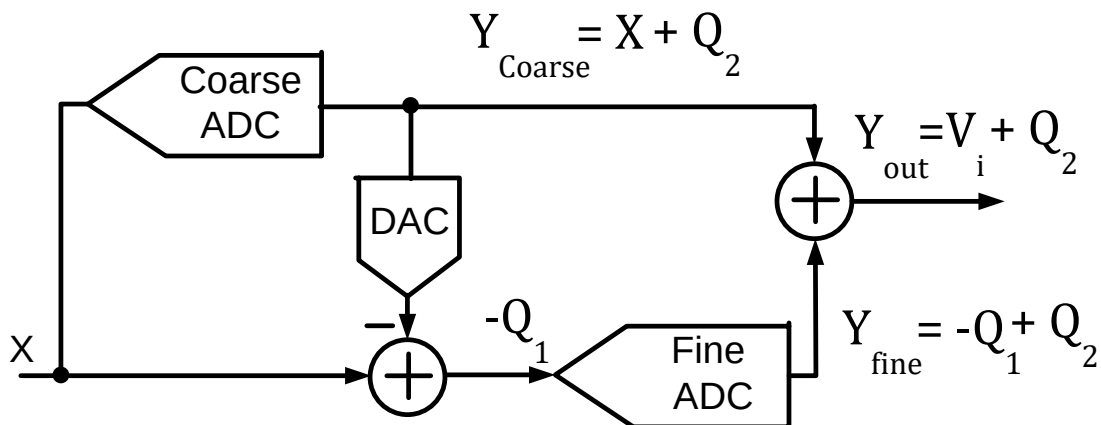


Figure 2.2: The Architecture of a Two-Step ADC [165].

In recent times, there has been a notable increase in the emergence of hybrid ADCs [165–167, 182–186]. These innovative ADCs strategically amalgamate the advantages inherent in various architectural approaches, resulting in enhanced performance that surpasses the capabilities achievable by a single architecture. The Zoom ADC, exemplified in a study from [182], cleverly integrates SAR ADC and 1st-order delta-sigma converter designs to optimize resolutions and energy efficiency for temperature sensor applications. The approach involves an initial SAR ADC conversion to narrow the signal range, followed by a fine conversion using a simplified sigma-delta ADC circuit. In a subsequent work from [183], a two-step zoom ADC is introduced, employing a 5-bit

SAR conversion followed by a 10-bit $\Delta\Sigma$ conversion, further enhancing its suitability for temperature sensor applications. This innovative design incorporates a modified 1st-order SC $\Delta\Sigma$ -ADC, featuring a SAR algorithm for efficient coarse conversion and a $\Delta\Sigma$ charge-balancing scheme for fine conversion. Utilizing 24 unit sampling capacitors and a folded-cascode opamp, the design eliminates the need for gain boosting, resulting in reduced power consumption and a more compact footprint. Within the realm of zoom ADCs, a distinctive approach is observed in [183], where an incremental $\Delta\Sigma$ ADC serves as the fine converter in a two-step ADC, devoid of residue computation. The outcomes of the coarse conversion play a pivotal role in dynamically adjusting the references of the fine ADC, aligning its input range with the current value of the input signal. This strategic adjustment significantly relaxes the resolution requirements of the fine ADC, given its reduced input range compared to the coarse ADC. However, it's essential to note that the linearity of the coarse ADC remains constrained by component matching.

In a following study, as outlined in [165], researchers devised an incremental zoom ADC, aiming to enhance both energy efficiency and overall performance. This innovative architecture operates in two steps, commencing with a coarse SAR ADC coupled with a fine incremental $\Delta\Sigma$ ADC. The initial phase involves the SAR ADC executing a coarse conversion with relatively lower resolution. In the ensuing fine conversion, the outcome is strategically utilized to adjust the references of the $\Delta\Sigma$ ADC, honing in on a narrow range around the input signal. Unlike traditional two-step ADC structures, the fine converter in a zoom ADC doesn't digitize the residue from the coarse converter. Consequently, the conversion accuracy is solely contingent on the precision of the fine converter. The zooming mechanism introduces a flexibility in the resolution requirement for the fine converter, leading to expedited conversion times and reduced internal signal swings. This, in turn, facilitates the use of uncomplicated and energy-efficient amplifiers, with the study employing inverter-based integrators. Notably, the ADC's performance is augmented through the incorporation of dynamic error correction techniques, such as dynamic element matching (DEM) for heightened linearity, alongside auto-zeroing and chopping to minimize offset and $1/f$ noise. Nonetheless, its sequential operation restricts its bandwidth to a mere 12.5 Hz. Addressing this limitation, the dynamic zoom ADC introduced in [166] takes a novel approach by concurrently running the SAR ADC and $\Delta\Sigma$, enabling effective handling of audio signals. However, its utilization of a 5-bit

synchronous SAR ADC comes with a drawback – the references of the $\Delta\Sigma$ undergo updates only once every five clock cycles. This design choice renders it susceptible to swift out-of-band interferers, posing a risk of overloading the $\Delta\Sigma$. In a subsequent investigation, detailed in [167], researchers proposed an enhanced dynamic zoom ADC. This version employs an asynchronous SAR, ensuring the $\Delta\Sigma$ references are updated every clock cycle. This modification not only enhances tracking capability but also bolsters resistance against out-of-band interference. Additionally, the altered design relaxes the loop filter’s input swing, facilitating an energy-efficient implementation.

However, drawbacks accompany the utilization of zoom ADCs. To compensate for non-idealities in SAR ADCs, the fine $\Delta\Sigma$ Ms in zoom ADCs are typically designed to encompass at least ± 1 LSB of over-ranging [165–167, 184]. For a 1-bit $\Delta\Sigma$, this implies that the modulator’s DAC must span at least three SAR LSBs, leading to a notable reduction in SQNR. Another challenge arises from the leakage of the SAR ADC’s quantization noise, a vulnerability shared with other MASH ADCs. This vulnerability stems from the implicit assumption that the signal transfer function (STF) of the $\Delta\Sigma$ is precisely unity, which is often not the case, especially at higher frequencies [167]. Mitigating these issues usually involves increasing the modulator’s oversampling ratio (OSR) or implementing a digital noise cancellation filter, but both strategies inevitably lead to higher power consumption [184]. Previous iterations of zoom ADCs also grappled with limited robustness against out-of-band interferers.

In a study outlined in [185], researchers proposed a discrete-time (DT) zoom ADC architecture that addresses SQNR loss and quantization noise leakage without compromising energy efficiency. While a continuous-time (CT) loop filter permits the use of low-power ADC drivers and provides inherent anti-aliasing, a DT loop filter exhibits greater robustness to component mismatch and, consequently, eliminates the need for calibration. By employing a $\Delta\Sigma$ with a 2-bit quantizer, fully leveraging the existing DAC levels, the SQNR can be enhanced by approximately 9.5 dB. The incorporation of an analog feed-forward path ensures a unity STF, significantly reducing quantization noise leakage. Collectively, these techniques facilitate a noteworthy reduction in OSR while concurrently enhancing the ADC’s resilience against out-of-band interferers. Nonetheless, the study in [185] highlights a common concern: many existing designs are characterized by substantial area requirements and a significant reliance on the ana-

log performance of CMOS technologies. Addressing this issue, a subsequent investigation [186] introduces an innovative architecture that amalgamates the counting ADC and CT-incremental-DSM (CT-IDSM) within the framework of a zoom ADC. The proposed zoom-incremental-counting (ZIC) ADC architecture stands out for its noteworthy attributes, being not only power-efficient but also compact in terms of area and predominantly digital. Operating at Nyquist sampling, it supports single-shot conversion and facilitates channel multiplexing. Moreover, it boasts a high-impedance input with full-scale common-mode rejection, enabling direct interfacing with various signal sources. Nevertheless, Zoom ADCs face challenges associated with their two-step conversion process, leading to a lower speed compared to ADCs completing the conversion in a single step. Additionally, the necessity for different clock systems during the two conversion periods introduces complexity to the clock circuit and potential errors. Furthermore, the incorporation of two distinct basic ADCs in their design raises concerns about increased area requirements, particularly in the implementation of high-order ADCs.

2.4 Neuromorphic Design for Scaling Challenges

Traditional digital architectures vary fundamentally from neural architectures. The pursuit of optimal solutions characterizes many real-life challenges, with pattern recognition and classification problems standing out prominently. Among these, the ADC problem holds significance. This section delves into neuromorphic approaches to address scaling challenges in analog-to-digital converters (ADCs). These methods are inspired by neural network principles and leverage their adaptive and parallel processing capabilities. The content is organized into subsections based on different neuromorphic techniques.

2.4.1 Hopfield Network-Based ADCs

The 1980s witnessed the rise of neural networks, gaining popularity through the introduction of backpropagation and Hopfield networks. Hopfield's discovery revolved around the symmetric feedback loop from the output to the neural network's inputs, resulting in the creation of an energy function. This function typically tends to converge to reach the lowest point [187]. These systems boast high parallelism and possess optimization potential for addressing a multitude of problems. In his study [188], Hopfield explores

the application of analog VLSI neural networks to address complex problems, initiating the discussion with the challenge of AD conversion. He employs analog amplifiers as neurons, incorporating feedback mechanisms and robust interconnectivity. The resistors within the structure serve as weights.

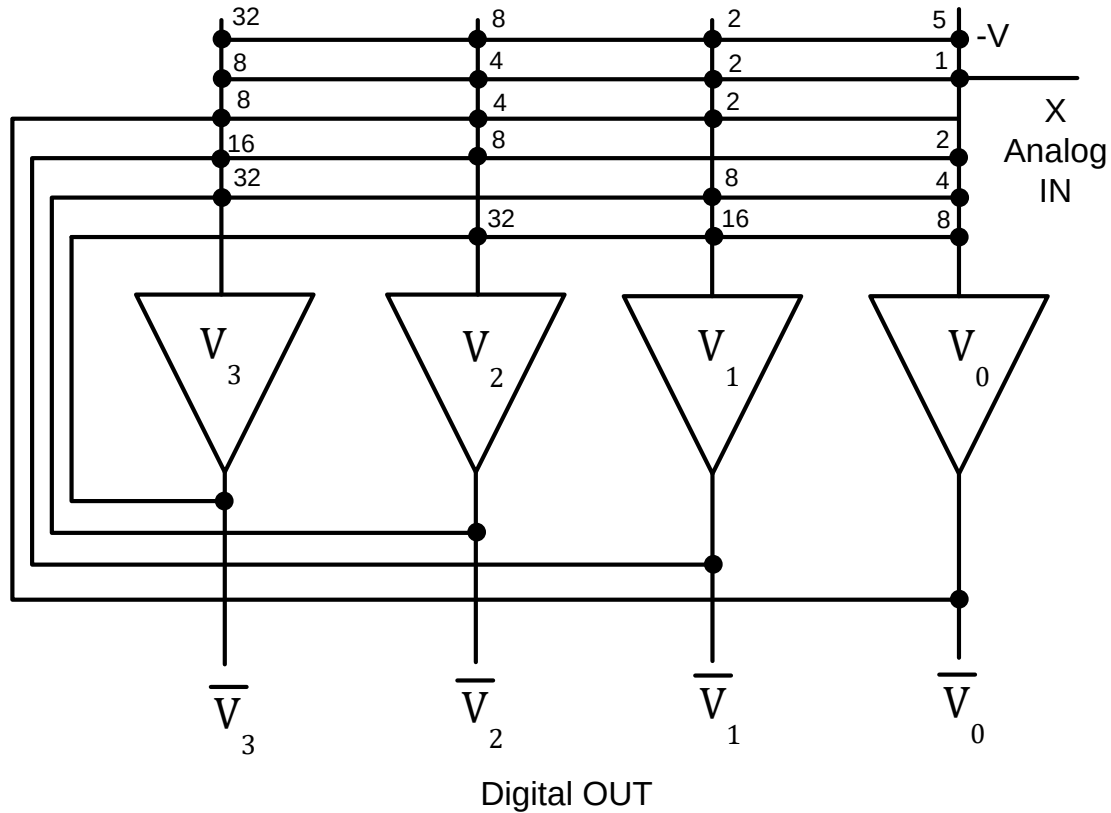


Figure 2.3: Hopfield Neural Network-Based 4-Bit Analog-to-Digital Converter [188].

Figure 2.3 illustrates the Hopfield 4-bit ADC, comprising four inverting amplifiers, each dedicated to a specific bit. These amplifiers, assumed to possess negligible time constants, link their inputs to a resistor, establishing connections to a reference ground and a capacitor. The system performs integrative analog summation of input currents from various network components, exhibiting attractor states (energy surface) that eventually attain the required states with an ideal starting point. The authors observe rapid convergence, albeit with a reliance on precise initial conditions to avoid getting trapped in local minima. Despite these drawbacks, the neural ADC operates entirely in parallel, yielding all digital word bits simultaneously. Additionally, the ADC demonstrates adaptability, allowing for adjustments to the device's conductances (resistances). This adaptability proves useful in compensating for device mismatches and addressing long-term drifts [189]. Notably, this neural ADC represents the pioneering instance in its cat-

egory, subsequently undergoing enhancements by numerous researchers [189–192]. The exploration of novel design techniques for mitigating local minima challenges in the Hopfield neural-based analog-to-digital (A/D) converter is detailed in [189]. This innovative approach involves the incorporation of correction logic circuitry at the amplifier outputs. Simultaneously, the resistive network undergoes expansion to encompass extra feedback from the correction logic circuitry. The purpose of this correction logic circuitry is to oversee the amplifier outputs, generating correction information subsequently introduced as supplementary inputs to the amplifiers.

The investigation detailed in [190, 191] focuses on a category of neural networks featuring nonsymmetrical connections, aimed at enhancing the Hopfield ADC. The primary goal is to examine the dynamic behaviors of these structures to establish their distinctive equilibrium point. It was discovered that a lower triangular matrix, indicative of a nonsymmetrical network, effectively eliminates local optima, thereby addressing the issue of unfavorable initial conditions. In their exploration, the researchers identified that the resistances within the network could be substituted with an $R/2R$ ladder. This substitution offers notable advantages for the overall resistance distribution across the network. The alteration of V_{ref} facilitates a shift in the obtained code to BCD, and a similar approach enables the generation of Gray codes. This method proves highly practical for constructing n -bit ADCs. By orchestrating the information to cycle through the ADC and a shift register for storage, a cyclical cascade is formed, allowing the extraction of numerous bits. However, it's important to note that this method sacrifices the parallelism advantage inherent in neural networks. In [192], a novel approach to enhance the design presented in [189] involves the introduction of a multilevel neuron and multilevel nonlinearities. The authors put forth an energy function specifically tailored for discrete multilevel neural networks. This energy function distinguishes itself by accommodating more than two discrete levels in both the neuron output and threshold settings. In contrast to conventional practices, the circuit designed by the authors avoids the incorporation of weight resistors. This deviation is motivated by the fact that resistors typically necessitate substantial space and precise conductance ratios, posing challenges for the implementation of large neural networks. Instead, they compensate for this limitation by employing a greater number of amplifiers and transistors. Notably, the determination of neuron weights relies on the MOS transistor geometry ratio. However,

it's essential to acknowledge that this method introduces higher nonlinearities compared to the techniques outlined earlier.

Despite being the initial ADC to gain popularity through a neural approach, Hopfield's ADC faced challenges due to its recurrent structure, specifically issues arising from local minima. The ADC's reliance on precise initial conditions posed a hurdle in achieving the desired attractor states. Although modified circuits have been developed to address these issues, they come with their own set of complexities, reduced resolution, non-linearity, and, in certain instances, a compromise on the parallelism that has traditionally been a strength of this structural design.

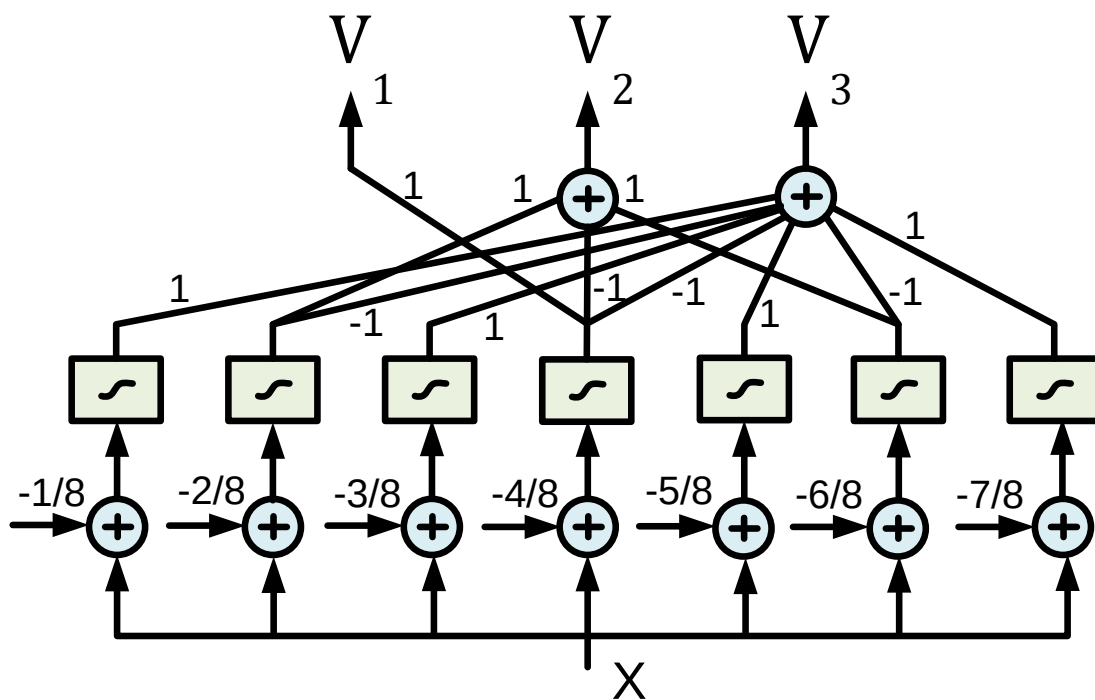


Figure 2.4: Synthesized Binary-Coded ADC [193].

2.4.2 Neural Network-Based ADCs

Growing interest surrounds the development of neural network-based analog-digital converters (ADCs) since Hopfield's pioneering work, resulting in various proposed neural-based ADCs [193]. Post-Hopfield, numerous authors have suggested diverse approaches to address associated inconveniences [189–192]. These solutions, however, often lead to increased complexity or diminished conversion speed. This exploration prompted researchers in [193] to elucidate systematic methods for synthesizing feedforward neural ADCs. The focus was on three distinct neural approaches, thoroughly examined for their

potential role in ADC synthesis. The first is ‘Synthesis by Superposition of Sigmoidal Functions’. Treating the ADC problem as a classification challenge, a multi-layer perceptron is trained to function as an ADC. Faced with challenges in traditional perceptron training employing backpropagation, the authors opt for utilizing a superposition of sigmoidal functions to represent the ADC. Each function corresponds to a specific ADC state and is trained utilizing an optimization algorithm. The initial attempt involves synthesizing a 3-bit ADC utilizing this approach, as depicted in Figure 2.4. This structure resembles a Flash ADC but offers easier implementation of the decoding circuit compared to a Flash ADC.

The second is ‘Synthesis by N-layer Perceptrons’. This approach capitalizes on the weighted nature of the code to synthesize the ADC, determining output digits in descending order from the most significant bit (MSB) to the least significant bit (LSB). Various techniques have been employed to synthesize structures akin to conventional ADCs such as the equilibrium encoder, Successive Approximation ADC, and algorithm ADC. The third ‘Synthesis using Neural Nets with Lower Triangular Interconnecting Structure’ involves operating within Hopfield networks, utilizing network connections and transition states for every connection matrix featuring diverse thresholds. Adjustments are made to weights and thresholds until the intended transition states are achieved. One of the results obtained includes the synthesis of a 4-bit ADC. Highlighting a crucial aspect, it’s worth emphasizing that three methodologies generate certain schemes already documented in technical literature but arrived at through distinct methods. Furthermore, nearly all the structures under consideration possess a non-neural equivalent. Despite this, the exploration has led to the discovery of novel schemes, without an exhaustive examination of all potential alternatives. In essence, this suggests that the neural approach harbors significant potential for unveiling innovative high-level architectures.

Motivated by studies exploring the integration of neural networks in ADC design, the work presented in [194] delves into the realm of complex system modelling utilizing artificial neural networks (ANNs). Acknowledging the challenges inherent in ADC modelling, the proposal introduces a fresh perspective by leveraging an Artificial Neural Network, as depicted in Figure 2.5. In pursuit of this objective, the frequently employed ANN architecture involves a feed-forward network with one or more hidden layers, complemented by the back-propagation learning algorithm. In this approach, a specific ADC

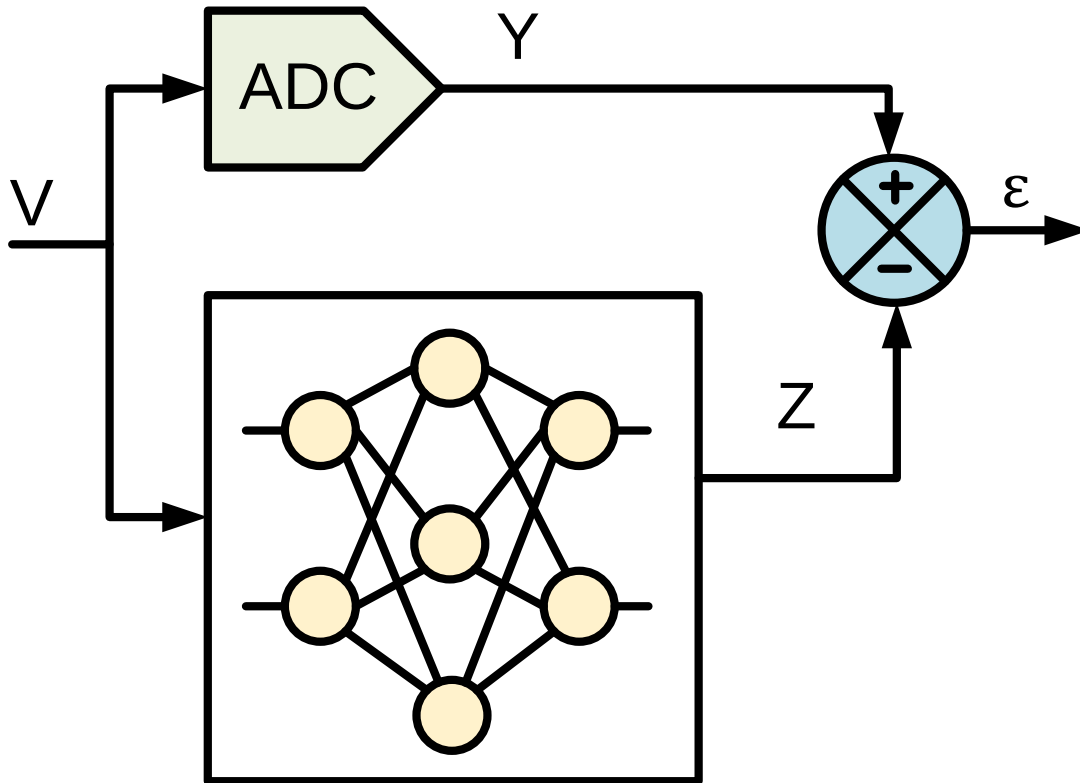


Figure 2.5: Neural Model of an ADC [194].

with precision serves as a reference, providing the network with a learning foundation. The resulting network might exhibit comparable precision to the reference ADC while potentially achieving significantly enhanced operational speeds.

In a separate study, detailed in [195], a researcher introduces a compensatory technique for an Analog-to-Digital Converter (ADC), depicted in Figure 2.6. This technique is implemented in both software and hardware description language, aligning with the ADC neural modeling approach. The neural network undergoes training by learning from a Look Up Table generated through the processing of ADC output for sine wave inputs.

Moreover, as detailed in [196], the authors introduce a bio-inspired ADC employing successive integrate-and-fire operations reminiscent of spiking neurons. This design is tailored for applications in the biomedical field. The methodology shares similarities with a conventional sequential pipeline converter. In this process, the incoming voltage energizes a capacitor, and the subsequent calculation of discharge time determines the most significant bit (MSB) of the ADC. The residual output undergoes conversion from time to voltage, is amplified by a factor of 2, and is fed back to the inputs. This approach

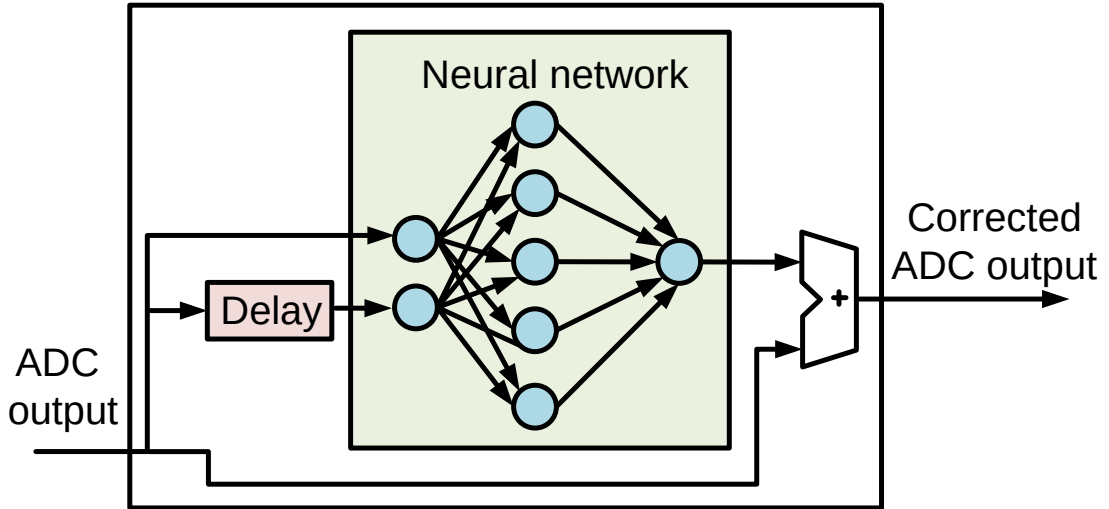


Figure 2.6: Neural Network-Based ADC Correction Scheme [195].

allows for the creation of a design where resolution linearly depends on time. Additionally, the incorporation of synchronizing clocks enhances accuracy and compensates for potential errors.

2.4.3 Spiking Neuron ADCs

The researchers in [197] present an ADC based on Artificial Spiking Neurons (ASNs). This approach constructs an ADC using spike interval times, where each analog input produces a unique spike pattern. Figure 2.7 illustrates a simple circuit model of their method. In this figure, $U(t)$ represents an input signal derived from the digital input Y , while $B1(t)$ denotes a periodic sawtooth signal with period T . These two voltage inputs, $B1(t)$ and $U(t)$, are connected in series and are synchronized with a clock signal of period T . The term 'Th' indicates the threshold voltage in the ASN circuit model, and 'MM' refers to the monostable multivibrator. The ASN-ADC architecture lacks active calibration to address component mismatches or environmental variations. It assumes ideal conditions for resistors, capacitors, and threshold values (e.g., $C = 20 \text{ nF}$, $I_0 = 0.20 \text{ mA}$). Unlike traditional 'pick-and-calibrate' ADCs, which adjust components post-fabrication, this design relies on static parameter assumptions, making it susceptible to real-world imperfections. It is important to highlight that the solution presented in [197] is not an integrated design but rather modeled with off-the-shelf, discretely packaged electronic components. As a result, the use of a 20 nF capacitor although practical in a discrete setup would be unrealistic for an integrated chip solution due

to the significant area it would occupy on the die. Moreover, the continuous spiking operation of the ASN-ADC inherently results in substantial power consumption. Each spike resets the integrator, causing repeated charging and discharging of capacitors. This issue is further amplified by the use of non-optimized components, such as TLC4066ID switches and LM339 comparators, which are not designed for low-power applications. Additionally, the design does not incorporate adaptation mechanisms to compensate for temperature fluctuations or aging effects. While the paper validates the ASN-ADC through idealized PSPICE simulations and mathematical proofs, it lacks experimental data from physical prototypes. Real-world deployments would require supplementary circuitry, such as temperature compensation or auto-zeroing, to maintain accuracy.

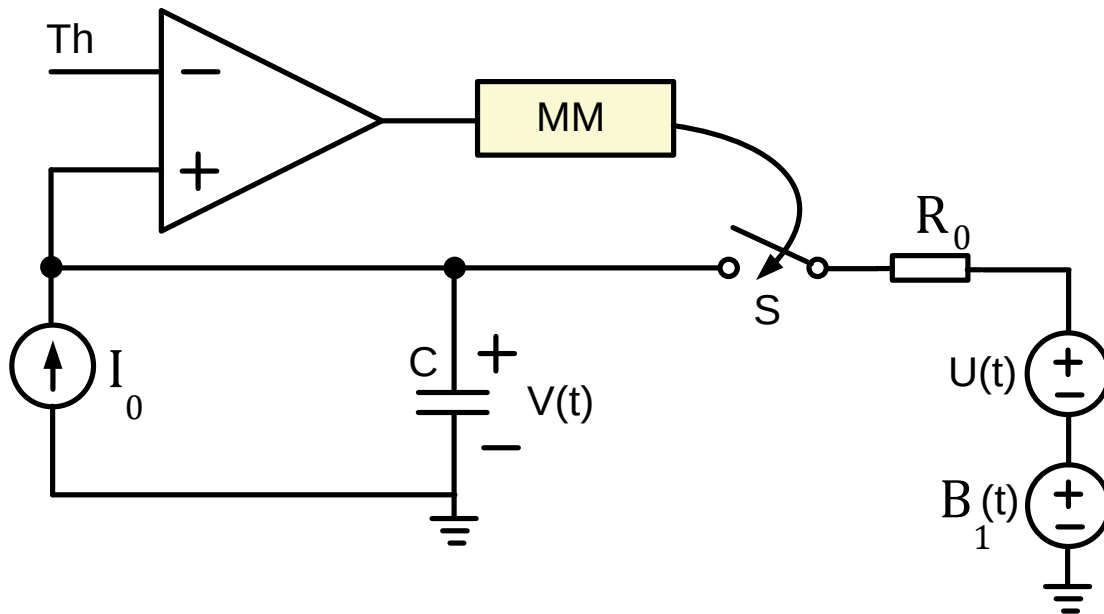


Figure 2.7: The Proposed ADC Based on Artificial Spiking Neurons [197].

The parallel neuromorphic ADC presented in [198] employs spiking integrate-and-fire (I&F) neurons to convert analog signals into time-based digital signals. The design consists of two groups of neurons: "On" neurons, activated when the input voltage exceeds a reference level (e.g., above a midpoint voltage V_{mid}), and "Off" neurons, triggered when the input falls below V_{mid} . These voltage domains align with the ADC's input range, enabling bipolar signal encoding through complementary excitation and inhibition. Lateral inhibition is implemented via inhibitory interneurons connected to each group. When a neuron fires, its interneuron generates a feedback spike that temporarily suppresses all other neurons in the same group, distributing spikes uniformly over time. However, the

paper does not explicitly explain how the input value range maps to specific neurons within a group firing. This ambiguity makes it difficult to assess how the parallel architecture improves resolution or linearity compared to single-neuron designs, which is a critical weakness in evaluating its efficacy relative to other approaches. The prototype, constructed with off-the-shelf ICs and discrete components (e.g., 12 k Ω resistors, 220 pF capacitors), employs five 'On' and five 'Off' neurons but omits post-fabrication calibration techniques, such as those used in traditional ADCs. In conventional designs, these techniques involve measuring component mismatches (e.g., resistor/capacitor variations) and either selecting matched components or digitally calibrating their offsets. Without dedicated calibration circuitry, the neuromorphic ADC cannot compensate for inherent circuit mismatches (e.g., variations in neuron thresholds or integrator time constants). This omission limits its precision, as uncorrected mismatches introduce nonlinearities and reduce effective resolution, particularly in high-accuracy applications. The design also lacks dynamic adaptation mechanisms (e.g., tunable thresholds or auto-zeroing) to mitigate environmental variations like temperature drift or aging effects. The ADC's operation depends on continuous spiking from both neuron groups to maintain a constant output rate. As input amplitudes increase, neurons fire more frequently, leading to higher dynamic power consumption. This issue is exacerbated by non-optimized off-the-shelf ICs, including 74HC14 Schmitt triggers and ULN2803 Darlington arrays, which are not designed for energy efficiency. Translating this architecture into a chip requires addressing several challenges, such as replacing discrete resistors (e.g., 12 k Ω , 2.7 k Ω) and capacitors (220 pF) with on-chip equivalents. The large 220 pF capacitor, for example, would occupy substantial area in an integrated design, further highlighting the need for calibration to minimize component count and mismatch sensitivity.

The NEF-based ADC employs the Neural Engineering Framework (NEF) to convert analog signals into digital representations [199]. In this design, an analog input signal is encoded by a population of spiking neurons, each characterized by a unique tuning curve that determines its response to changes in the input. These tuning curves are scaled by a set of encoder weights, which modulate how strongly each neuron reacts to the input signal. The neurons produce spikes at a rate proportional to the input with higher input signals generally causing higher spike rates. To obtain the digital output, the spikes are summed and processed through a linear decoder, which uses

precomputed decoder weights to transform the spike trains back into a digital value representing the original analog signal. An exponential filter, or kernel, is then applied by the decoder to smooth out the spikes over time, producing a stable digital output. To address hardware variations due to manufacturing processes, the NEF-based ADC employs a 'pick-and-calibrate' approach, requiring custom decoder weights to be calculated for each individual chip instance. This adaptation ensures proper functionality, even for static compensation. Despite this adaptation to manufacturing inconsistencies, the NEF ADC does not account for dynamic environmental changes such as temperature fluctuations or variations in supply voltage (VDD), which can impact performance over time. Additionally, the NEF ADC heavily relies on spike rate encoding, where stronger input signals trigger more frequent spikes. This continuous spiking, even during output stabilization, results in significant power consumption, measured at 160 mW. Furthermore, the NEF ADC's dependence on precomputed decoder weights introduces stability challenges, as it struggles to maintain accuracy when operating conditions, like VDD or temperature, deviate from those used during initial calibration.

2.4.4 Memristive Neural ADCs

Inspired by research investigating the incorporation of neural networks into ADC design, along with advancements in devices like memristors and resistive random-access memory (RRAM), recent studies have introduced innovative ADC structures.

The research presented in [62] introduces a novel architecture for an analog-to-digital converter (ADC) known as the pipelined Hopfield neural network memristive ADC. This innovative approach aims to capitalize on the benefits of memristors in terms of area and power efficiency, overcoming typical constraints associated with traditional ADCs. By integrating memristors, the proposed ADC structure, illustrated in Figure 2.8, is designed based on neural networks.

To address precision limitations impacting the number of memristor resistance states, the low-precision ADC sub-block depicted in Figure 2.9 is extended through a pipeline structure. This sub-block comprises three key modules: a 2T2R synaptic unit, a neuron unit, and a random perturbation unit (RPU). The 2T2R synaptic unit involves components such as a NMOS tube, a PMOS tube, an inverter, and two memristors, controlled by the RPU. The RPU unit primarily incorporates operational amplifiers, data selectors,

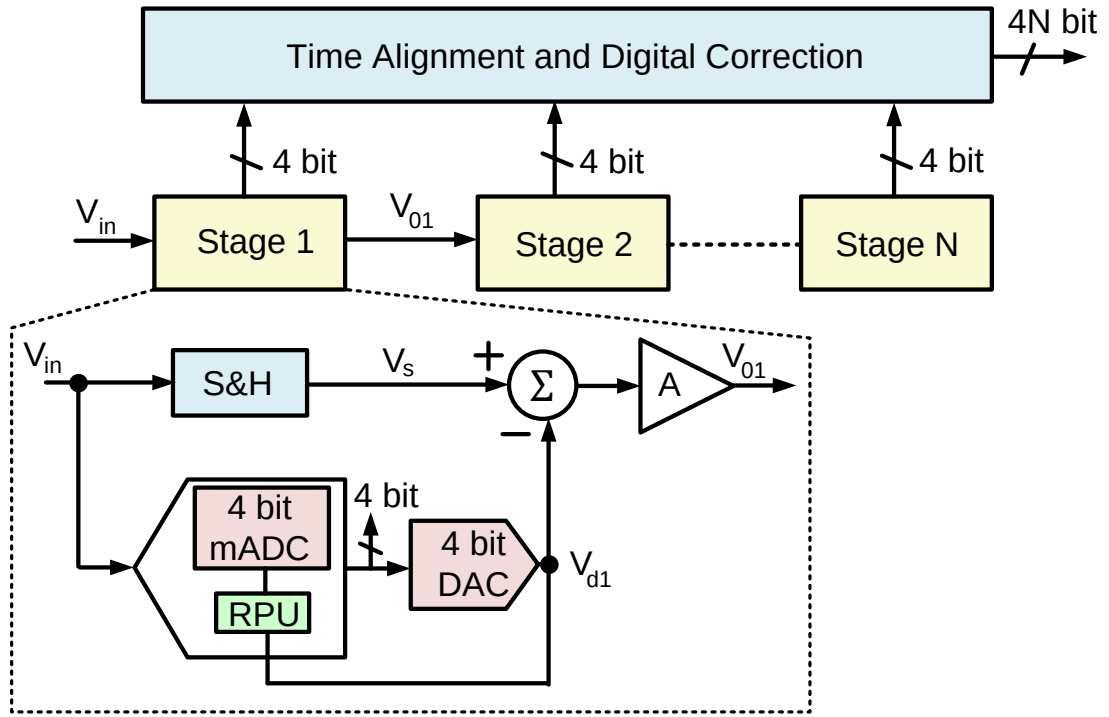


Figure 2.8: The Proposed Architecture of a Pipeline Memristive ADC [62].

NAND gates, a random number generator (RNG), and a T trigger. Notably, the random weight change (RWC) algorithm has been modified for weight tuning.

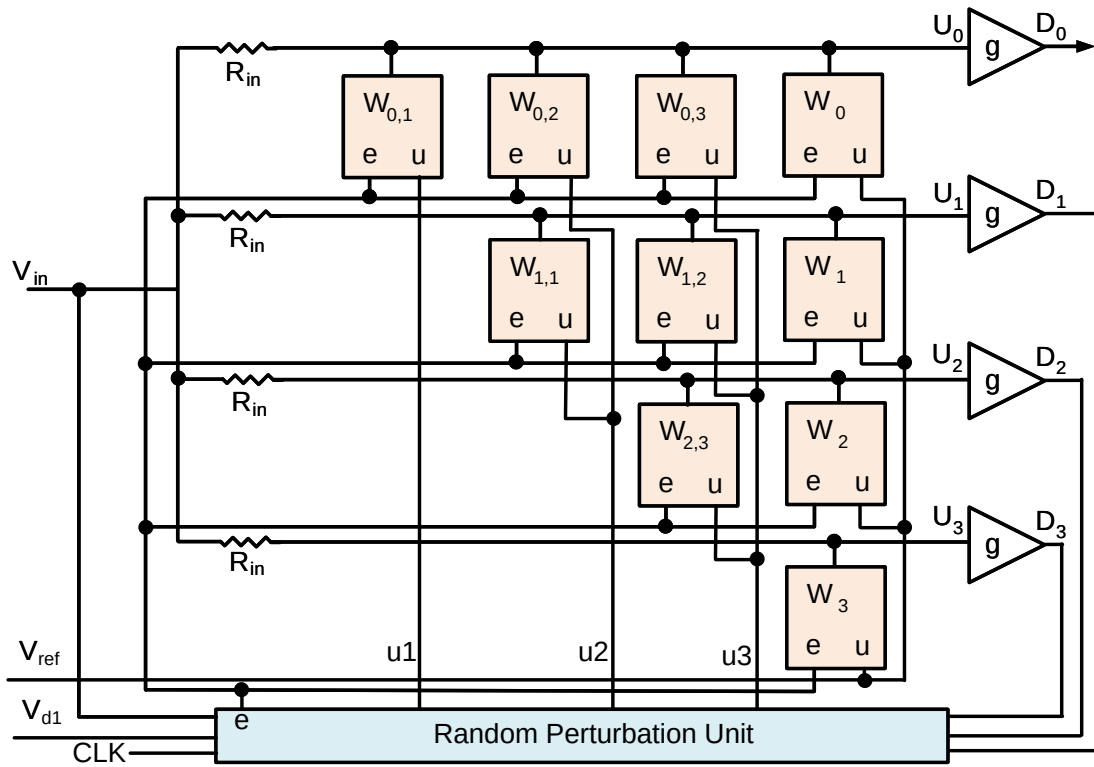


Figure 2.9: Circuit Diagram of RPU and 4-bit mADC Sub-Block [62].

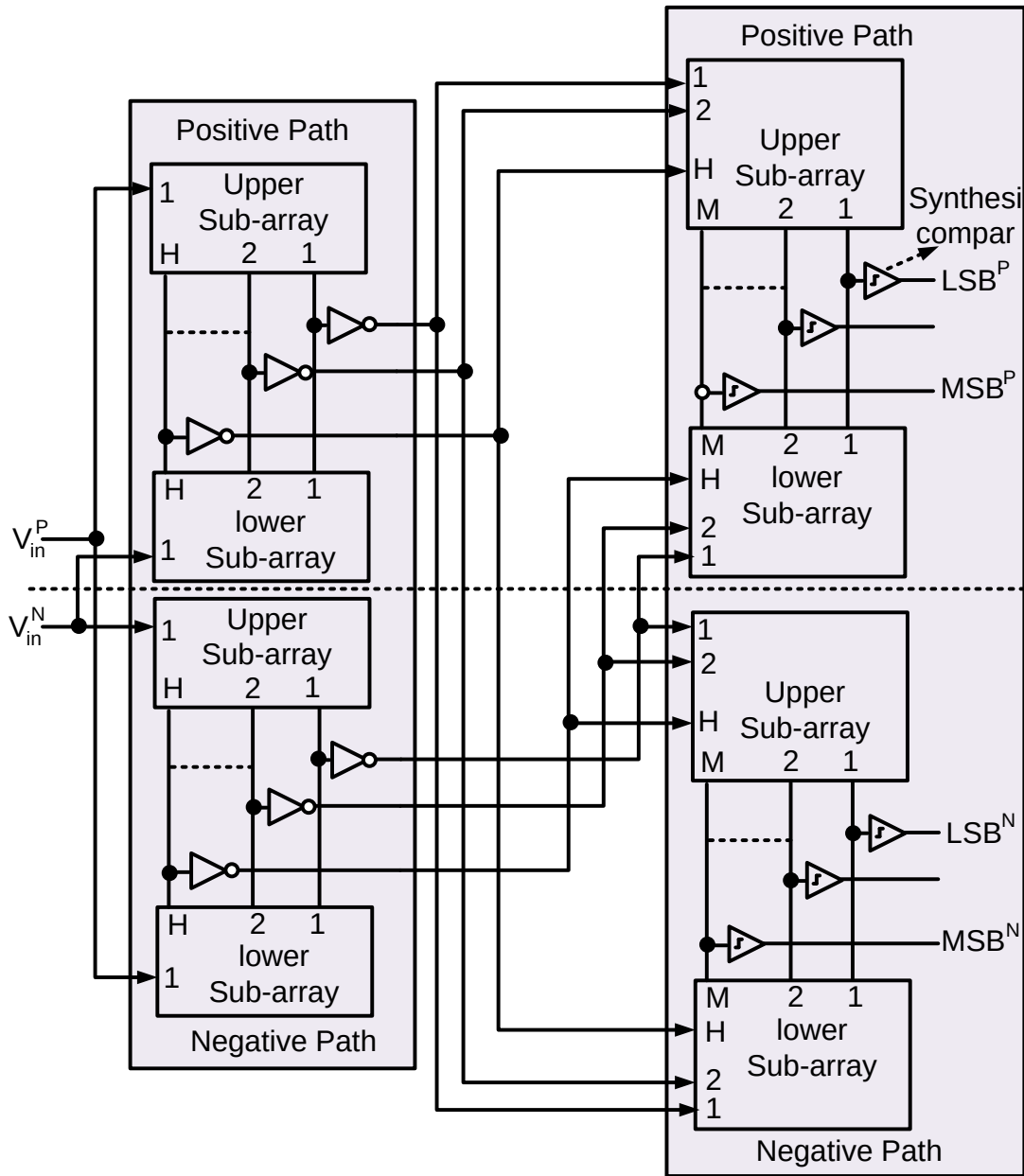


Figure 2.10: Block diagram of NeuADC [64].

Moreover, in [64], researchers introduced a novel synthesizable ADC, termed NeuADC, aiming to overcome challenges encountered in traditional ADC designs. Inspired by neural networks (NN), NeuADC is based on a deep learning framework and implemented by utilizing a mixed-signal resistive random-access memory (RRAM) crossbar architecture. Their proposed RRAM crossbar architecture facilitates mixed-signal vector-matrix multiplication (VMM) required by NeuADC in a scaling-compatible manner. Additionally, an inverter voltage transfer curve (VTC)-based activation function is used to implement the nonlinear activation function (NAF). Datasets for training, derived from the

preferred ideal quantization function, are used in the optimization algorithm. Tailored objective functions and constraints are employed to precisely represent the hardware attributes of the foundational circuits. The weights of the NN undergo iterative training through back-propagating the output errors. These weights configure different RRAM resistance values, enabling multiple signal quantization schemes on the same NeuADC hardware substrate. The operation of the hardware substrate based on the RRAM crossbar array is conceptualized as a multilayer perceptron (MLP). The NeuADC architecture, realizing a three-layer MLP, comprises distinct hardware layers—a foundational input layer, an intricate hidden layer, and an ultimate output layer as shown in Figure 2.10. Resistive random-access memory (RRAM) crossbar arrays and static CMOS inverters are employed to construct these layers, along with scalable and synthesized operational amplifiers and analog inverters within the RRAM crossbar. The output is obtained using Thevenin’s theorem applied to the RRAM crossbar arrays.

In their work [63], researchers introduced an innovative analog-to-digital converter (ADC) based on an artificial neural network (ANN). This ADC incorporates subranging and nonuniform memristors to address device mismatch issues. To counter fabrication mismatch, a trainable Memristive weight crossbar and ANN calibration (Training) is employed. The proposed ADC utilizes a level-crossing nonuniform sampling (NUS) approach, allowing it to sample whenever the input signal changes. The ADC adopts an alternative training mechanism, where synapse weights are trained separately to successively approximate the desired value. The training and working modes alternate to ensure accurate training results. The network structure consists of two layers: the first layer (coarse stage) computes the result through input and weights to obtain D_3D_2 as a coarse classification of the analog input. The second layer (fine stage) uses the output from the first stage, after the stage converter, to finely classify the input voltage and obtain D_1D_0 .

In the working mode, the ADC is controlled by a finite state machine (FSM) with two states: state 1 for determining 2nd-stage bits D_3D_2 (coarse) and state 2 for determining 1st-stage bits D_1D_0 (fine), as shown in Figure 2.11. The detailed ADC structure includes synapse weight W_j , computation neuron N_k , and feedback. The architecture comprises a composite structure with a 2T1R weight unit circuit, a converter stage with amplifiers for gain enhancement, neurons consisting of a trans-impedance amplifier (TIA) and an

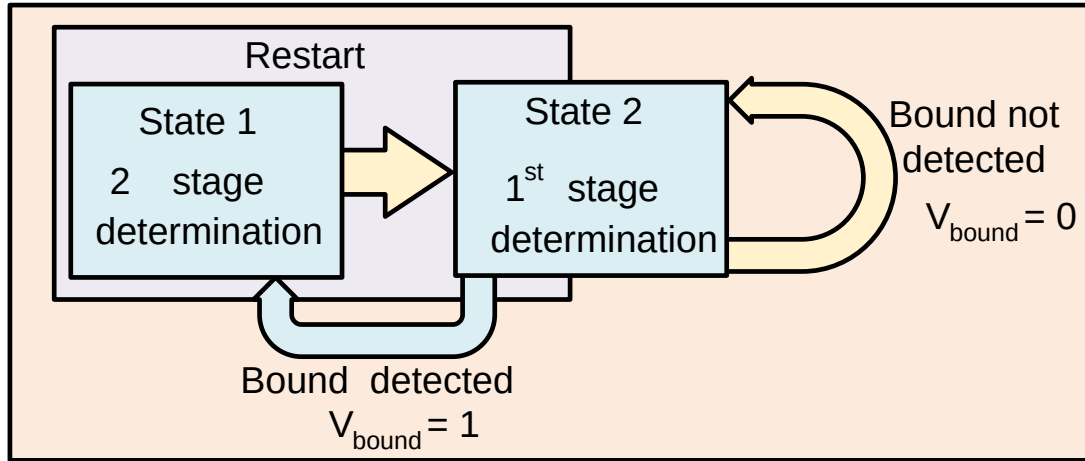


Figure 2.11: ADC Finite State Machine (FSM) with Two States per Operational Stage [63].

inverter, and a feedback circuit for control purposes.

2.5 Summary

The state-of-the-art techniques addressing sensor signal interface challenges in modern mixed-signal systems involve a range of innovative approaches aimed at improving system reliability, scalability, and adaptability. These systems face significant obstacles, including process variations, environmental stress, long-term aging, and the scaling challenges posed by modern CMOS technology. Key solutions include layout matching to reduce mismatches in critical components, automated design tools for circuit optimization, and advanced trimming methods that enable post-production adjustments to compensate for device imperfections. Dynamic calibration techniques, such as chopping and auto-zeroing, further enhance circuit stability by correcting static and dynamic deviations during operation. Evolvable hardware (EHW), a bio-inspired paradigm, has emerged as a promising approach for sensor systems, incorporating self-X properties like self-calibration, self-repair, and self-optimization. These properties allow systems to adapt dynamically, improving robustness and reducing the need for manual recalibration, particularly in autonomous and high-stakes environments. Despite these advancements, significant challenges arise in scaling analog-to-digital converters (ADCs), a critical component of sensor systems. Conventional designs for ADCs face increased difficulties as transistor sizes shrink and supply voltages decrease, making it harder to achieve the desired performance metrics. Traditional amplitude-coded ADC designs, such as flash,

delta-sigma, and hybrid architectures, focus on enhancing precision and energy efficiency. However, they often require extensive calibration, complex architectures, and significant energy overhead to address issues like comparator offsets and process variations. Advanced hybrid ADCs, such as Zoom ADCs, attempt to combine multiple architectural benefits to balance energy efficiency, resolution, and bandwidth. Nevertheless, these designs remain rooted in amplitude-coded signals, limiting their scalability and introducing additional complexity. Neuromorphic systems inspired by neural network principles offer an alternative approach, leveraging adaptive and parallel processing capabilities to tackle scaling challenges. Neuromorphic ADC designs utilize spiking neurons and other neural-inspired mechanisms, demonstrating potential for efficient signal encoding and processing. Spiking neuron-based ADCs explore encoding information through spike timing or frequency, providing novel pathways to overcome traditional design constraints. However, these systems face limitations due to their reliance on amplitude-coded signals or their dependence on large spike arrays, which can lead to elevated energy consumption and reduced practicality for real-world applications. In contrast to the state-of-the-art approaches, this thesis introduces a novel neuromorphic model of an adaptive spiking sensory front-end using time or spike-coded signals. This work moves beyond ADC-specific optimization to develop a scalable sensory interface that leverages the principles of spiking neural networks for enhanced adaptability and robustness. Unlike conventional methods, this model focuses on amplifying and level-shifting the sensor signal in the time domain, offering a fundamentally different framework for addressing the challenges of modern sensor signal interfaces while paving the way for more energy-efficient and adaptive systems.

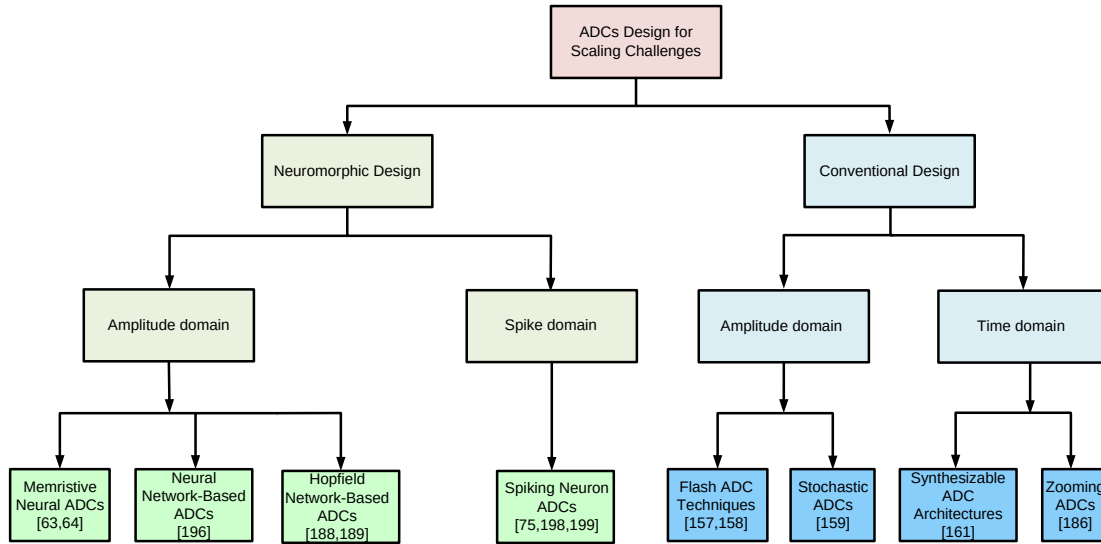


Figure 2.12: Conventional and neuromorphic design

Table 2.1: Comparisons of state-of-the-art ADC designs (Part 1).

	[198]	[159]	[161]	[75]
ADC Architecture	Neuromorphic ADC	Stochastic ADC	Synthesizable ADC	Neuromorphic ADC
Resolution (bits)	No data	11	7	8
Technology	Off-the-shelf	65 nm	40 nm	350 nm
	Components	CMOS	CMOS	CMOS
Power Supply (V)	No data	0.9	1	3.3
Power Consumption (mW)	No data	33	0.0031	No data
Area (mm^2)	No data	0.756	0.003	8.5
Sampling Frequency (MHz)	No data	100	0.0028	0.15
Nyquist Bandwidth (MHz)	No data	50	0.0014	0.075
ENOB	No data	6.2	6.4	No data
Adaptable	No	Yes	Partially	No
Domain	Spike	Amplitude	Amplitude	Spike

Table 2.2: Comparisons of state-of-the-art ADC designs (Part 2).

	[196]	[199]	[63]
ADC Architecture	Neuromorphic	Neuromorphic	Neuromorphic
	ADC	ADC	ADC
Resolution (bits)	8	No data	4
Technology	180 nm CMOS	180 nm CMOS	180 nm Memristor
Power Supply (V)	1.2	1.8	1.8
Power Consumption (mW)	0.00096	160	0.515
Area (mm^2)	0.021	2.92	3.96
Sampling Frequency (MHz)	0.045	0.75	NUS*
Nyquist Bandwidth (MHz)	0.0225	0.375	No data
ENOB	7.4	11.5	5.6
Adaptable	No	Yes	Yes
Domain	Amplitude	Spike	Amplitude

* NUS: nonuniform sampling

Table 2.3: Comparisons of state-of-the-art ADC designs (Part 3).

	[186]	[64]	[62]
ADC Architecture	Zooming	Neuromorphic	Neuromorphic
	ADC	ADC	ADC
Resolution (bits)	19	6	8
Technology	28 nm CMOS	130 nm CMOS, RRAM	Off-the-shelf Components
Power Supply (V)	0.9	1.2	No data
Power Consumption (mW)	0.475	18	7.4
Area (mm^2)	0.014	0.01	No data
Sampling Frequency (MHz)	0.02	1000	10
Nyquist Bandwidth (MHz)	0.01	500	5
ENOB	No data	5.95	7.59
Adaptable	No	Yes	Yes
Domain	Amplitude	Amplitude	Amplitude

Chapter 3

Biological Foundations of Neuromorphic Spiking System

3.1 Insights Drawn from Biological Sensory Systems

Living organisms exhibit a remarkable innate sensing capacity, attuned to both physical and chemical variables [200, 201]. Their capacity for adaptation in the face of shifting environmental conditions and the emergence of faults or lesions is equally noteworthy, with neural networks serving as the linchpin of this regulatory process. This intricate interplay of sensors and neural ensembles enables living beings to navigate and thrive in diverse and ever-changing environments, showcasing the remarkable capabilities of biological systems.

While the common trend in sensory systems typically involves the integration of signals, acoustic localization stands as an exception to this paradigm. In this unique process, living beings adeptly locate a variety of objects, from potential predators to essential resources like water or food, employing spatially separated sensor pairs [202–206]. The key to this remarkable feat lies in the utilization of interaural time differences (ITDs), reflecting the time disparities between signals received by the two ears. This temporal information is skilfully transmuted into a spatial representation within intricate neural networks, a concept originally formulated by Jeffress in 1948 [207]. This phenomenon underscores the ingenious adaptability of living organisms in response to their surroundings, emphasizing the fascinating intricacies of biological sensory mechanisms.

Jeffress’ seminal theory, expounded in 1948, is grounded in a trio of fundamental

postulates elucidated by Ashida and Carr [202]. These foundational tenets comprise an organized arrangement of ascending nerve fibers functioning as delay lines within conduction pathways, a complex assembly of coincidence detectors adept at transmuting synchronized inputs into discernible output spike rates, and the culminating creation of a neuronal place map within the cell array, achieved through deliberate modulations in spiking rates. Jeffress' theory thus serves as an intellectual cornerstone, shedding light on the intricate mechanisms underpinning auditory perception and localization, ultimately providing valuable insights into the neural intricacies of sensory systems.

3.2 Biological Neuron Model

While Neuromorphic Computing has yet to reach the pinnacle of mainstream adoption, a growing awareness of its inherent advantages is steadily permeating the technological landscape. The aspiration of harnessing the power of parallel computing, facilitated by the utilization of adaptive modular silicon neurons imbued with remarkable pattern recognition capabilities, has remained a focal point in research for over three decades. Numerous compelling motivations drive the modelling of neurons in silicon, a few of which include:

1. The inherent inefficiency of software-based neural models when executed on von Neumann systems [208, 209].
2. The quest for parallel computing is aided by the utilization of noisy neurons [210, 211].
3. An unwavering pursuit of comprehending the intricacies of the human brain, with the dual objectives of emulation and the quest for curative solutions to neurological ailments [212, 213].
4. The desire to establish interfaces with biological neurons, bridging the realms of silicon and biology [214, 215].
5. The progressive transition from traditional analog systems to neural modules [216].
6. The ambition to develop autonomous robots endowed with the capacity to learn in a manner reminiscent of human children [217].

Various biological neuron models exhibit a spectrum of distinct properties, and their exploration yields valuable insights. In a seminal work [218], researchers delve into the intricate neuro-computational characteristics inherent in actual neurons and their pivotal role in temporal coding and spike-timing information processing. Additionally, they embark on a comprehensive comparison of several extensively utilized spiking neuron models. Their exploration commences with the rudimentary integrate-and-fire model dating back to 1907 [219] and culminates with the intricate yet resource-intensive Hodgkin-Huxley model [220]. Along this trajectory, they meticulously scrutinize diverse spiking neuron models and assess their merit based on two crucial criteria: 1) their ability to faithfully replicate neuro-computational attributes, and 2) their implementation efficiency, gauged by the computational workload, encompassing floating-point operations such as addition and multiplication, essential for simulating each model. This systematic evaluation sheds light on the intricate landscape of neuron models and their practical feasibility.

3.3 Synapse

As this section unfolds, the narrative navigates the cutting edge of technological innovation, where memristors come to the fore as a catalyst for transforming computing systems. With the limitations of Moore's law looming, numerous sources have pointed to memristors as the key to ushering in a new era of computational potential [221, 222]. This transformation is not confined to the realm of conventional computing; it extends its influence into the field of biologically inspired systems. Particularly in the context of contemporary cognitive integrated sensor systems and the demand for low-power intelligent solutions, memristors are emerging as a linchpin for progress [222–224].

The spiking neural network (SNN) architecture, empowered by memristors, emerges as a focal point in this transformative journey. These memristor-based SNNs are characterized by their resilience to noise, adaptability to various technologies, minimal on-chip space requirements, scalability, energy efficiency, proficiency in machine learning, and inherent self-regulating properties. These attributes position memristor-based SNNs as pivotal elements in shaping the landscapes of Industry 4.0 and the Internet of Things (IoT), as corroborated by numerous references [225–229]. However, a closer look reveals

that adaptive synapses are the cornerstone of the SNN framework, acting as the vital cogs in this sophisticated computational engine.

Numerous researchers have directed their efforts toward the design of neuromorphic systems, aiming to replicate the functionalities of biological neural networks [230–235]. Notably, recent focus has shifted towards harnessing the capabilities of memristors to replicate synaptic functions [236,237]. Biological synapses exhibit two forms of synaptic plasticity: short-term plasticity (STP) and long-term plasticity (LTP) [238,239]. In various studies [240–245], researchers have successfully created memristors that faithfully emulate the characteristics of STP and LTP in synapses.

The implementation of a spiking neural network (SNN) utilizing memristors as synapses, drawing inspiration from biological neural network sensors, presents a set of formidable challenges. These include concerns regarding resistance level stability, the intricate fabrication of memristor systems, compatibility with CMOS technology, the finite range of resistance levels, as well as issues related to the reliability and lifespan of memristor devices [226,246]. These challenges pose obstacles to their near-term integration into commercial chips, primarily due to numerous unresolved issues demanding investigation, as evidenced by [226,246]. Consequently, many researchers have turned their attention towards developing memristor emulators for the realization of neuromorphic architectures on contemporary microchips [247–259].

State-of-the-art designs face challenges when attempting to incorporate on-chip memristors. These challenges stem from the inherent complexity of the circuits, necessitating external devices for support. These designs often employ a multitude of active components and passive elements [247–259]. Furthermore, some of these designs adopt grounded structures [251–254,258], while others opt for floating structures [255–257,259]. It's important to note that designing a circuit with floating memristors proves more intricate compared to a grounded memristor circuit. However, the grounded memristor design has its limitations, restricting its range of applications.

In a previous study [254], a grounded memristor was introduced, incorporating a complex arrangement of components including two operational amplifiers, ten transistors, two resistors, a capacitor, and a multiplier. Similarly, another study [251] presented a grounded memristor emulator circuit leveraging a current backward transconductance amplifier (CBTA), a multiplier, two resistors, and a single capacitor. Furthermore, an

alternative grounded memristor emulator design was proposed in [252], featuring a configuration involving four transistors. In a separate endeavor [253], another grounded memristor emulator was introduced, utilizing a setup with four transistors. Another study [258] contributed yet another grounded memristor emulator employing seven transistors and a single capacitor. Diverging from grounded designs, a floating memristor emulator circuit was outlined in [256], which adopted three operational transconductance amplifiers (OTA), four second-generation current conveyors (CCII), six resistors, and a single capacitor. Furthermore, in a separate study [257], a floating memristor design was presented, consisting of only three transistors, an external capacitor, and a current source. Additionally, another research effort [259] unveiled a floating memristor emulator circuit, employing a current backward transconductance amplifier (CBTA) in conjunction with two capacitors. In yet another approach, a different study [255] introduced a floating memristor emulator circuit, relying on a composition of four second-generation current conveyors (CCII) and a single multiplier.

3.4 Sensor-to-Spike Concepts

Sensor-to-spike encoding is a cornerstone of neuromorphic engineering, enabling biological plausibility and energy-efficient signal processing. This section reviews established and emerging methods for converting analog sensor signals into spike trains.

A CMOS image sensor, as described in [260], utilizes spiking pixels with pixel-level analog-to-digital conversion (ADC) for high dynamic range (HDR) and linear light-intensity transduction. The spiking pixels encode light intensity into pulse rates (rate coding), where the pulse frequency is proportional to irradiance. This spike-based transduction aligns with neuromorphic computing paradigms, enabling direct interfacing with systems processing temporal spike codes. The pixel-level ADC employs digital counters to convert these spike trains into digital values, allowing adjustable resolution by varying counting intervals, thereby trading precision for frame rate. This dual capability neuromorphic-compatible spike output and conventional digital output—bridges sensory data processing between bio-inspired and traditional computing systems. Key innovations include a self-resetting pixel design with a light-controlled oscillator, integrating a photodiode and a Schmitt trigger to generate spikes.

Table 3.1: Comparison of state-of-the-art memristor circuits..

Reference	Active component	Passive device	Frequency	Memristors type
[254]	2 OP-AMPs, 1 Multiplier, 10 Transistors	2 R, 1 C	800 Hz	Grounded Memristor
[251]	CBTA, 1 Multiplier	2 R, 1 C	100 kHz	Grounded Memristor
[252]	4 transistors	-	100 MHz	Grounded Memristor
[253]	4 transistors	-	100 kHz	Grounded Memristor
[258]	7 transistors	1 C	50 MHz	Grounded Memristor
[256]	3 OTA, 4 CCII	6 R, 1 C	10 kHz	Floating Memristor
[247]	1 MO-OTA, 1 Multiplier	1 R, 1 C	1 kHz	Floating Memristor
[257]	3 transistors	1 C	1 MHz	Floating Memristor
[259]	1 CBTA	2 C	1 MHz	Floating Memristor
[255]	4 CCII, 1 Multiplier	5 R, 1 C	20.2 kHz	Floating Memristor

The vision sensor presented in reference [261] employs an architecture where each pixel independently and continuously quantizes local relative intensity changes to generate spike events. This design asynchronously encodes temporal contrast rather than static illumination. Each pixel detects relative intensity changes over time, generating digital spike events only when significant variations occur, thereby eliminating redundant data transmission inherent in frame-based systems. The pixel architecture integrates a logarithmic photoreceptor to compress light intensity over a wide dynamic range (120 dB), enabling operation under uncontrolled illumination conditions from dim moonlight to bright sunlight. When thresholds are crossed, comparators produce ON/OFF events.

Chapter 4

Neuromorphic Spiking Sensory System

The growing demand for sensor systems in IoT and Industry 4.0, specifically those capable of dynamic and resource-efficient performance, has become increasingly apparent. Traditional amplitude-based sensors present limitations that need addressing. This research’s objective is to develop a novel neuromorphic spiking sensory system with self-X capabilities, which is imperative to meet the requirements of the modern era. This system offers several key advantages, including efficient low-voltage operation, robustness in noisy environments, and minimal power consumption, addressing the challenges associated with technology scaling. By providing a high level of adaptability, this neuromorphic spiking sensory system excels in dynamic settings, making it a choice for applications in IoT and Industry 4.0, which demand seamless performance in ever-changing conditions. Notably, the neuromorphic spiking sensory system is engineered to communicate information through spike timing, making it a candidate for integration into advanced electronic sensory systems.

The architectural blueprint and design principles of neuromorphic systems are firmly rooted in their aspiration to emulate the intricate structures of the biological nervous system. In this context, delay lines within acoustic localization represent a clear model of adaptive SNN architecture, as illustrated in Figure 4.1a. However, it’s important to note that the primary objective here is not an exact replication of acoustic localization mechanisms, but rather the inventive adaptation of these principles into a pioneering neuromorphic spiking sensory system. This adaptation extends beyond the original

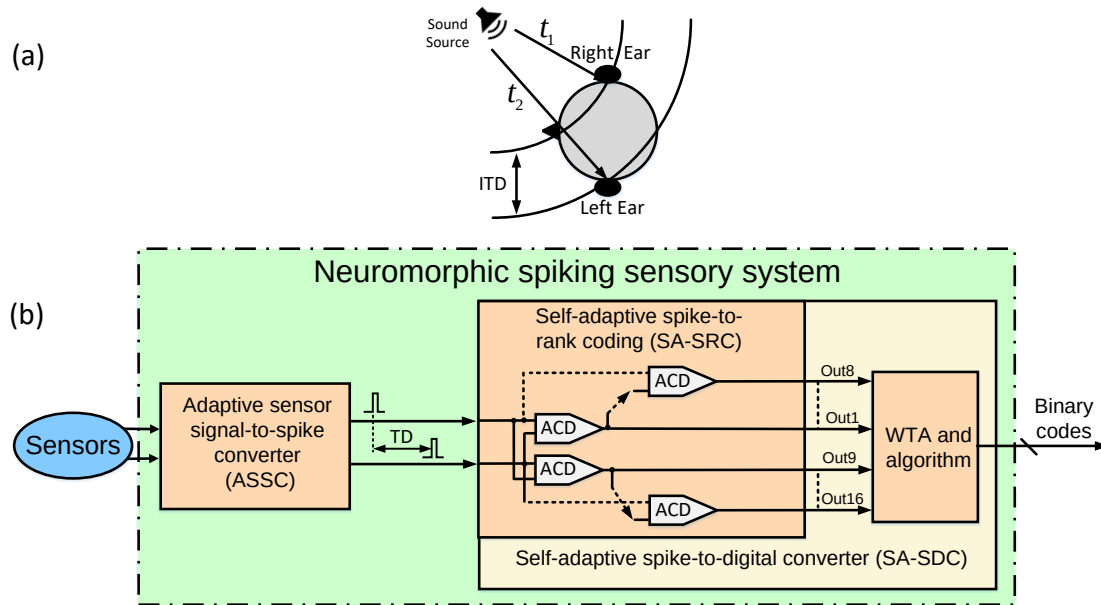


Figure 4.1: (a) Sound localization process: The brain identifies the origin of a sound by evaluating the interaural time difference (ITD) between signals detected by each ear, where t_2 represents the time the sound reaches the left ear and t_1 the right ear. (b) Structural overview of the proposed neuromorphic spiking sensory system: The adaptive signal-to-spike converter (ASSC) transforms the input sensor signal into two distinct spikes, separated in time based on the sensor's input. The self-adaptive spike-to-digital converter (SA-SDC) generates a digital output by analyzing the temporal gap between the spikes. The SA-SDC integrates two key modules: adaptive coincidence detection (ACD) and a winner-take-all (WTA) mechanism with embedded memory.

context and ventures into novel application domains.

In prior work, documented in references [262–265], a notion of employing spike timing mechanisms to tailor the concept of acoustic localization for a neuromorphic spiking sensory system was introduced. Figure 4.1a provides a visual representation of a unique SNN model explicitly engineered for acoustic localization, while Figure 4.1b introduces a sophisticated neuromorphic spiking sensory system that amalgamates adaptive features within a two-stage framework, effectively mirroring the foundational model articulated by Jeffress [207]. It is pivotal to reiterate that the primary objective transcends the mere augmentation of acoustic localization; instead, in this thesis, the aim is to adapt and apply this concept to usher in a paradigm shift in the realm of neuromorphic spiking sensory systems.

In the initial phase of this process, the sensor signal undergoes a transformation via the adaptive sensor signal-to-spike converter (ASSC), resulting in the generation of a pair of spikes. These spikes exhibit time differences (TD) that vary in response to the

incoming sensor signal. In Figure 4.1b, the second component is encountered, denoted as the self-adaptive spike-to-digital converter (SA-SDC), which draws inspiration from Jeffress' theoretical framework established in 1948. This framework is underpinned by three core assumptions. The first assumption finds expression through the synaptic weights, while the second is executed through an array of adaptive coincidence detectors (ACD). These specialized detectors are responsible for converting the time differences (TDs) inherent in the dual input pulses into a ranked spike code. The third and final assumption comes to fruition through the employment of winner-take-all (WTA) mechanisms and algorithms, transmogrifying the ranked spike code into a digital representation.

4.1 Neuron model

In this thesis, scrutiny delves into the essential prerequisites for the effective realization of the proposed design. This implementation mirrors the dynamics of a neural network time delay, where the duration between the initial spike and the incoming charge's magnitude exhibits an inversely proportional relationship. These specific attributes constitute fundamental elements present in all spiking neuron models. To conform to the specific requirements of this study, while minimizing the complexity introduced by adaptation variables and transistors, a series of adjustments and the removal of redundant components from the LIF neuron model originally presented by Indiveri in 2003 [266] were initiated. Indiveri's LIF analog neuron model, meticulously crafted to emulate the intricate workings of biological neurons, encompasses an extensive array of elements. These include provisions for configuring a customizable refractory period, the regulation of spike frequency adaptation, the modulation of the neuron's threshold voltage, the introduction of positive feedback, the incorporation of a membrane capacitor, the integration of a transistor to address current leakage, and the inclusion of a digital inverter for pulse generation. While this neuron circuit exhibits remarkable flexibility in its architecture, its core focus remains on emulating the behaviours of biological neurons. Consequently, this design direction results in an augmented presence of adaptation variables and an elevated transistor count.

In the Indiveri model, the component responsible for regulating the neuron's threshold voltage is designed to manage this critical parameter. Conversely, the CMOS tran-

sistors (M3 and M4) efficiently fulfil this role for the specific objectives of this thesis. Consequently, to streamline the design and minimize the number of adaptation variables and transistors, this component has been eliminated. Additionally, the spike frequency adaptation feature, which typically governs spike frequency in response to continuous inputs or identical signals, is redundant for the goals of this thesis. The primary focus in this thesis revolves around the essential attributes necessary for the proposed coincidence detection to function as a neural network time delay, featuring an inversely proportional relationship between incoming charge magnitude and the time to the initial spike. Therefore, this element is also omitted to reduce adaptation variables and transistors, aligning the design with the specific objectives in this thesis.

The incorporation of positive feedback in the circuit accelerates the membrane's potential and expedites the neuron's threshold attainment. While this rapid switching of the inverter (M3 and M4) effectively minimizes power dissipation, it runs contrary to the specific objectives of this work. In this thesis, the focus centers on maintaining an inverse relationship between the incoming charge's magnitude and the time required for the first spike to occur. Hence, to align with these objectives, the positive feedback element is similarly excluded from the design.

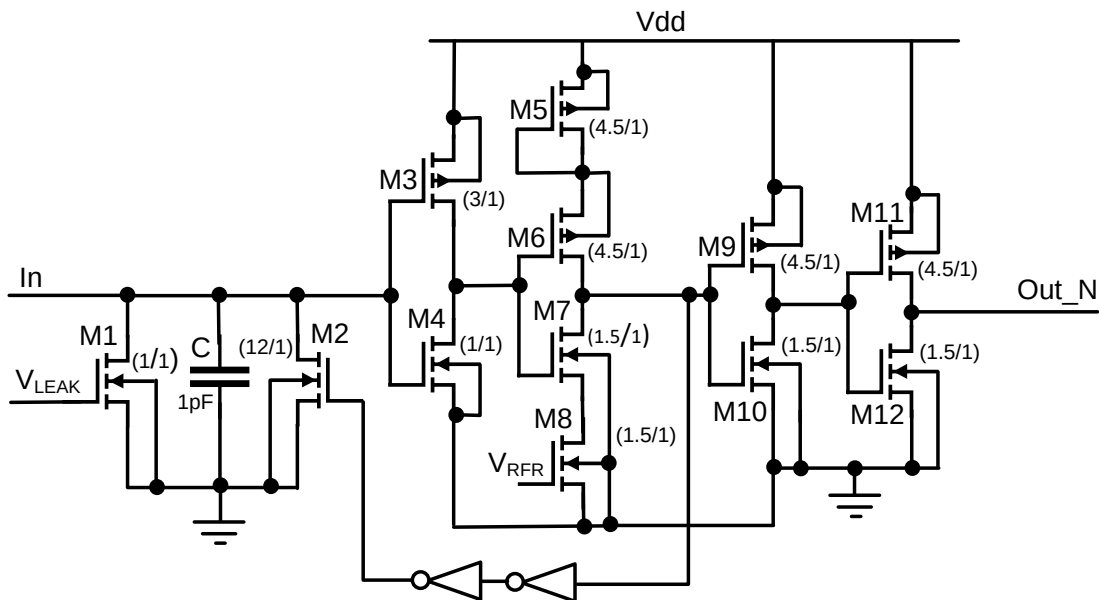


Figure 4.2: The analog leaky integrate-and-fire (LIF) neuron circuit is optimized to meet the functional needs of the ASSC and SA-SDC modules. Designed with transistor dimensions in micrometers, it is a simplified variation of Indiveri's neuron model, customized for this specific application.

In this thesis, the proposed neuron circuit exhibits a streamlined design with 16

transistors and two variables, a significant reduction compared to the Indiveri model's 20 transistors and four variables [263]. This simplification of the neuron's adaptation process, now utilizing only two variables, delivers several advantages over the Indiveri model. It results in an impressive eightfold speed gain, a 20% reduction in power consumption, a 30% decrease in the overall circuit area, and an eightfold spike rate increase when compared to the Indiveri model. The modified circuit model, as depicted in Figure 4.2, incorporates several crucial components. The charging of the membrane capacitor (C) is achieved through the incoming synaptic current. Upon reaching a voltage exceeding the inverter (M3 and M4) transistor's threshold, it triggers a secondary inverter (M6 and M7). The V_{RFR} , serving as a vital control element, governs both the pulse width of the neuron's output and the inverter (M6 and M7) responsible for generating the output and discharging the capacitor. Simultaneously, M1 facilitates the gradual leakage of the capacitor, controlled by the V_{LEAK} parameter. Notably, the sizing of transistors plays a pivotal role in the Self-Adaptive Spike-to-Rank Coding (SA-SRC) design, tailored to ensure accurate functionality across various process, voltage, and temperature (PVT) conditions. The specific transistor sizes are visually presented in Figure 4.2.

4.2 Synapse

In this thesis [262], an adaptive synapse is introduced that leverages CMOS memristor technology, enabling on-chip integration without the need for external components, as illustrated in Figure 4.3. This synapse effectively emulates the Short-Term Plasticity (STP) and Long-Term Plasticity (LTP) observed in biological synapses. Within this design, transistors M1 to M4 serve to replicate STP characteristics, while M5 to M12 transistors capture the essence of LTP. Notably, M4 works as a capacitor by connecting the source, drain, and bulk terminals to the ground, with its voltage control managed by the feedback circuit involving M2 and M3 transistors. Additionally, an 8-bit up-down counter, realized using eight JK flip-flops, is employed to govern alterations in the LTP properties of the synapse.

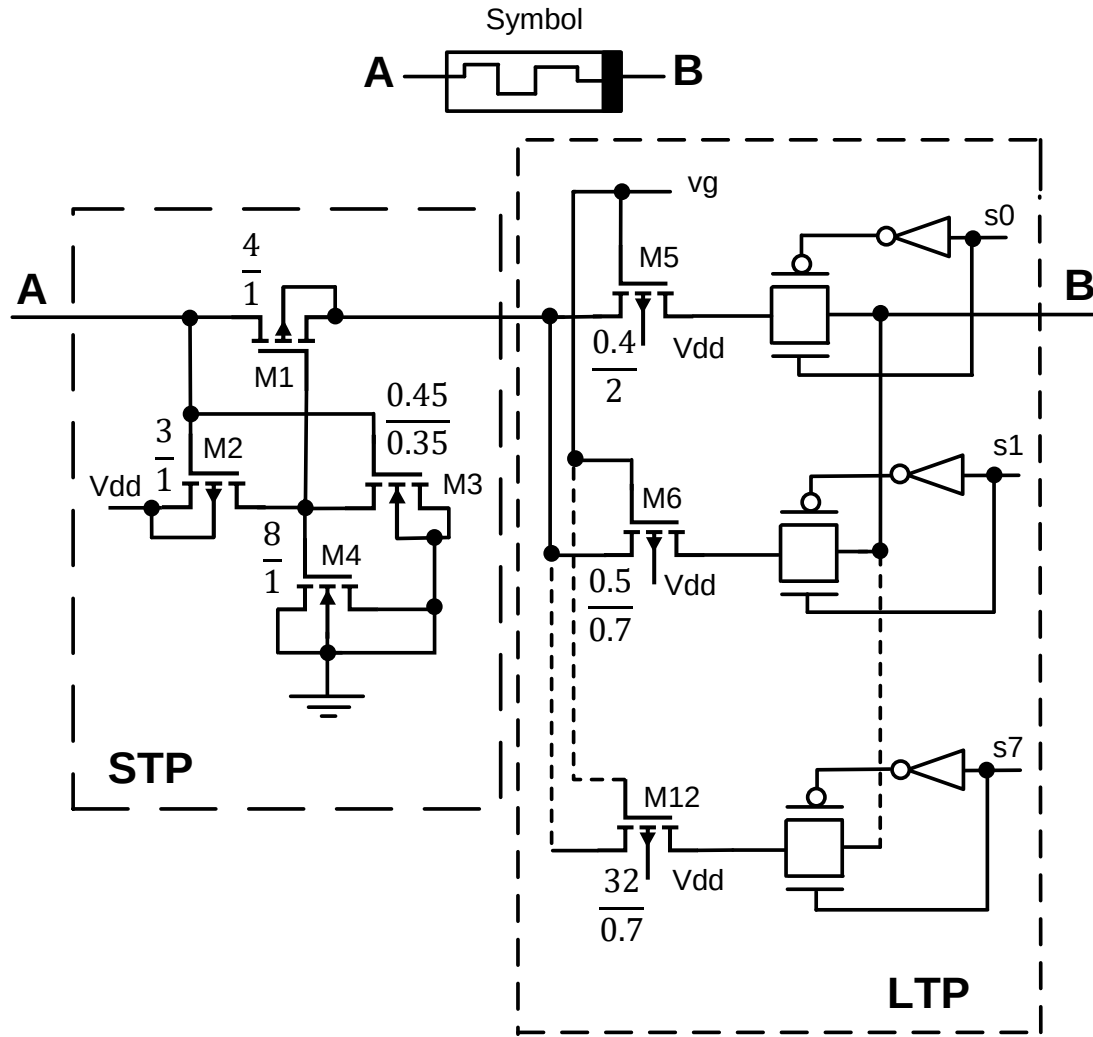


Figure 4.3: Schematic of the synapse for the ASSC and ACD units. The CMOS-based memristor replicates the synaptic plasticity observed in biological systems, encompassing long-term (LTP) and short-term (STP) adaptability. This circuit represents the proposed architecture’s adaptive synapse (AS), utilizing transistors sized in micrometers.

4.3 Adaptive Sensor Signal-to-Spike Converter (ASSC)

Achieving alignment between the spans of the sensor and SA-SDC is critical for performance, as illustrated in Figure 4.4. In cases where the sensor span is smaller Figure 4.4a, the SA-SDC’s dynamic range may be underutilized, necessitating careful management of available ACDs. On the other hand, when the sensor’s span exceeds the SA-SDC input range Figure 4.4c, there’s a risk of losing valuable sensor data. Scenarios with equal spans but offset Figure 4.4b or variations in duration and offset Figure 4.4d require precise alignment using time domain techniques such as level shifting and amplification.

The lack of alignment between sensor and SA-SDC spans can lead to challenges,

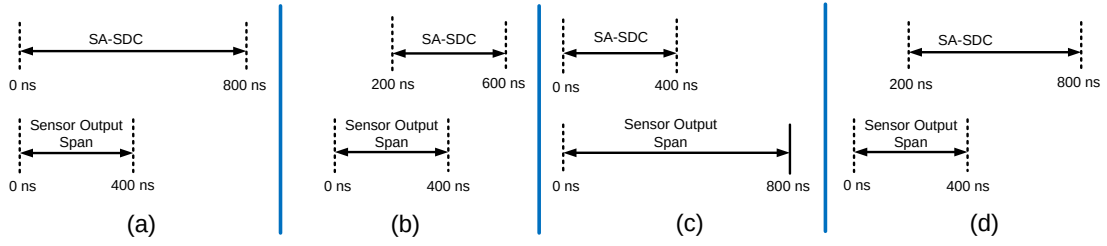


Figure 4.4: Corrections are necessary in the following cases: (a) The sensor's range falls short of the SA-SDC's input capacity. (b) Another situation arises when the sensor and SA-SDC have similar operating ranges, but a noticeable offset or misalignment exists that requires adjustment. (c) The sensor's range exceeds the input capacity of the SA-SDC. (d) The sensor and SA-SDC have differing ranges and exhibit a positional misalignment.

prompting the need for strategic solutions. In this context, the ASSC emerges as a versatile conditioning circuit, playing a pivotal role in ensuring span equality without resorting to additional level shifting. Notably, the ASSC showcases the ability to simultaneously amplify, and level shift the sensor signal in the time domain. This multifaceted functionality positions the ASSC as a comprehensive solution, addressing the complexities of span misalignment and contributing to the achievement of system performance.

The designed ASSC introduces a dual-component structure, incorporating two synapses and two neurons, as visually depicted in Figure 4.5. Interconnecting the synapse inputs, the output of each synapse is intricately linked to an individual neuron. Furthermore, each neuron establishes a connection with a dedicated switch, creating a linkage between these switches and the V1 and V2 inputs, respectively. This configuration emphasizes the interdependence and coordination between the synapses, neurons, and input switches, forming a cohesive and purposeful architecture. Figure 4.3 and Figure 4.2 illustrate the schematics of the devised adaptive synapse and neuron, offering comprehensive insights into their respective configurations and interconnections.

The ASSC executes a two-phase operation. Initially, switches SW1 and SW2 are activated, initiating the charging of the membrane capacitors within the neurons up to voltages V1 and V2, respectively. In the subsequent phase, these switches are disengaged, and a timed pulse is applied to the synapses, concluding the integration of membrane capacitors. This pulse propels the neurons toward the activation threshold, instigating the generation of spikes. It's essential to emphasize that the temporal gap between these neuronal spikes is dictated by the voltage difference between V1 and V2.

Traditional signal conditioning systems typically integrate instrumentation amplifiers

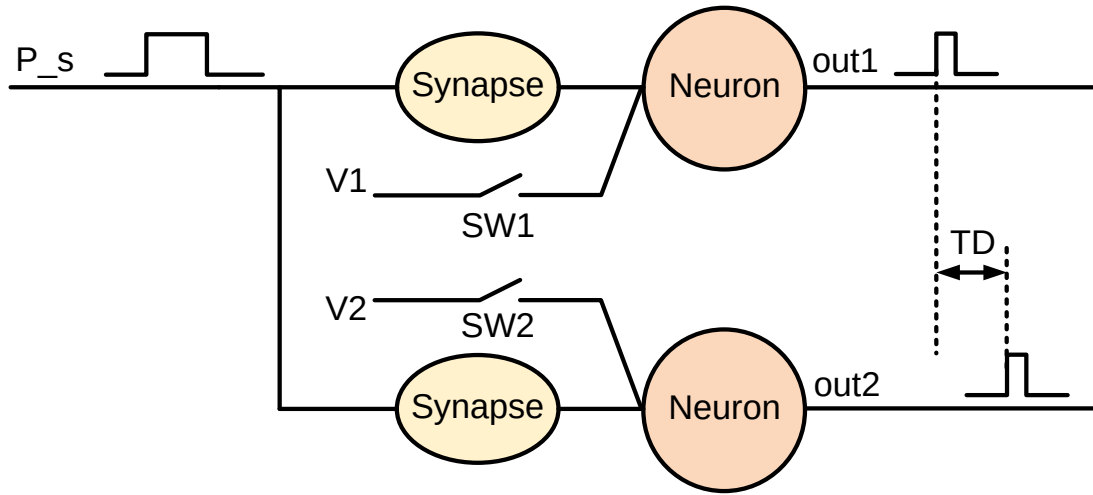


Figure 4.5: Schematic of the suggested adaptive sensor signal-to-spike converter (ASSC). The ASSC comprises two components: two synapses and two neurons. The synapses share interconnected inputs, with their outputs routed to corresponding neurons. Each neuron is further connected to a dedicated switch, which interfaces with the V1 and V2 inputs.

as signal-processing components, relying on amplitude coding and exhibiting vulnerability to swift technological progress. In contrast, neuromorphic spiking sensory system adopts a novel approach, performing amplification in the time domain. The ASSC determines gain through the following equation:

$$\text{ASSC Gain} = \frac{\text{ASSC Output Span at Weight A}}{\text{ASSC Output Span at Weight B}} \quad (4.1)$$

The regulation of synaptic weights involves the modulation of both their V_{gs} values and the corresponding adjustments to their up counters. Weight A represents a customizable weight configured to attain the desired gain, while weight B signifies the synapse weight when V_{gs} values are set to zero, and the up counters reach a value of 255. To accommodate the two synapses, two up counters, namely V_{gs1} and V_{gs2} , are employed in this process. The offset represents the disparity between the sensor span and the SA-SDC input span, causing a transition from the SA-SDC's "first code" digital output to the subsequent code increment. This offset is quantified in the least significant bit (LSB) and can be computed using the following equation:

$$\text{Offset} = \frac{\text{TDS}}{\text{LSB}} \quad (4.2)$$

The Time Difference Span (TDS), representing the temporal gap between the sensor

span and the SA-SDC input span, allows for gain and offset modulation by adjusting synaptic weights. The quantifiable bit capacity, labelled as NoB (Number of Bits), achievable through SA-SDC, relies on the time span of the ASSC, extendable through gain application. The calculation of the Maximum Number of Bits (MNoB), the maximum achievable bit capacity by ASSC, is determined by the following equation:

$$\text{MNoB}_{\text{ASSC}} = Id(\text{MNoL}_{\text{ASSC}}) \quad (4.3)$$

The total number of ASSC levels ($\text{MNoL}_{\text{ASSC}}$) is determined using this formula:

$$\text{MNoL}_{\text{ASSC}} = \frac{\text{Time Span of the ASSC}}{\text{LSB}} \quad (4.4)$$

4.4 Self-Adaptive Spike-to-Digital Converter (SA-SDC)

The SA-SDC design incorporates two fundamental components: the Self-Adaptive Spike-to-Rank Coding (SA-SRC) and the Winner-Take-All (WTA) mechanism and algorithm, illustrated in Figure 4.1b. The SA-SRC plays a crucial role in generating spike orders that reflect the temporal differences between two spikes received at their inputs. These spike order codes, integral to a coding approach, depend on the precise sequential arrangement of spikes within a neuron cluster. This arrangement is directly shaped by the firing sequence of neurons, as highlighted in previous studies [267, 268].

In the current developmental phase, the SA-SRC employs sixteen adaptive coincidence detection (ACD) units, as illustrated in Figure 4.6. The SA-SRC architecture features two symmetric sections upper and lower yielding SA-SRC outputs labeled as Out1 to Out8 and Out9 to Out16, respectively. This design facilitates the accommodation of both single-ended and differential sensory inputs. The SA-SRC configuration involves two distinct inputs, in1 and in2. In the upper segment, in1 is directly routed to the first input of ACDs, while in2 traverses the ACDs sequentially, forming delay chains in the upper segment. Conversely, in the lower segment, in2 is directly connected to the primary ACD input, with in1 undergoing sequential processing through the ACDs, forming delay chains specific to the lower segment. The temporal extent of the delay chain unit is influenced by the neuron's firing time, modulated by incoming current, and adapted by synapse weights to accommodate timing variations within each chain

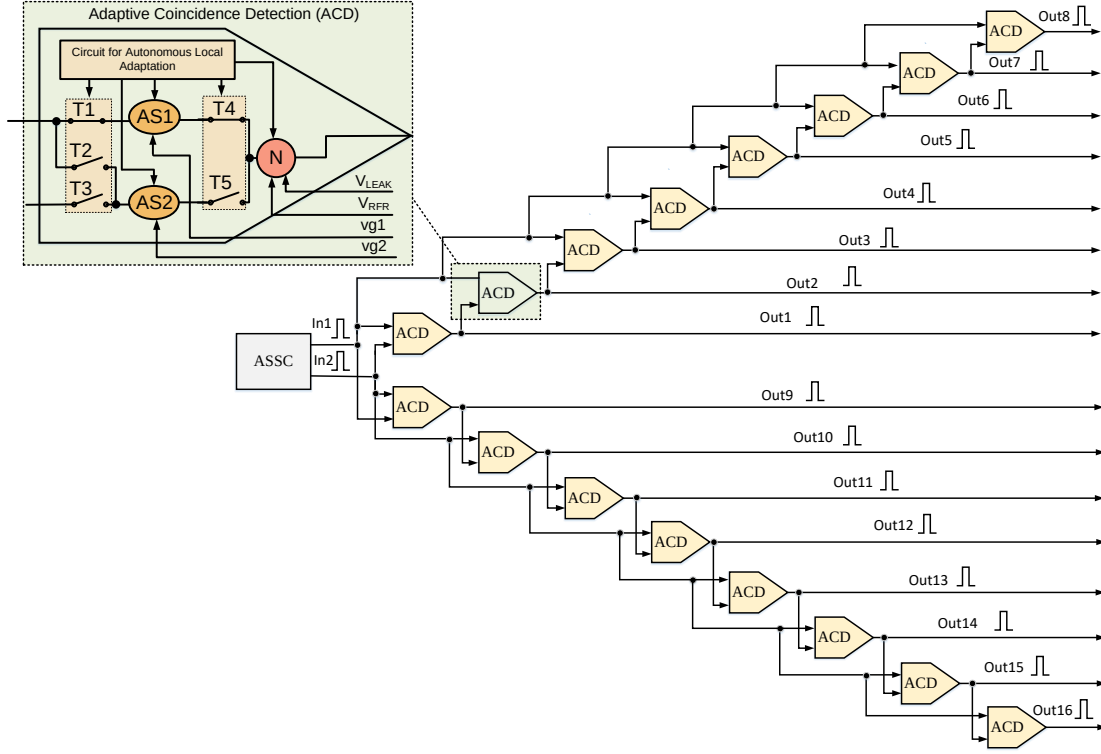


Figure 4.6: The proposed Self-Adaptive Spike-to-Rank Coding (SA-SRC) method introduces a novel approach to neural coding. Its core feature is the Adaptive Coincidence Detection (ACD) module. The SA-SRC integrates 16 ACD units, each consisting of two adjustable synapses (ASs) and a neuron (N). This system generates spike outputs that encode rank information based on the temporal difference between input spikes. The SA-SRC leverages self-ability mechanisms through a dual-layer adaptive structure. The autonomous ACD system powers the first layer, while the second layer employs V_{LEAK} and V_{RFR} for neural modulation, along with $vg1$ and $vg2$ for managing synaptic dynamics.

unit. The Figure 4.7 shows the achievable delay range versus the output counter for different V_g values. The core element within the SA-SRC architecture is the Adaptive Coincidence Detector (ACD), implemented by integrating a single neuron (N) and two adjustable synapses (AS), as illustrated in Figure 4.6. Schematic representations of the neuron and synapse can be found in Figure 4.2 and Figure 4.3, respectively.

The SA-SRC functions in two primary modes. The first mode, the normal operational mode, establishes a connection between both synapses of the ACD and the neuron. The second mode, known as the adaptation mode and introduced in a previous study [263], employs a two-layer adaptation hierarchy. In this hierarchical structure, the initial layer operates at the ACD level and the subsequent layer functions at the SA-SRC level. The first layer exhibits full self-adaptation and operates in a localized manner, functioning autonomously without external supervision, and exists in two distinct states. During the

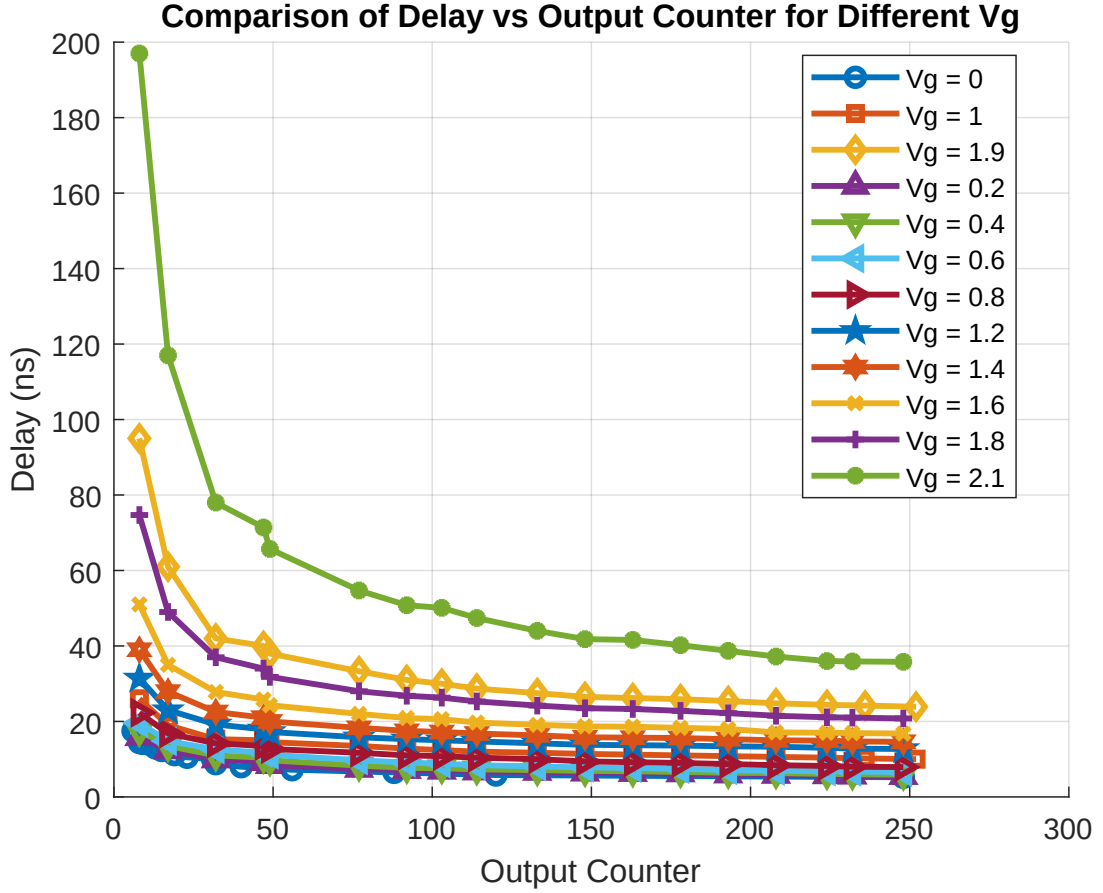


Figure 4.7: Achievable delay range versus the output counter for different V_g

adaptation mode, the SA-SRC undergoes two distinct states for adjusting the synapse weights. In the first state, exclusively the first synapse is connected to the neuron to adapt its weight, as illustrated in Figure 4.8. Subsequently, the second state involves the exclusive connection of the second synapse to the neuron to adapt its weight, as depicted in Figure 4.8. The transmission gate (T8) facilitates the connection of in1 to in2 during the adaptation mode, utilizing in1 for synapse weight adaptation. In the first state, all ACDs' first synapses are connected in parallel to in1, adapting their weights simultaneously. Similarly, in the second state, the second synapses of all ACDs are connected in parallel to in1 for simultaneous weight adaptation. Upon completion of the adaptation process, T8 is deactivated, as shown in Figure 4.8. In the initial layer of the adaptation process, the calculation of a synapse's weight hinges on the exact timing of neuron firing, a timing intricately linked to the magnitude of the received input current. This methodology operates under the assumption that the timing of neuron firing is directly affected by the input current, where the synapse weight serves as a regulatory

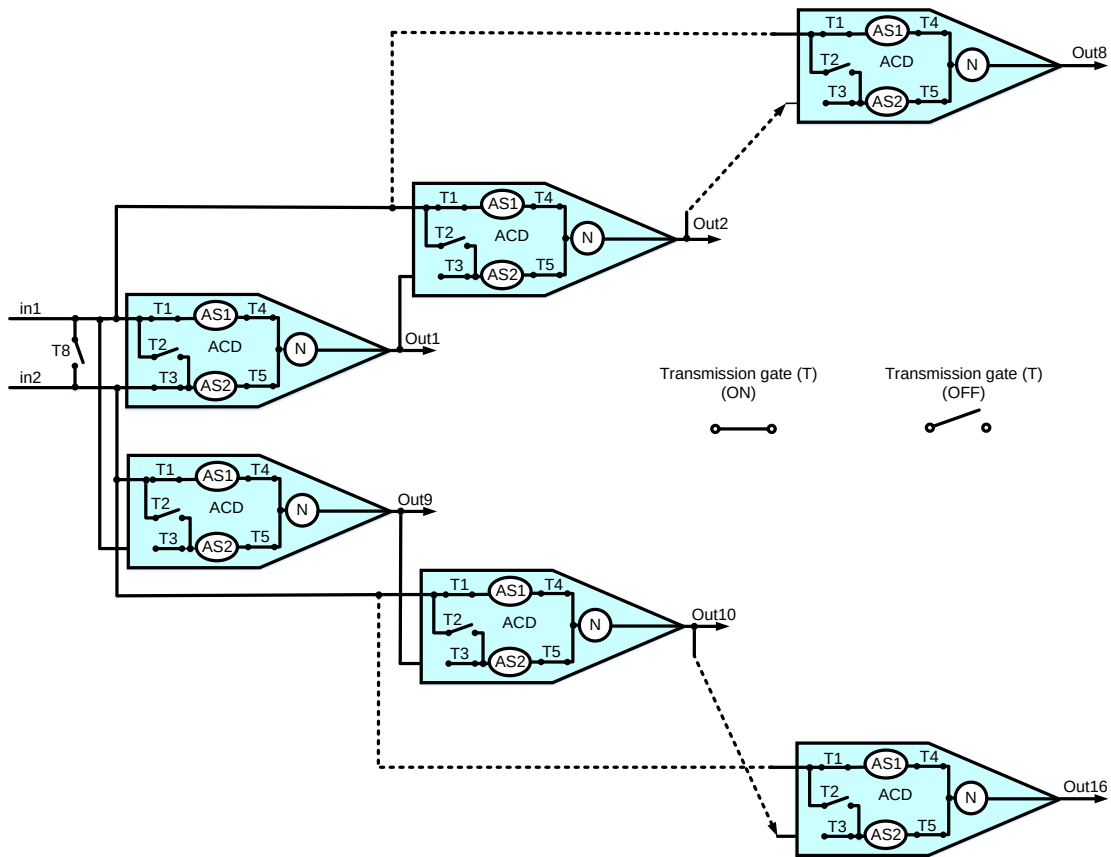


Figure 4.8: This illustration depicts the two modes of operation in the ASRC: normal and adaptive. In normal mode, both synapses within the ACD are linked to the neuron. During this mode, transmission gates T1, T3, T4, and T5 are on, while T2 and T8 remain off. The adaptive mode operates in two distinct states. In the first state, only the first synapse connects to the neuron, with T1, T4, and T8 on, and T2, T3, and T5 off. In the second state, the second synapse alone connects to the neuron, on T2, T5, and T8, while T1, T3, and T4 are off.

factor for this current. Consequently, a direct correlation is established between the synaptic weight and the timing of neuronal firing.

Two pulses, namely the P_d pulse and the in1 pulse, assess the timing of neuron firing before and after the rising edge of the neuron pulse. The left output of the first AND gate in Figure 4.9 should register as 0 if the neuron's output remains unchanged, as illustrated in Figure 4.10. Conversely, the right output of the second AND gate, also depicted in Figure 4.9, should be 1 if there is no rightward shift in the neuron's output, as shown in Figure 4.10. D flip-flops DFF1 and DFF2 store the outputs of the first and second AND gates, capturing the left and right shifts, respectively. Simultaneously, the first and second counters adjust and store the weights of the first and second synapses. The Clear input serves multiple functions, clearing DFF1 and DFF2 outputs for the subsequent weight assessment, discharging the neuron capacitor, and acting as a clock

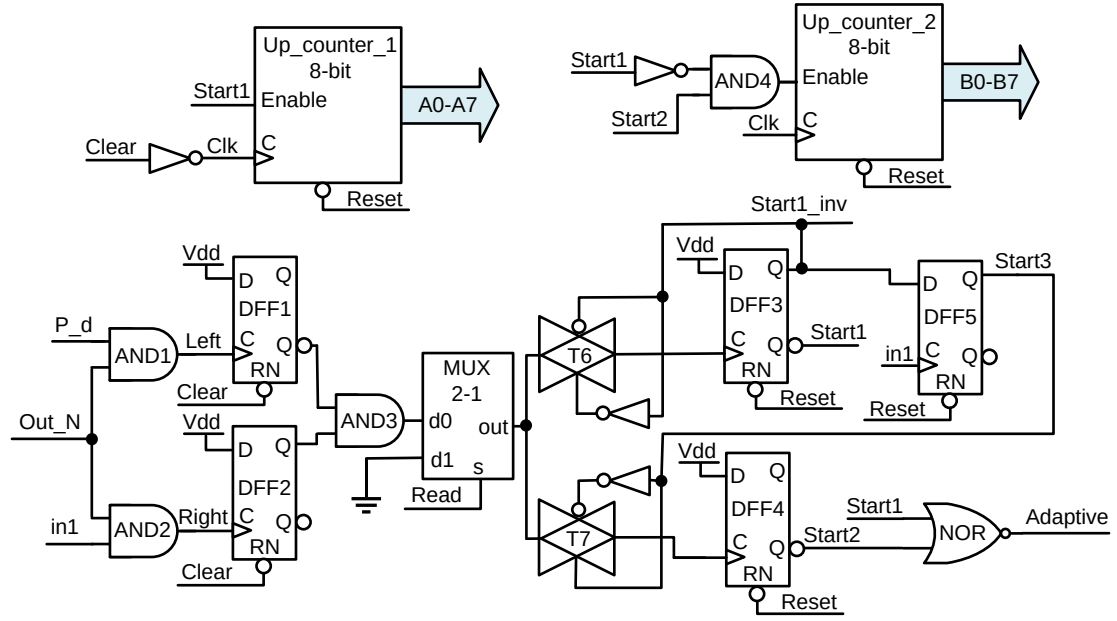


Figure 4.9: The control schematic of the adaptive coincidence detection (ACD) system utilizes a self-adaptive approach to modify synaptic weights and stores these values in up_counters.

for the counter after inversion. The multiplexer, by setting the Read signal to zero, allows the output of the AND3 gate to pass at a specific time. Activation of the multiplexer's selection signal occurs after completing the signal comparisons (P_d , $in1$, and Out_N) and saving the results (left and right) on DFF1 and DFF2. The reset function in the control circuit, as highlighted in Figure 4.9, serves to reset DFF3, DFF4, and DFF5. Activation of the Reset signal initiates the adaptation mode. DFF3 and DFF4 play a role in storing the adaptation weights of the first and second synapses, by saving Start1 and Start2 signals. The Adaptive signal output from the first NOR gate serves to indicate the ACD's engagement in self-adaptation when its value is 0.

During the first state of the adaptation mode, focused on adapting the weight of the first synapse, the flow diagram of the SA-SRC models, as illustrated in Figure 4.11, comes into play. The adaptation process commences with the reset of the control circuit, initializing the counters to zero. Concurrently, signals such as Adaptive, Start3, and Start1_inv are set to 0, while Start1 and Start2 signals are set to 1. These signals intricately manage the transmission gates (T1, T2, T3, T4, T5, T6, and T7), delineated in Figure 4.12 and Figure 4.9. Consequently, T4 and T1 are activated, facilitating the connection between the neuron and the first synapse while disconnecting the second synapse. T1 directs $in1$ to the first synapse, while T2 and T3 sever connections between

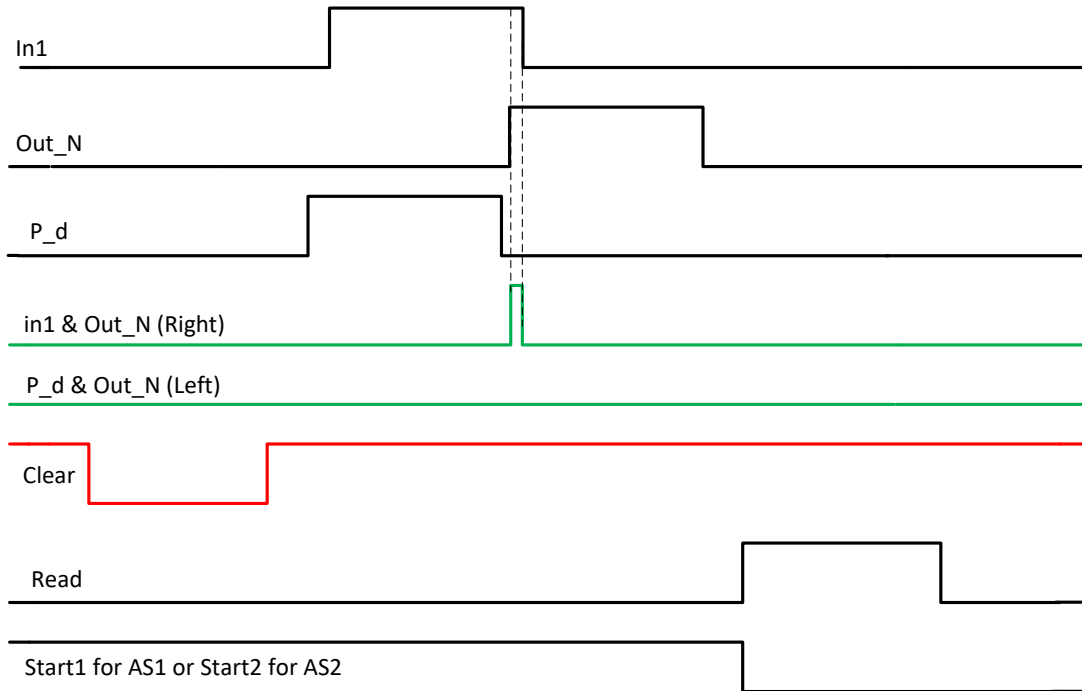


Figure 4.10: The timing diagram for the adaptive synapse illustrates two pulses, P_d and $in1$, which monitor neuron firing times before and after the rising edge of the neuron pulse. When the neuron fires at a designated time, the right signal is set to 1, and the left signal to 0. The Read signal activates to retrieve data after a defined interval.

$in1$ and the second synapse as well as $in2$ and the second synapse, respectively, as depicted in Figure 4.8. Notably, during this phase, the Enable of `up_counter_1` is set to 1, and that of `up_counter_2` is set to 0. Additionally, T6 is engaged, connecting the multiplexer output to the DFF3 clock, while T7 remains inactive, disconnecting it from the DFF4 clock.

Initiating the adaptation process involves applying a pulse signal to the Clear input, facilitating the clearance of DFF1 and DFF2, discharge of neuron capacitors, and an increment in `counter_1`. Subsequently, pulses are directed to the $in1$ and P_d inputs. An assessment of the neuron spike's lateral shift, either left or right, is then conducted through AND1 and AND2 gates, with outcomes securely stored on DFF1 and DFF2, respectively. The combined negative output of DFF1 and the Q output of DFF2 navigate through the AND3 gate to reach the multiplexer.

Subsequently, if the output of the AND3 gate registers as 0, indicating a lateral shift in the neuron's output, it signifies that the synapse's weight hasn't reached the target value. Consequently, the adaptation of the first synapse's weight persists. The output from AND3 traverses through the multiplexer and transmission gate (T6), directing

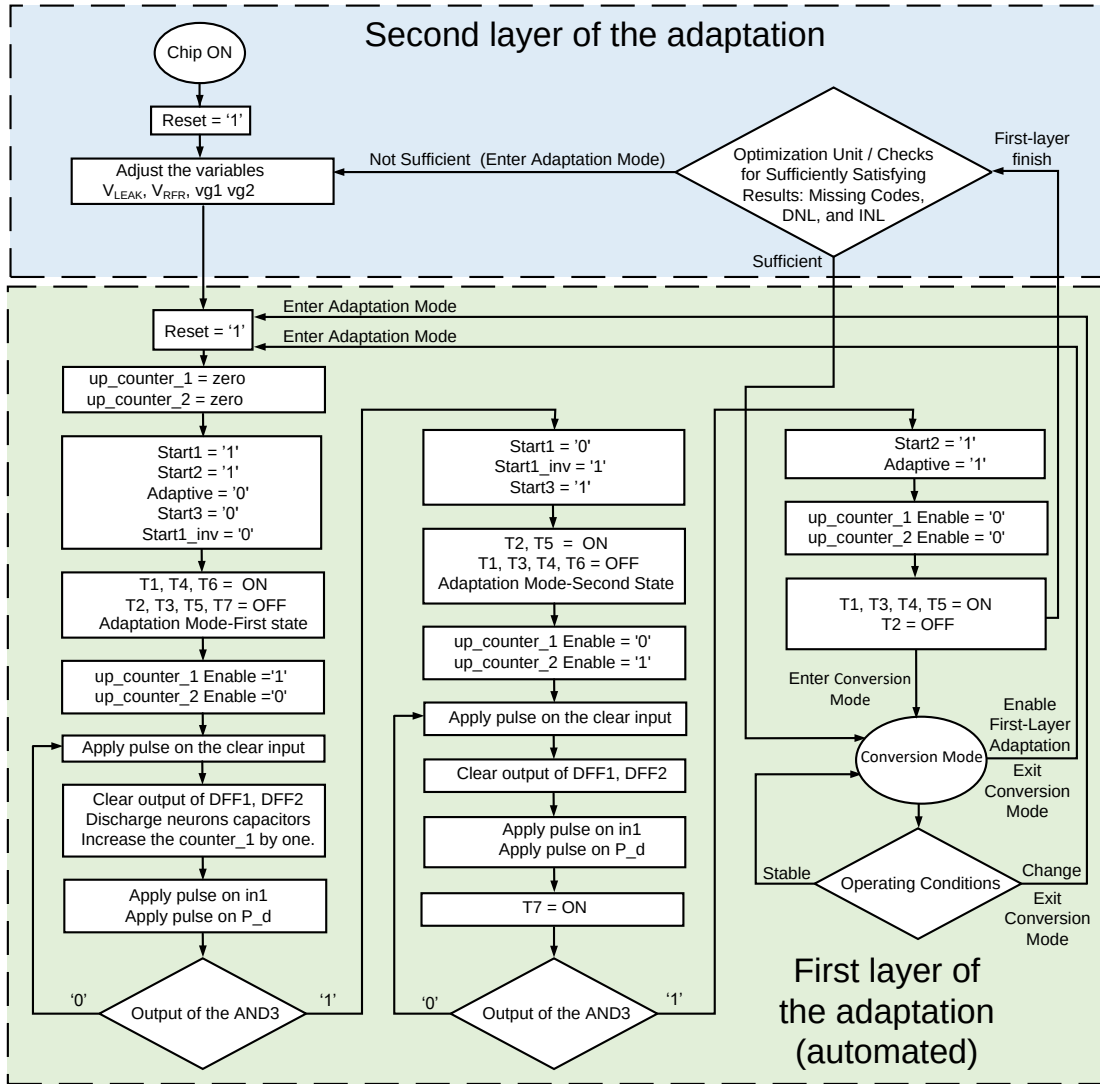


Figure 4.11: The flowchart illustrates the hierarchical structure of the adaptation layers. The first layer handles the adaptive functioning of the ACD. Up_counter_1 and up_counter_2 store 8-bit binary-transistor values for the first and second synapses, respectively. Signals such as Start1, Start1_inv, P_d, Start2, Start3, Adaptive, and Clear are utilized within the ACD's control circuit.

the signal to the clock of DFF3. Simultaneously, Start1_inv remains at 0 while Start1 maintains its state at 1. T6 stays engaged in connecting the multiplexer's output to DFF3. The Enable input of up_counter_1 stays at 1, allowing the counter to increment with the subsequent pulse on the Clear input. Additionally, Start3 remains at 0 upon the next pulse on in1, ensuring the multiplexer's output doesn't establish a connection with DFF4.

The SA-SRC persists in the initial state of the adaptation mode, depicted in Figure 4.8, until the target weight for the first synapse is achieved. It orchestrates a firing event of the neuron within the temporal span between the P_d and in1 signals, resulting

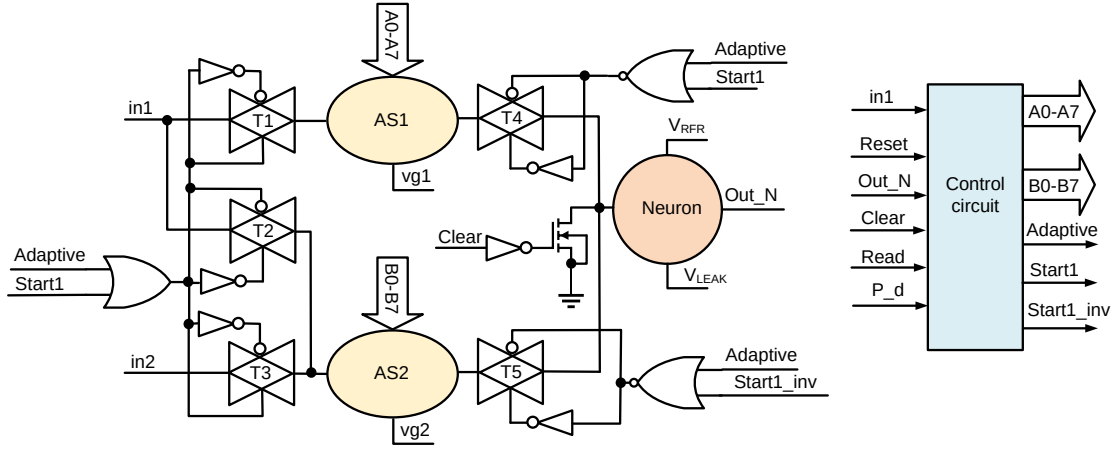


Figure 4.12: The proposed adaptive coincidence detection (ACD) system incorporates two adjustable synapses (ASs) and a single neuron. The control unit applies a self-adaptive approach to adjust synaptic weights. Transmission gates T1–T5 manage the connection and disconnection of the ASs during the weight adjustment process.

in the AND3 gate transitioning to 1. Subsequently, the outputs of DFF3, Start1_inv, and Start1 assume values of 1 and 0, respectively. This prompts the deactivation of T6, discontinuing the connection between the multiplexer output and DFF3. It also halts the modification of the synapse weight by deactivating up_counter_1, marking the completion of the adaptive weight adjustment for the first synapse. Furthermore, up_counter_2 is enabled, and T1, T3, and T4 are deactivated, while T2 and T5 are activated, as delineated in Figure 4.8. This transition signifies the shift of the SA-SRC adaptation mode from the initial state to the second state. Additionally, Start3 assumes a value of 1 with the ensuing in1 pulse, activating T7 and establishing the connection between the multiplexer output and the DFF4 clock.

In the second state of the adaptation mode, corresponding to the adjustment of the second synapse weight, the process mirrors that of the first synapse adaptation. The weight refinement persists until the AND3 gate output transitions to 1, transmitting through the multiplexer and T7 to activate the DFF4 clock. Consequently, the negative output of DFF4, Start2, assumes a value of 0. Subsequently, the output of the NOR gate, labeled as Adaptive in Figure 4.8, attains a value of 1. This prompts the Adaptive output to shift the SA-SRC from the adaptation mode's second state to the normal mode by activating T1, T3, T4, and T5, and deactivating T2, as illustrated in Figure 4.8. The maximum duration for the adaptation process is determined by multiplying the adapt_pulse duration by the maximum number of steps, with the method accommodating

up to 512 steps. It is crucial to recognize that the actual adaptation time may vary depending on the prevailing process, voltage, and temperature (PVT) conditions. Upon powering up the chip, all weights are initialized to zero, each weight associated with a specific delay. The adaptation process initiates anew, persisting until the target synapse weight is attained, ensuring consistent delays across all connections.

Operating at a higher hierarchical level, the second stage of adaptation is tasked with adjusting variables such as V_{LEAK} and V_{RFR} , $vg1$, and $vg2$. Positioned above the initial stage, it awaits the resolution of the first level, which occurs subsequent to any modifications made to V_{RFR} , $vg1$, and $vg2$. The adaptation process concludes when the solution successfully rectifies the synapse weight. In instances where the synapse weight remains uncorrected, the second level proceeds to modify the variables (V_{RFR} , $vg1$, and $vg2$) and initiates adaptation for the next iteration. V_{LEAK} plays a crucial role in resetting the membrane capacitor of the neurons, facilitating its discharge before the next sample through a delivered pulse. In the present phase of design development, manual adjustments are applied to three variables: V_{RFR} , $vg1$, and $vg2$. Following the completion of the adaptation process, the SA-SRC seamlessly reverts to its normal mode. In this operational mode, it adeptly receives input pulses on both of its inputs ($in1$ and $in2$), thereby adjusting the output code in accordance with the time difference between these inputs.

The on-chip SA-SRC cell currently features 16 sparse rank-coded spike outputs. Converting these rank order code outputs into digital numbers involves the design of a WTA circuit and algorithm using Verilog, a hardware descriptive language. WTA cells play a crucial role in determining the winner among the SA-SRC outputs by detecting incoming signals and assigning corresponding orders based on their time of arrival, illustrated in Figure 4.13. For instance, if $in2$ arrives first, it is assigned a value of 1, while $in1$, arriving after $in2$, receives a value of 2. The algorithm, implemented on the Red Pitaya 2, is depicted in Figure 4.14, showcasing the decoding of rank codes into binary codes.

The SA-SDC is designed to generate a digital output code based on the time difference between $in1$ and $in2$. Ideally, this output should evenly span the entire range of time differences, with each code representing a fraction of the time difference. The uniform distribution relies on the weight of the Least Significant Bit (LSB), a value influenced by the converter's resolution and the full-scale time difference (FSTD). The

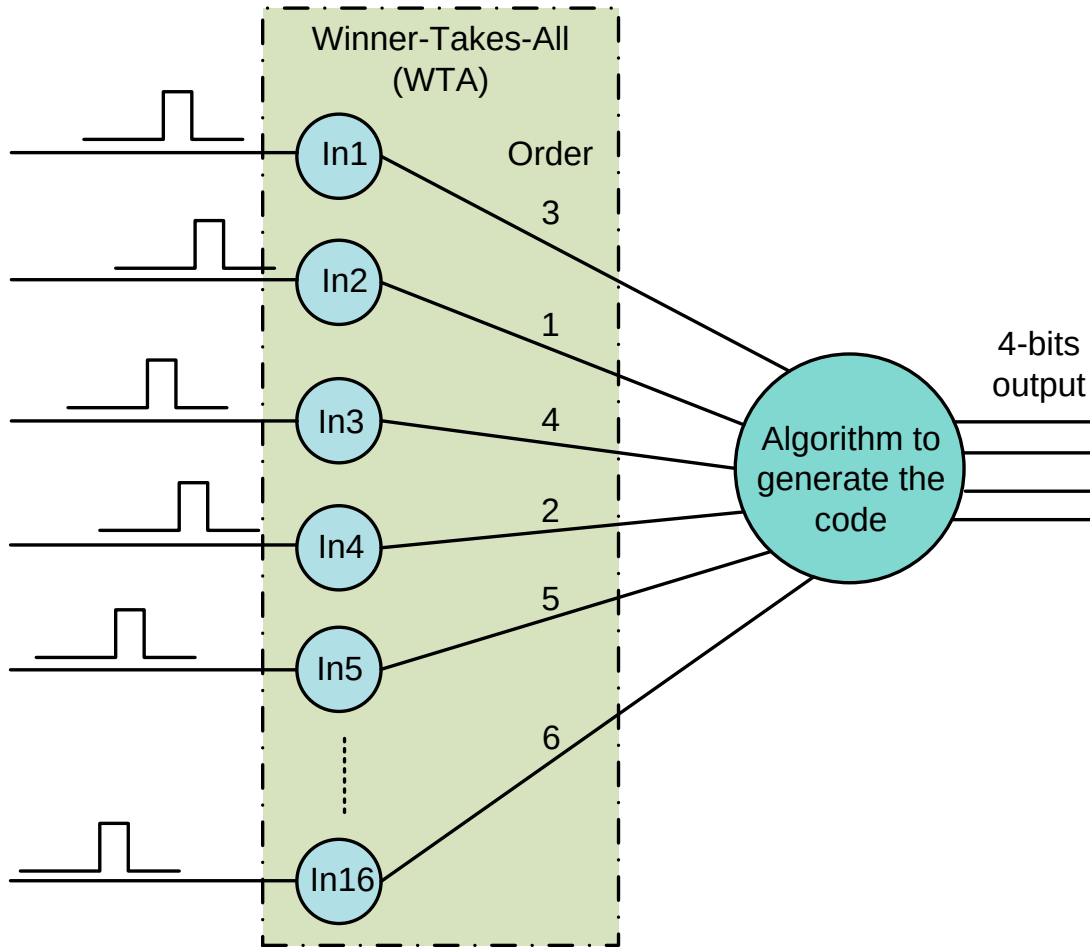


Figure 4.13: The design of a state machine diagram for the WTA and its algorithm converts the rank-order code outputs of the SA-SRC into digital values. The WTA processes incoming signals, prioritizing them by their sequence of arrival.

term "Full-Scale" (FS) denotes the range of time differences between in1 and in2 that the SA-SDC processes, covering the maximum possible time difference. The calculation for the weight of the Least Significant Bit (LSB) is determined by the following formula:

$$\text{LSB} = \frac{\text{FSTD}}{2^n} \quad (4.5)$$

Within this equation, 'n' represents the number of bits employed for resolution. Expanding the cascade with the inclusion of more ACDs enhances the SA-SDC's ability to measure time intervals between in1 and in2, thereby increasing its resolution. Each ACD introduces a 15 ns delay to the chain, representing the least significant bit (LSB). To determine the necessary number of ACDs for measuring the maximum time interval (Tmax) between in1 and in2, the following equation can be applied:

Input: Rank codes with outputs (*out1*, *out2*, *out3*, ..., *out16*)

Output: Binary codes

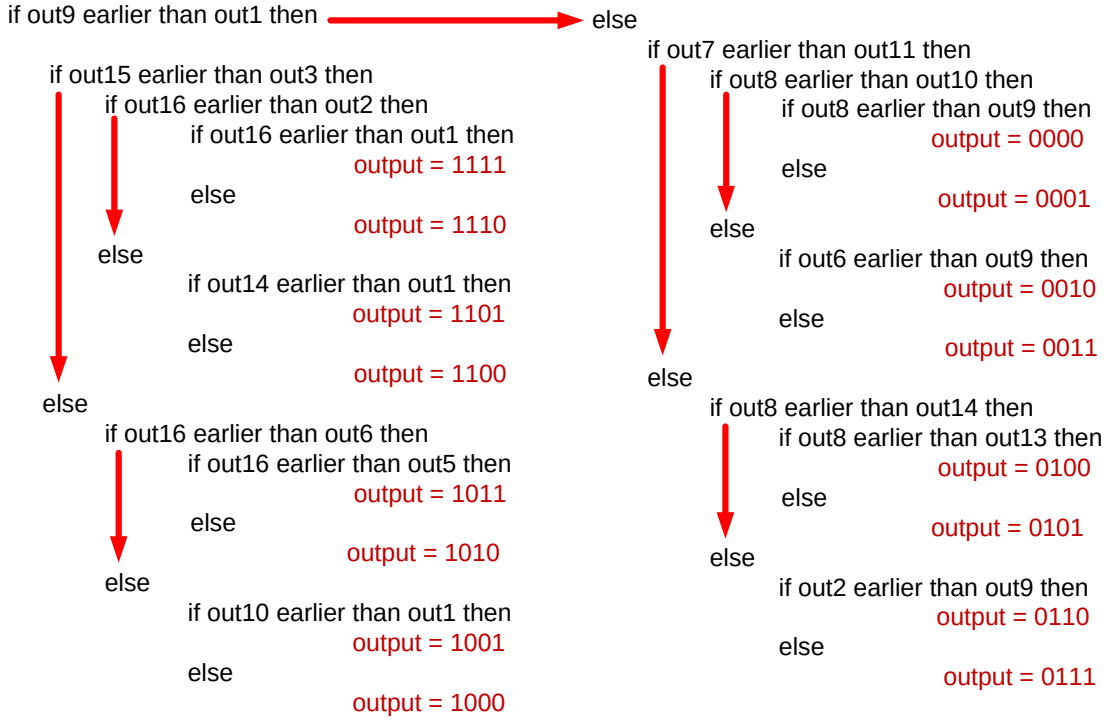


Figure 4.14: The rank code decoding algorithm is used to transform rank codes into binary formats.

$$\text{Number of ACDs} = \frac{T_{\max}}{T_{\text{LSB}}} \quad (4.6)$$

$$\text{Number of levels of ADC} = 2^{\text{NOB}} \quad (4.7)$$

$$\text{Number of levels of SA-SDC} = \frac{T_{\max}}{T_{\text{LSB}}} \quad (4.8)$$

Consequently, based on Equations 4.6, 4.7, and 4.8, the following conclusions can be derived:

$$\text{Number of ACDs} = 2^{\text{NOB}} \quad (4.9)$$

The calculation for the number of bits (NOB) is outlined as follows:

$$\text{NOB}_{\text{SA-SDC}} = \frac{\ln(\text{Number of ACDs})}{\ln 2} = \text{NOB} = Id(x) \quad (4.10)$$

The variable 'x' in the equation represents the quantity of ACDs employed. In the current design iteration, sixteen ACD units have been integrated, as depicted in Figure 4.6. The computation for the number of bits (NOB) is defined by Equation 4.10, yielding a precision of 4 bits. The calculation of the conversion speeds for the neuromorphic spiking sensory system is ascertained through the following equation:

$$\text{Conversion time} = \text{ASSC time} + \text{SA-SDC time} \quad (4.11)$$

In this context, the term "ASSC time" signifies the duration essential for the proper functioning of the ASSC. This duration is adaptable, allowing adjustments based on the synaptic weights to attain the desired gain. The SA-SDC time denotes the duration required for the SA-SDC to transform the time difference value between two input spikes into digital code. This duration is influenced by two essential components: the SA-SRC and the WTA mechanism along with its corresponding algorithm. The calculation of the SA-SDC time is determined by the following equation:

$$\text{SA-SDC time} = \text{SA-SRC time} + \text{WA time} \quad (4.12)$$

The WA time signifies the time needed for the WTA mechanism and algorithm to convert the rank order code outputs of the SA-SRC into digital values. The duration of the SA-SRC is dependent on both the time of the ACDs and the number of ACDs utilized in its construction. This time interval can be calculated using the following equation:

$$\text{SA-SRC time} = \text{Number of ACDs} \times \text{ACD time} \quad (4.13)$$

Chapter 5

Integration of Neuromorphic System Components

In the integrated circuit, the aforementioned issues were addressed through two unique contributions to augment the functionalities of the universal sensor interface with self-X features (USIX), as elaborated in the [77]. The nomenclature of USIX on the multi-project-chip (MPC) is derived from the amalgamation of vital elements for both amplitude and spike-domain representation, accompanied by the integration of self-X capabilities for analog front ends (AFE). The circuit designs were crafted using Cadence design tools and XFAB's $0.35\ \mu\text{m}$ CMOS NWELL technology, supported by the Europractice initiative. The chip encompasses a total surface area of $10.89\ \text{mm}^2$ and incorporates 100 input/output pads, featuring 62,921 transistors. For context, the preceding versions, USIX 1.0 and USIX 2.0, developed by the institution, occupied areas of 11.59mm^2 and 18mm^2 , respectively. These chips provided an all-encompassing solution for sensor interfacing and managing diverse mixed-signal components in the readout circuit pathway. In contrast, the ongoing project centers on the essential AFEX cells within a cost-effective prototyping chip.

5.1 Chip Design and Demonstration Board

The chip undergoes construction through the incorporation of four metal layers. The initial three layers, extending up to metal3, are exclusively designated for the arrangement and interconnection of cells within the lower tiers of the design hierarchy. Conversely,

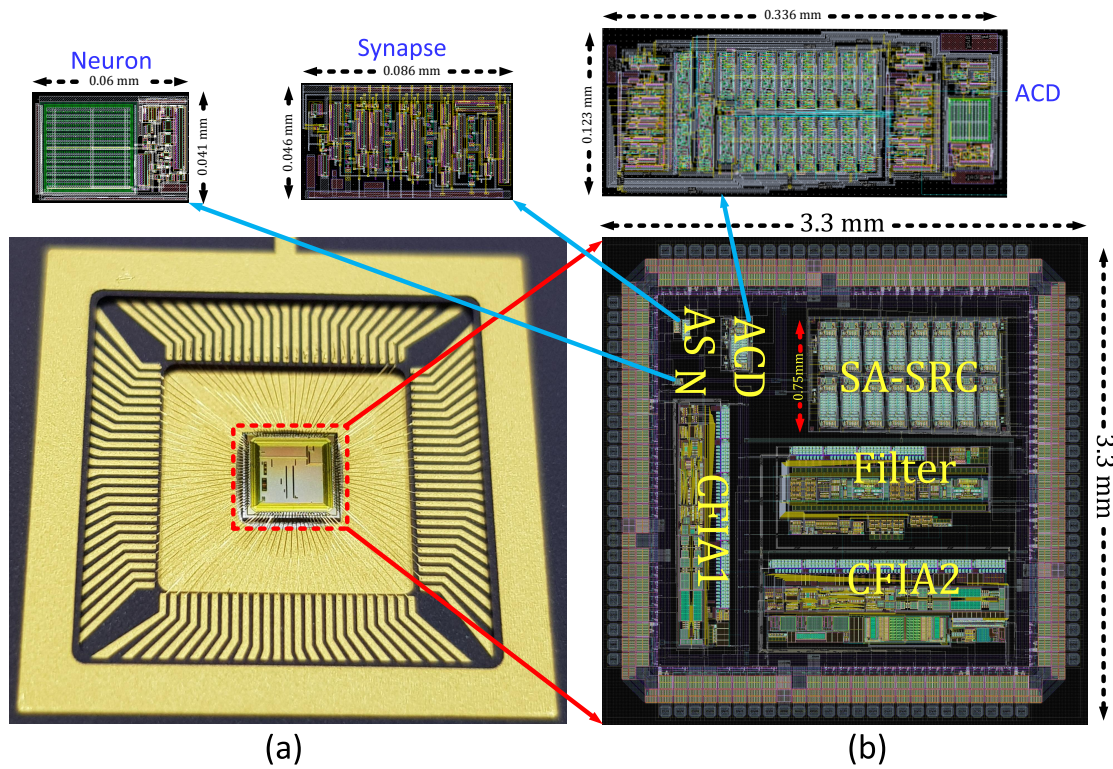
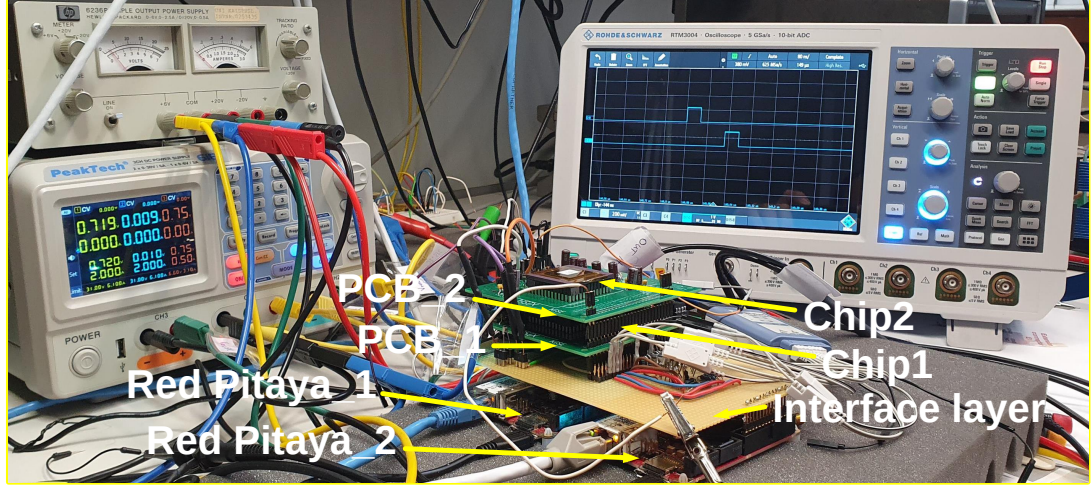


Figure 5.1: MPC USIX chip: (a) After fabrication, the chip showcases bonding wires and a sealing ring, highlighting the integration of essential elements for operation and connection. (b) The layout features a pad frame, reflecting its well-structured design.

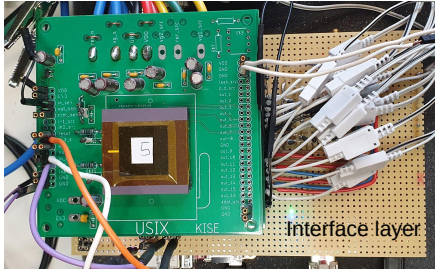
the more substantial metal4 layer is employed to interconnect the power rings within the upper-level hierarchy, chosen for its capability to manage heightened current density. In order to address localized IR drops along the supply rails and avoid surpassing the driving capacity of a single power pad, eleven pads are specifically assigned for powering the chip. The remaining pads consist of 61 digital I/O and 28 analog pads. The driving capability of digital pads is meticulously selected to harmonize with the speed of the designed circuits. Failure to achieve a proper match may result in an excessive driving margin, potentially leading to unnecessary additional dynamic requirements for the power metal width. Substrate contacts are generously distributed among the cells to sustain a uniform bulk potential across the chip's surface. This proves crucial in preventing latch-up issues and averting the formation of forwarded diodes. The pad-frame is formulated to accommodate the chip within the CPGA100 packaging. The amplitude domain was formulated as part of the doctoral investigation conducted by another Ph.D. candidate, [269]. He devised two separate CFIA modules and an adjustable filter, as illustrated in the block-level representation of the chip in Figure 5.1. Another PhD candidate in our research group has explored a cost-effective approach to

enhancing the autonomy and optimization of smart sensory electronic systems (SSES) by integrating AI into automated test equipment (ATE) [270]. His work introduces a novel experience replay particle swarm optimization (ERPSO) algorithm, implemented on Red Pitaya FPGA boards, to enable intrinsic in-field optimization of a reconfigurable instrumentation amplifier.

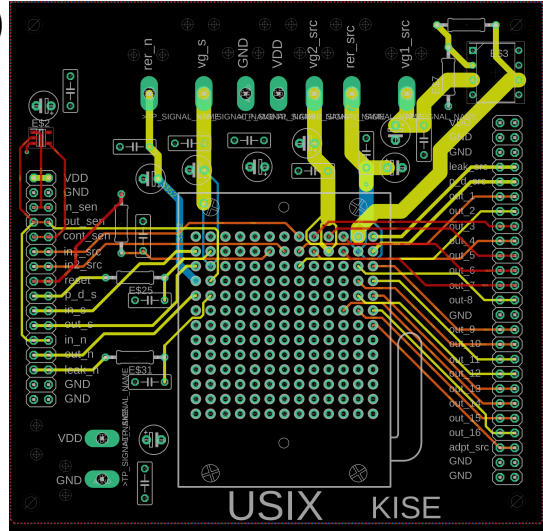
(a)



(b)



(d)



(c)

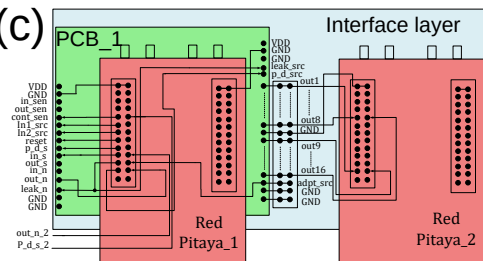


Figure 5.2: (a) The experimental setup highlights the measurement capabilities of a neuromorphic spiking sensory system, utilizing two MPC USIX chips. The first chip integrates SA-SRC, neuron, and synapse cells, while the second contains neuron and synapse cells. (b) A top view shows the second chip on PCB 2 and part of the interface layer, which connects the Red Pitaya boards to the PCBs. (c) The block diagram depicts connections between Red Pitaya 1, Red Pitaya 2, PCB 1, and the interface layer. (d) The four-layer PCB design for the chips was created using Eagle Autodesk, incorporating separate power and ground planes with decoupling capacitors near power pins to minimize noise.

The aim of this work is to enhance the spike domain sector by employing the chip

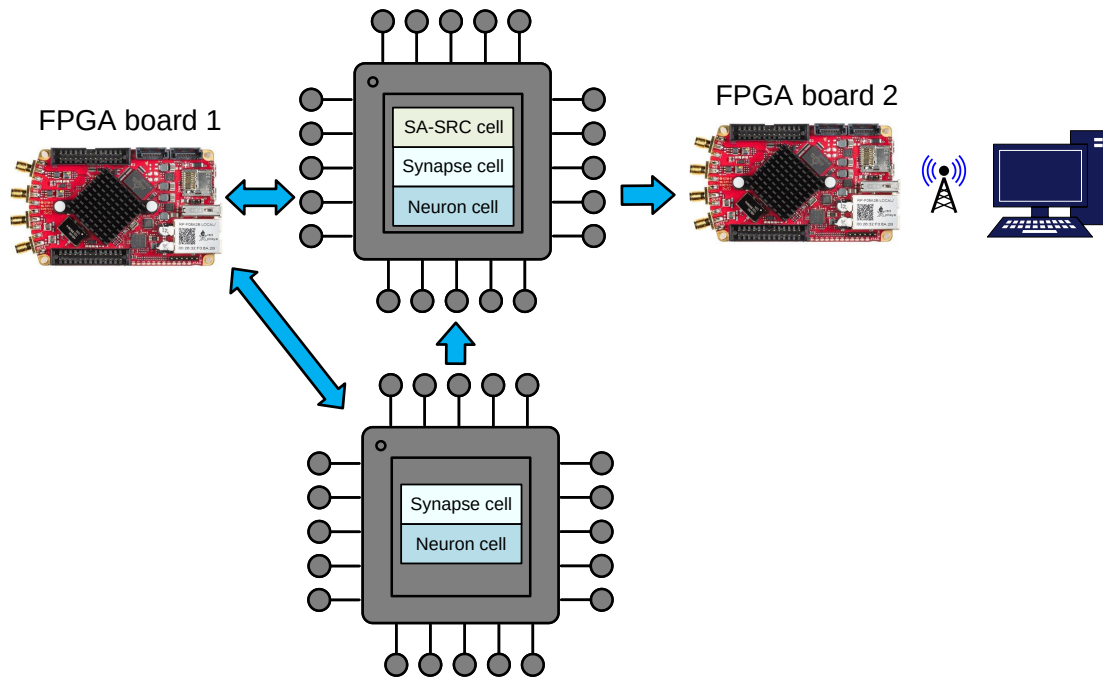


Figure 5.3: The block diagram outlines the hardware prototype for testing key elements of the adaptive neuromorphic spiking sensory system. Two Red Pitaya FPGA boards were used: the first configured to control SA-SRC cells, synapses, and neurons within the programmable logic, and the second implemented the Winner-Takes-All mechanism and rank code decoding algorithm.

and measurement results. The chip integrates crucial elements for the neuromorphic spiking sensory system, such as the neuron, synapse, adaptive self-adaptive spike-to-rank coding (SA-SRC), and coincidence detection (ACD). Detailed insights into the post-manufacturing chip are depicted in Figure 5.1a, while Figure 5.1b illustrates the chip layout implementation. The protective coating, in conjunction with the upper metal layer, conceals the die's features. Before fabrication, simulations are conducted to verify cell functionality at the chip level under nominal conditions, encompassing post-layout parasitic extraction to verify actual connectivity and evaluate the influence of pads on design performance. A thorough internal assessment of the chip will be elaborated in the following chapter.

The initial element in the envisioned sensor system, labeled ASSC, involves a structure consisting of two synapses and two neurons. To implement this design practically, two chips were needed, with each chip accommodating a single neuron and a synapse. For the in-depth hardware-level evaluation and testing of the adaptive neuromorphic spiking sensory system during the prototype demonstration phase, the FPGA assessment platform provided by Red Pitaya was chosen as the embedded computing system. To

achieve integration, a specialized PCB with an integrated socket was utilized to enhance the capabilities of the Red Pitaya system and develop a comprehensive demonstration board, as illustrated in Figure 5.2.

5.2 Implementation and Architecture

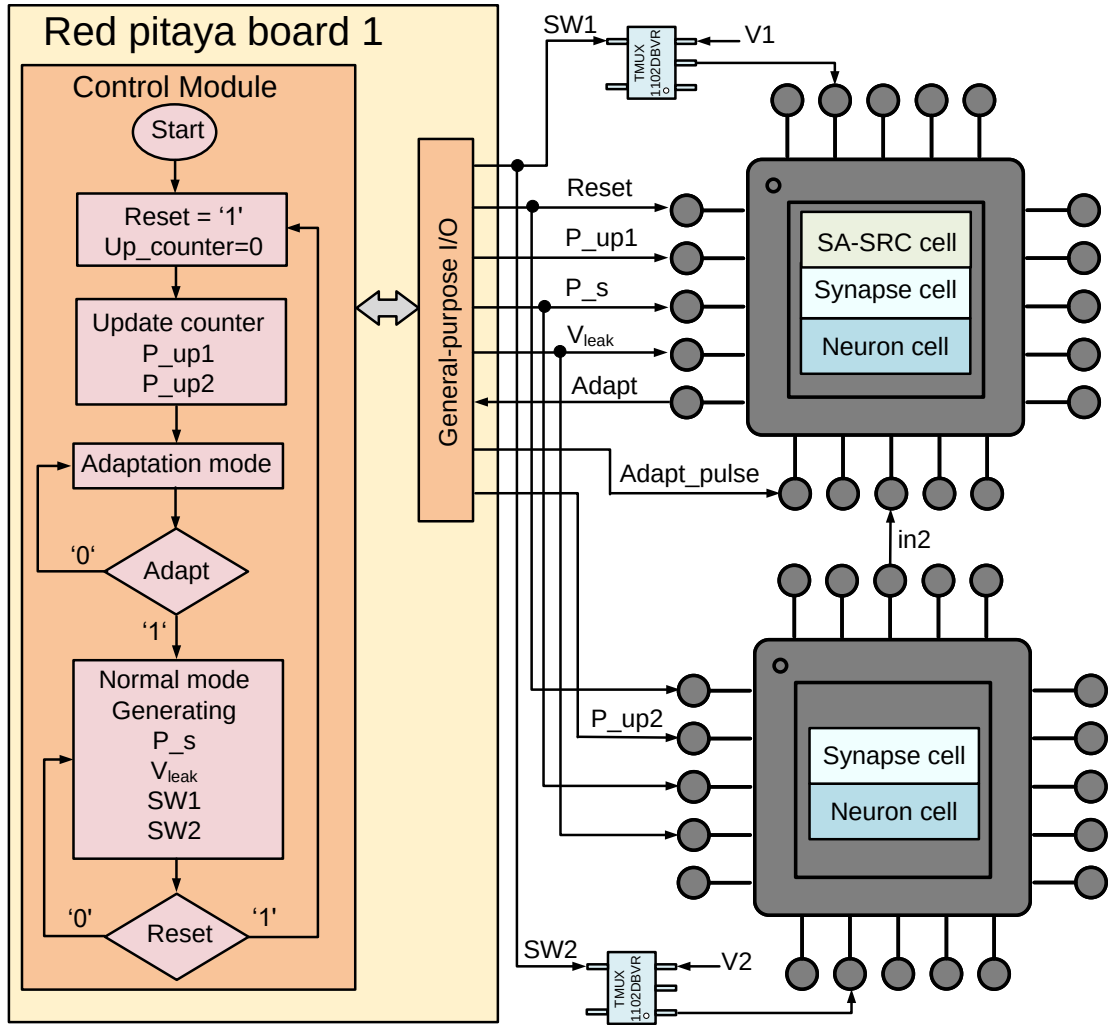


Figure 5.4: The flow diagram of the control module in the programmable logic utilizes the versatile GPIO pins of the Red Pitaya to directly interface with the chip's neuron, synapse cells, and SA-SRC. These GPIO pins are also linked to TMUX1102DBVR chips.

In Figure 5.3, the block diagram representation illustrates the physical hardware setup designed for the prototype demonstration, specifically crafted to assess the functionality of the neuromorphic spiking sensory system. In this experimental arrangement, two FPGA evaluation boards sourced from Red Pitaya are utilized. The primary board is tasked with generating a control module within the programmable logic (PL), over-

seeing the SA-SRC cell, the synapses, and the neurons of the ASSC. On the secondary board, both the Winner-Takes-All (WTA) mechanism and the decoding algorithm for rank codes are executed.

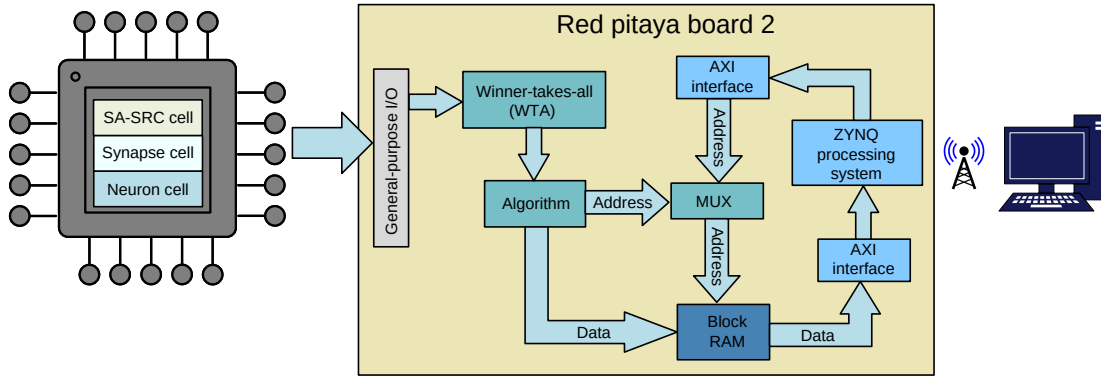


Figure 5.5: Red Pitaya board 2 executes the module architecture, integrating the Winner-Takes-All (WTA) mechanism and the algorithm simultaneously for seamless functionality.

In Figure 5.4 and Figure 5.5, a detailed representation reveals the implemented framework for the adaptive neuromorphic spiking sensory system on Red Pitaya boards 1 and 2, respectively. The Verilog hardware descriptive language was employed to implement a control module within Red Pitaya’s programmable logic (PL), depicted in Figure 15. This module oversees crucial elements in the proposed system: the ASSC and the SA-SRC, managing two synapse cells, two neuron cells, and an SA-SRC cell. The module executes various essential functions, including the control of reset, p_up1, p_up2, P_s, and V_{LEAK} I/O pins linked to synapse and neuron cells. It also generates signals to regulate the functionality of TMUX1102DBVR chips (SW1 and SW2). Furthermore, it manages the V_{LEAK}, adapt, and adapt_pulse I/O pins functionality of the SA-SRC cell. To achieve these tasks, the control module utilizes the general-purpose I/O pins on the Red Pitaya, establishing direct connections to the chips’ I/O pins. The Texas Instruments TMUX1102 switches, precision complementary metal-oxide semiconductor (CMOS) switches, are incorporated. On the dedicated Red Pitaya board 2, both the WTA mechanism and the algorithm are implemented, illustrated in Figure 5.5. Successful integration of the MUX allows seamless switching of the block RAM’s address, enabling alternation between addresses from the algorithm module during writing and addresses from the processor during reading operations.

Chapter 6

Neuromorphic Chip

Characterization and Application

This chapter aims to showcase the measurement attributes of the neuromorphic spiking sensory system integrated into a manufactured chip. The first phase of this experimental process centers on characterizing the components within the envisioned system, namely the ASSC and SA-SDC. Subsequently, the process moves forward to connect the ASSC with the SA-SDC, aiming to thoroughly characterise the entire system in question. The Neuromorphic Spiking Sensor is integrated with TMR integration for real-world applications.

6.1 Characteristics of ASSC on Chip

The ASSC generates a pair of spikes, and the time gap between them depends on the voltage difference between V1 and V2. Shown in Figure 6.1 is the ASSC output when V1 is adjusted to 0.9 V while V2 remains at 0 V. The ASSC's synapse weights are controlled by the up counters and the voltages vs1 and vs2. Initially, the up counters are initialized at 255, and the voltage levels vgs1 and vgs2 are set to 2.4 V and 2.35 V, respectively. With these particular synaptic weights, the transfer function of the ASSC displays an offset, as depicted in Figure 6.2. The magnitude of this offset, calculated using equation 4.2, is found to be 77.6 LSB. To address this offset, modifications were applied to the synapse weights, as shown in Figure 6.2. In this modified setup, the up counters were maintained at a value of 255, while both vgs1 and vgs2 were adjusted to 2.4 V.

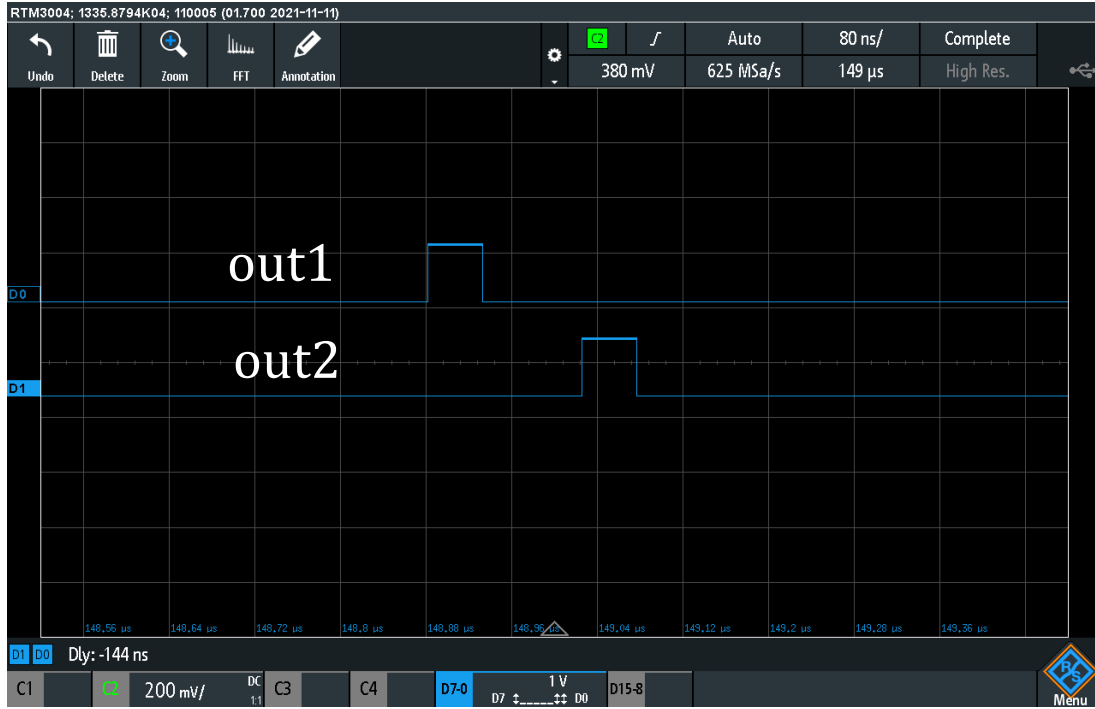


Figure 6.1: The ASSC produces an output when 0.9 V is applied to V1, while V2 remains at 0 V.

To characterize the ASSC's transfer function, the voltage difference between V1 and V2 was systematically varied from -1.45 V to 1.45 V in 0.05 V increments. The modulation of gain is achieved by tuning the synaptic weights in the ASSC. Figure 6.3 and Figure 6.4 portray the transfer function of the ASSC, illustrating the measurement results for different gains. By fine-tuning the gain settings, the duration of the ASSC has been prolonged, leading to an increase in the number of bits effectively resolved by the SA-SDC. The achievable MNoB, resulting from these gain adjustments, can be calculated employing formula 4.3, resulting in a measure of 11.98 bits.

6.2 Characteristics of SA-SDC on Chip

This work investigates the characteristics of the SA-SRC cell and its adaptability on a fabricated chip. The adaptation procedure initiates with the reset of the SA-SRC. Once the reset signal reverts to one, the SA-SRC undergoes adaptation using a pulse signal named `adapt_pulse`, as shown in Figure 6.5. The output signal, `adapt`, signifies whether the SA-SRC is currently undergoing self-adaptation, with a value of 0 indicating so. Weight adaptation is achieved through the input pulse `adapt_pulse`, functioning at a frequency of 2 MHz, resulting in a time of one step being 500 ns. Throughout the

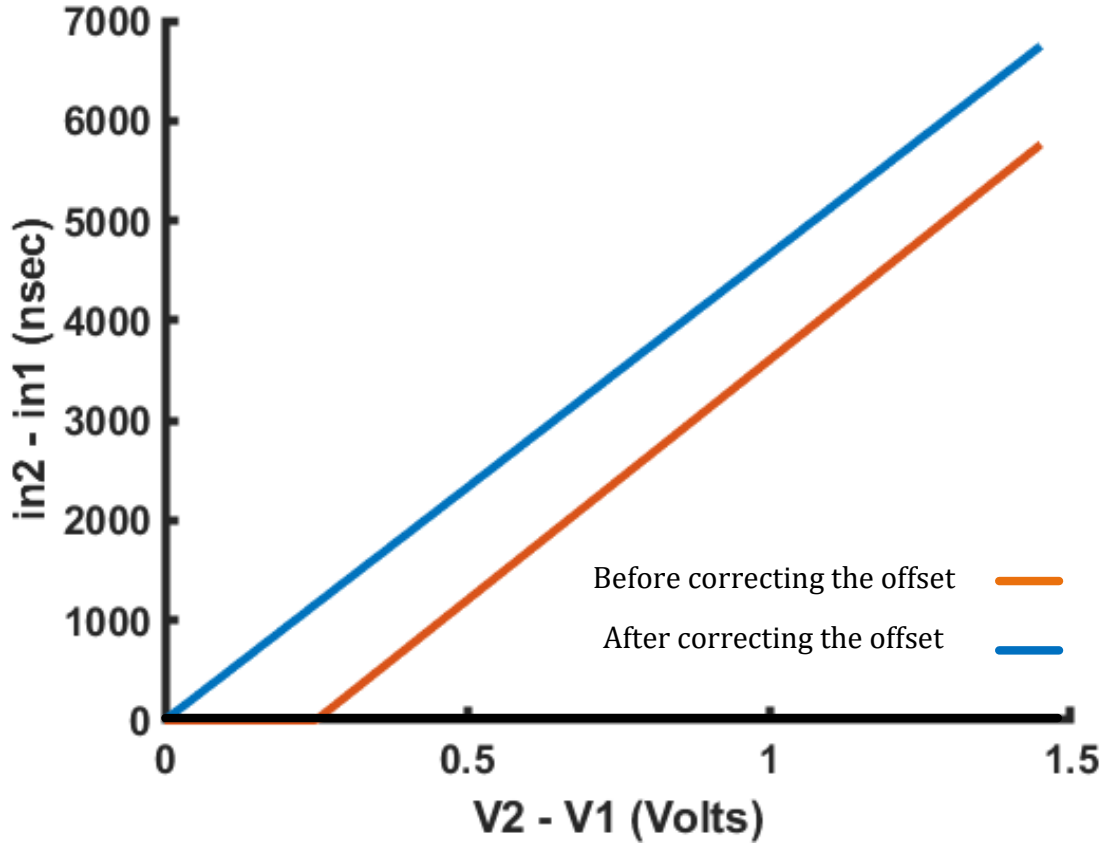


Figure 6.2: Highlights the effectiveness of the ASSC in correcting offset deviations. The synaptic weights were modified to compensate for this error.

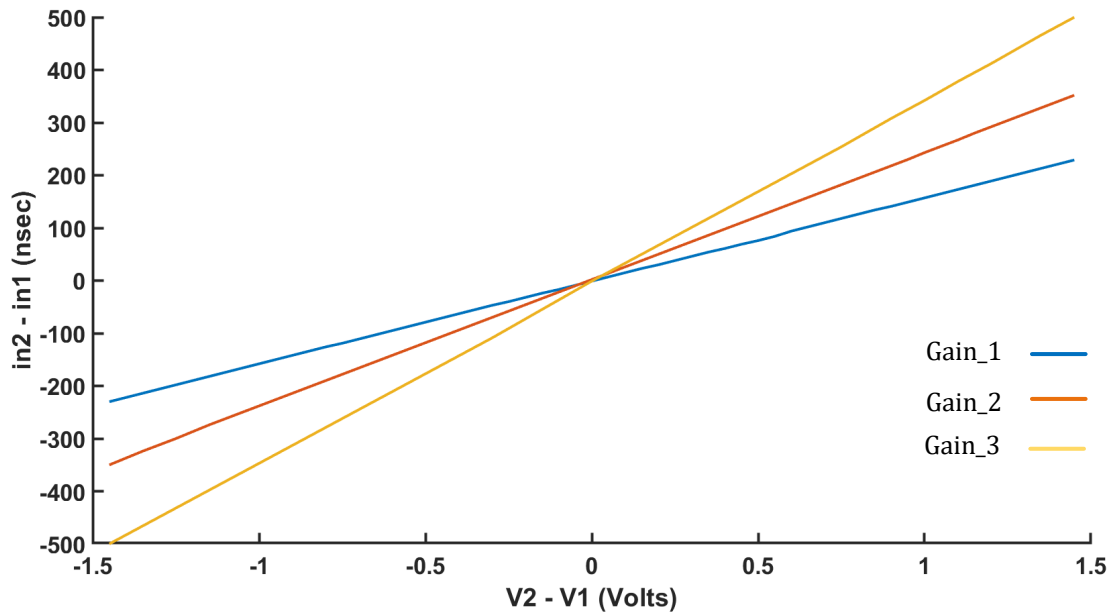


Figure 6.3: The ASSC system's response is evaluated using a measurement method designed for low-gain conditions.

experiment, both the adaptation time and the count of steps taken by the SA-SRC were documented, and at a room temperature of 22 °C, the recorded values were 210 μ s for

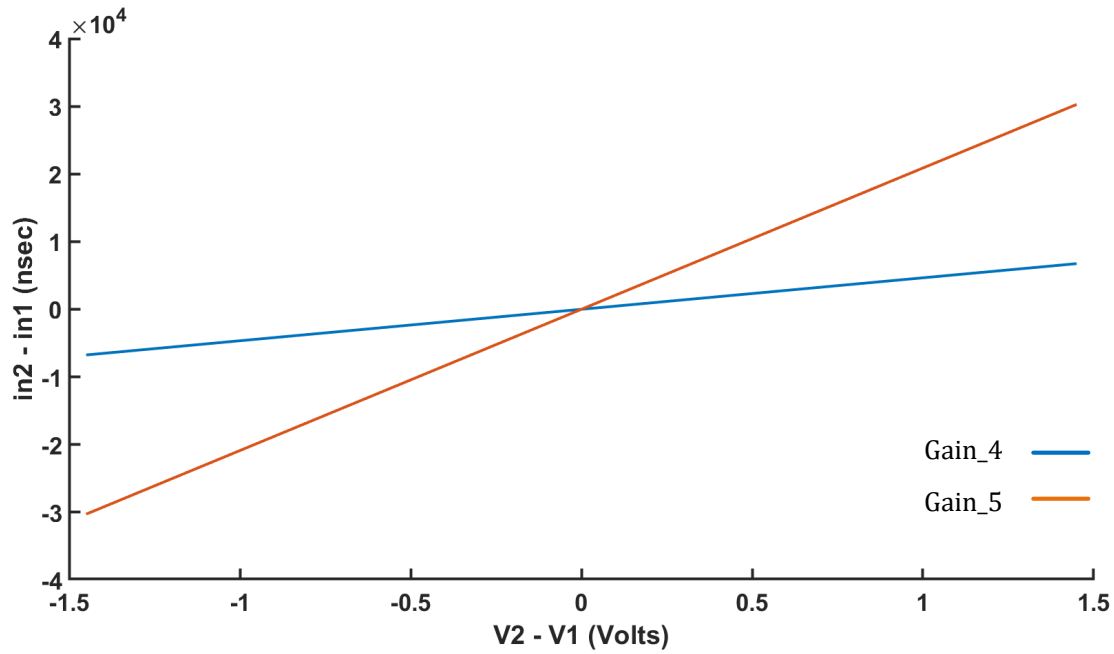


Figure 6.4: The ASSC system's response is evaluated using a measurement method designed for high-gain conditions.

adaptation time and 420 steps.

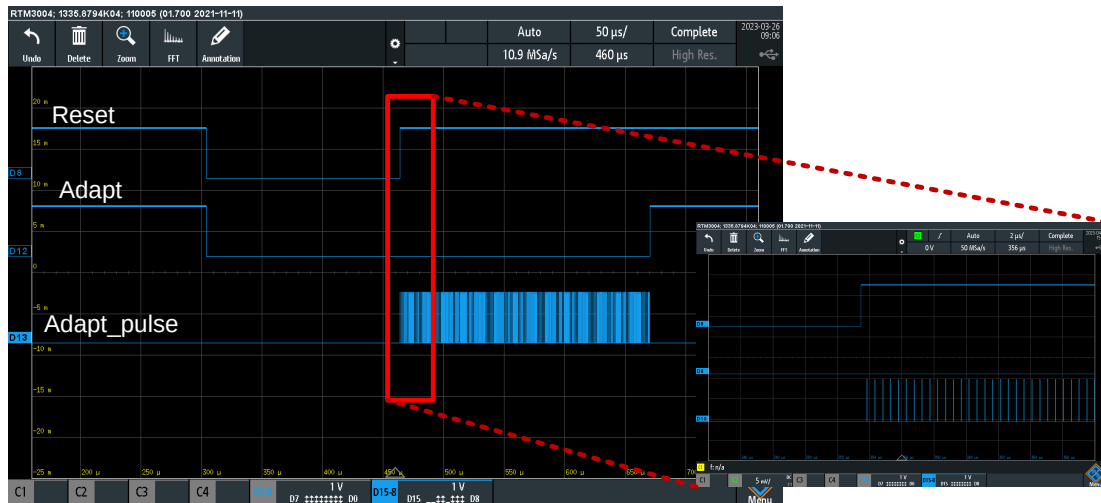


Figure 6.5: Adaptation process measurement outcomes for the SA-SRC cell on the chip.

The SA-SRC block receives input from two outputs, $in1$, and $in2$, originating from the ASSC. In the process of characterizing the SA-SRC block, an Agilent pulse generator (hp hewlett packard 8131A), as depicted in Figure 6.6, was used to generate the inputs. At the second level, four variables $vg1$, $vg2$, V_{LEAK} , and V_{RFR} are present. In the current design phase, manual adjustments have been made to $Vg1$, $Vg2$, and V_{RFR} . Initially, empirical data and observations guided the determination of values for $Vg1$,

V_{g2} , and V_{RFR} , which were 2 V, 0 V, and 0.75 V, respectively. V_{LEAK} , another variable, is employed to reset the membrane capacitor of the neurons based on empirical data. To guarantee the discharge of the membrane capacitor before the subsequent sample, a pulse featuring a width of 80 ns and an amplitude of 3.3 V will be applied. The control of V_{LEAK} is managed by the Red Pitaya.

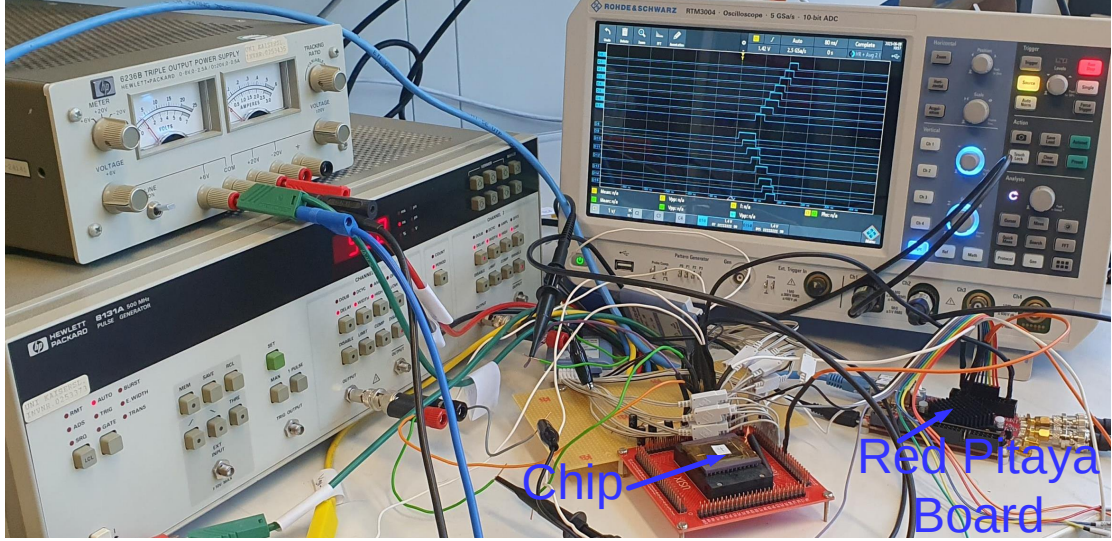


Figure 6.6: Presenting an SA-SRC block-on-chip test setup using a supporting PCB and Red Pitaya.

The results obtained from the experiment, as illustrated in Figure 6.7 and Figure 6.8, showcase the distinctive codes generated by the SA-SRC when subjected to input pulses with varying time differences (TD). The SA-SRC outputs denoted as out1 to out16, signify the spike order code, with the numerical annotations on the output waveforms indicating the sequence of the spike order in comparison to other outputs. In Figure 6.7, in2 precedes in1 with a time difference of 120 ns, while Figure 6.8 displays the reverse scenario, where in1 precedes in2 with a time difference of 15 ns.

The functionality of the SA-SRC is assessed across different voltage levels. Variations in output spike orders are observed with a shift in power supply from 3.3 V to 3 V, as shown in Figure 6.9. The inherent automatic adaptation mechanism in the initial layer compensates for these changes, resetting the output spike orders to their initial states, as evidenced in Figure 6.8. Throughout the duration of the experiment, both the adaptation time and the number of steps required by the SA-SRC were recorded. Results obtained at a room temperature of 22 °C indicate an adaptation time of 225 μ s and 450 steps. The measurement outcomes validate the SA-SRC's capability to counteract fluctuations

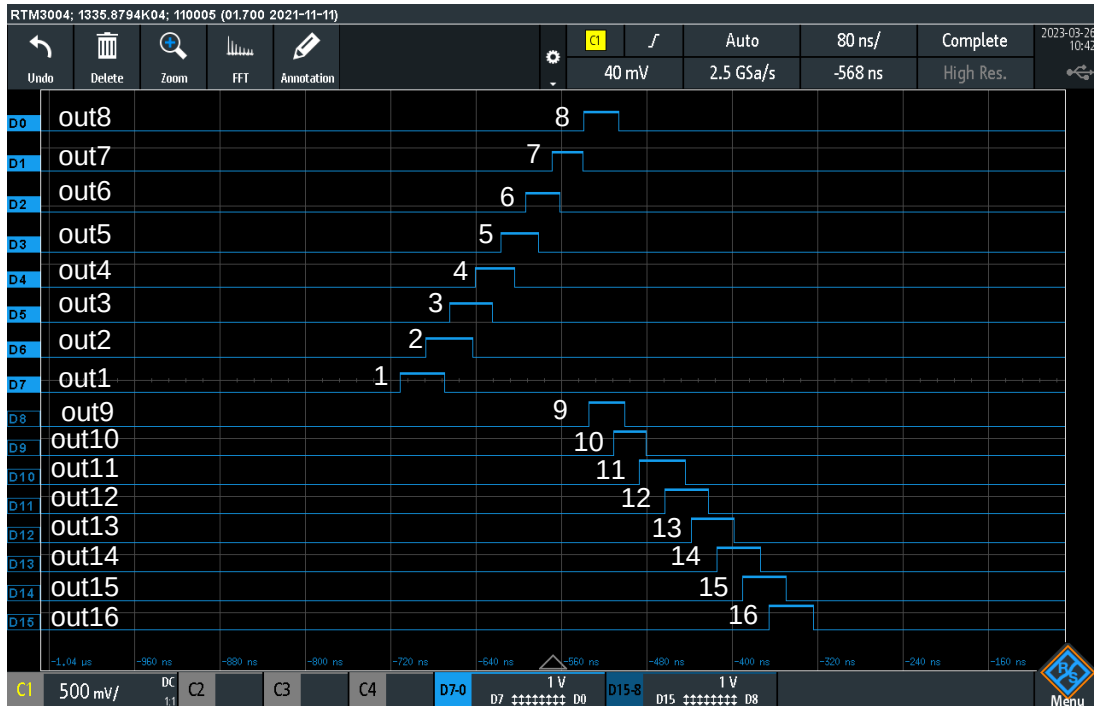


Figure 6.7: On-chip measurement results of the SA-SRC, where in2 follows in1 with a 120 ns delay.

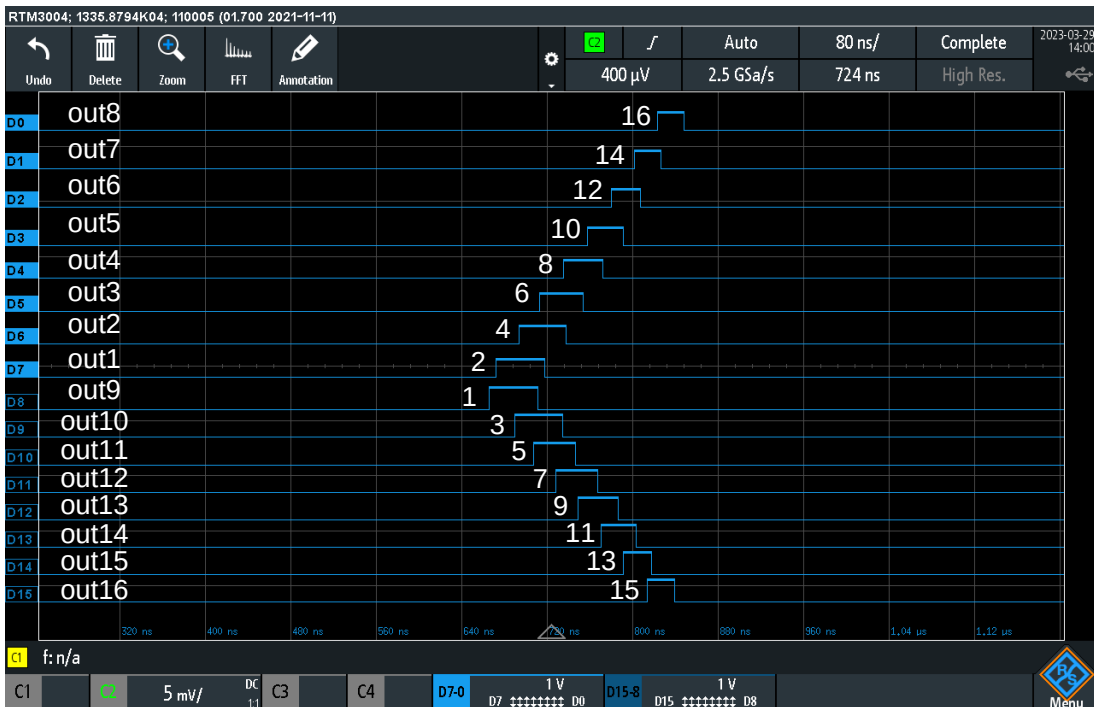


Figure 6.8: On-chip measurement results of the SA-SRC, where in1 follows in2 with a 15 ns delay.

in both process and voltage.

In the initial phase, a pulse generator was employed to define the input range of the SA-SRC. This involved adjusting the time delay between the in1 and in2 signals. The

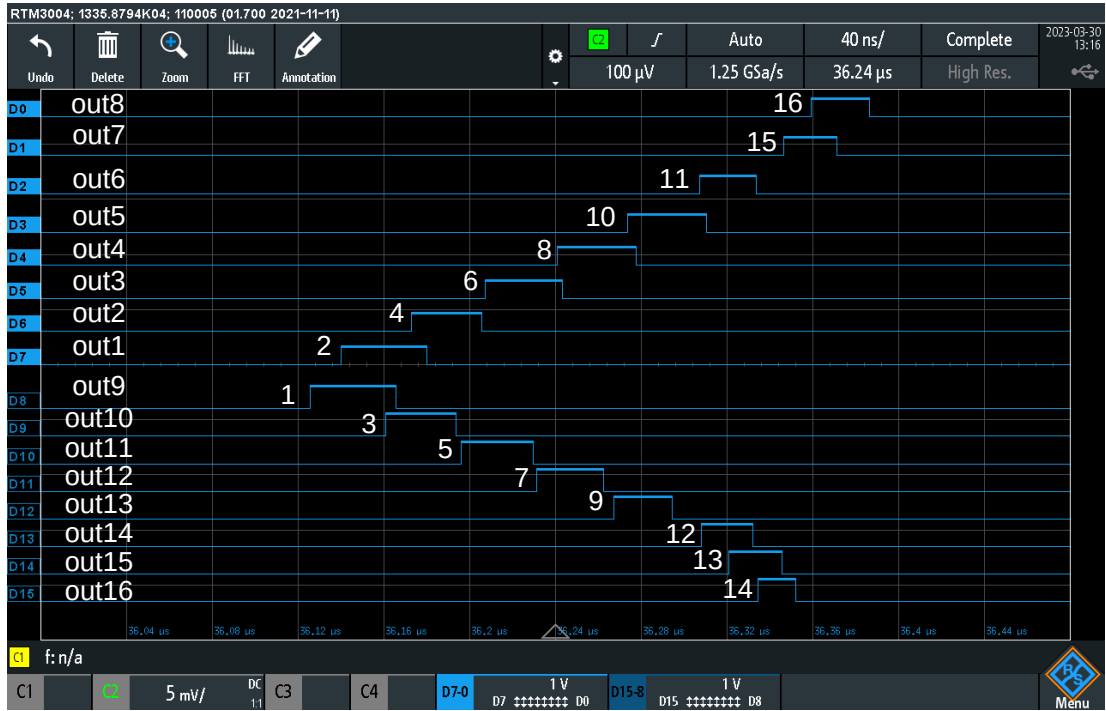


Figure 6.9: SA-SRC measurements show that the on-chip signal in1 advances in2 by 15 ns. The order of output spikes shifts as the voltage decreases from 3.3 V to 3 V

observed range displayed a shift from -120 ns to +120 ns. Based on the experimental results, it is evident that the SA-SRC cell exhibits the capacity to generate 16 unique spike order codes, each corresponding to specific time difference values between its input signals. The time difference (TD) spans from -120 to 120 ns, representing a 4-bit binary code. Consequently, FSTD is established at 240 ns, and the determination of the least significant bit (LSB) involves the computation outlined in equation 4.5, yielding a value of 15 ns.

To assess the SA-SRC's functionality, specifically the INL, DNL, and transfer function, a pulse generator was employed to generate a single cycle ranging from -120 ns to 120 ns. By systematically modifying the time discrepancy between in1 and in2 in increments of 1 ns (equivalent to 0.067 LSB), the entire range from -120 ns to 120 ns was covered. Three experiments were conducted to examine the operational performance of the SA-SRC.

The first assessments were carried out in ambient conditions with V_{dd} set at 3.3 V and a temperature of 26°C. Figure 6.10 shows the transfer function of the SA-SRC in the first experiment, illustrating the correlation between the SA-SRC output (vertical axis) and the time difference between in2 and in1 (horizontal axis). Each time interval in the

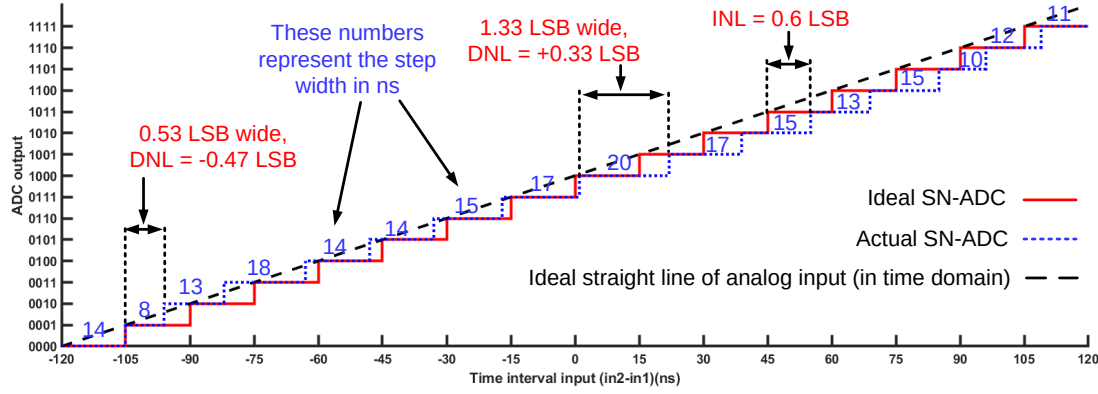


Figure 6.10: SA-SRC transfer function: actual vs. ideal curves. Adaptation transitions from reset to the target synapse weight upon powering the chip. Post-adaptation measurements at $V_{dd} = 3.3$ V.

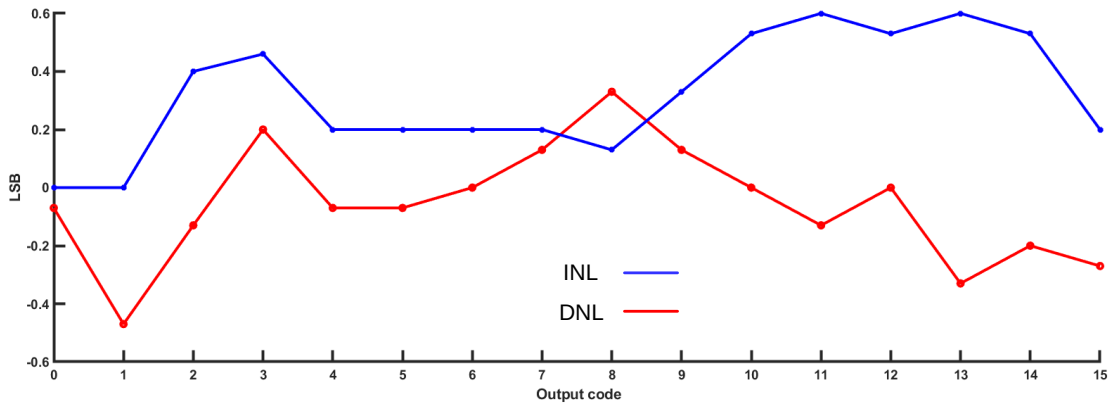


Figure 6.11: DNL and INL curves were recorded for the measured response in Figure 6.10 under ambient conditions at $V_{dd} = 3.3$ V.

SA-SRC input corresponds to a binary code at the output. Ideally, the SA-SRC should exhibit a step width of 1 LSB, representing the smallest increment in its time-to-digital conversion process. The disparity between the ideal and actual step widths is termed the differential non-linearity (DNL) error. Conversely, the integral non-linearity (INL) gauges the maximum deviation between the real and ideal response curves.

As per the experimental findings, the parameters of the SA-SRC, including DNL, INL, and the number of missing codes (NOMCs), exhibit nominal values of 0.47, 0.6 LSB, and zero missing codes, respectively, as indicated in Figure 6.10. Figure 6.11 provides the DNL and INL curves for the actual curve in Figure 6.10.

During the second evaluation, the power supply transitioned from 3.3 V to 3 V, and the temperature was 27°C , as indicated in Figure 6.12. In this scenario, four missing codes (NOMC) were detected, representing steps without available data. The DNL and INL values, measured at 0.6 and 2.07 LSB, respectively, are illustrated in Figure 6.12.

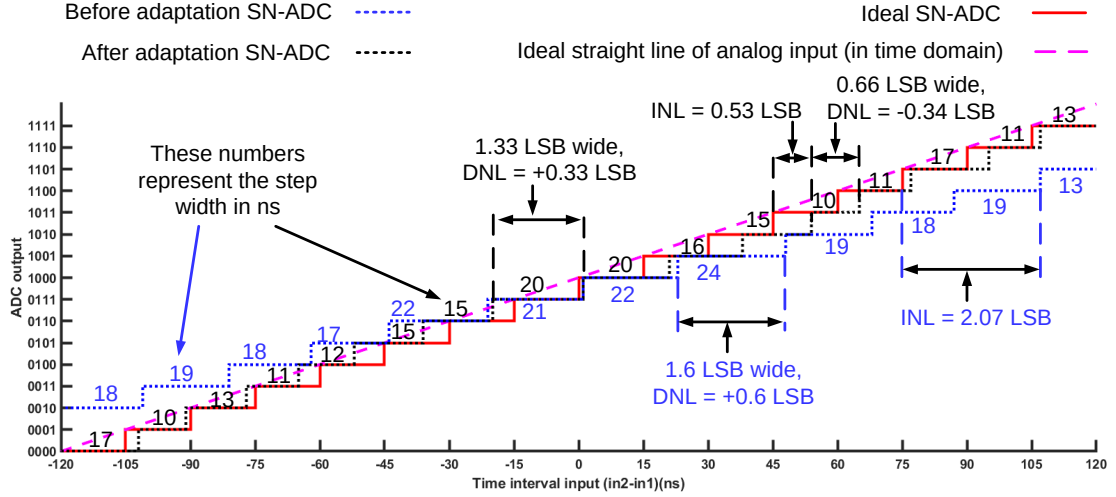


Figure 6.12: SA-SRC transfer functions: ideal, pre-adaptation, and post-adaptation. Pre-adaptation measurements follow a V_{dd} shift from 3.3 V to 3 V, while post-adaptation measurements reflect the final state at $V_{dd} = 3$ V.

The automatic adaptation mechanism of the first layer effectively compensates for these fluctuations, ensuring the absence of missing codes (NOMC) with DNL and INL values of 0.34 and 0.53 LSB, respectively.

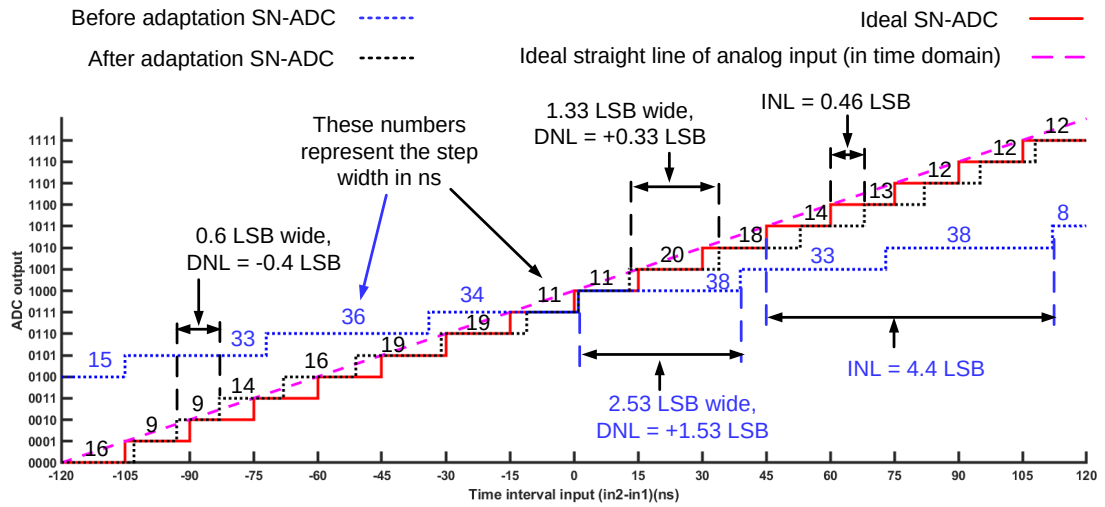


Figure 6.13: SA-SRC transfer functions: ideal, pre-adaptation, and post-adaptation. Pre-adaptation measurements follow a V_{dd} shift from 3.3 V to 2.4 V, while post-adaptation measurements reflect the final state at $V_{dd} = 3$ V.

For the third assessment, the power supply was altered from 3.3 V to 2.4 V, with a temperature at 29.9 °C, as depicted in Figure 6.13. In this instance, eight missing codes (NOMC) were identified, accompanied by DNL and INL values of 1.53 and 4.4 LSB, respectively. The compensation for these deviations, illustrated in Figure 6.13, involved adjustments to the variables $vg1$, $vg2$, and V_{RFR} to 0.6 V, 0 V, and 0.74 V,

respectively, coupled with the execution of the automatic adaptation process in the first layer. Following adaptation, the SA-SRC parameters exhibited no missing codes (NOMC) and demonstrated DNL and INL values of 0.4 and 0.46 LSB, respectively, as shown in Figure 6.13.

6.3 Characteristics of a Neuromorphic Sensory System on Chip

After the initial characterization, the ASSC is connected with the SA-SDC to examine the entire system under investigation. The first segment of the SA-SDC denoted as the SA-SRC, produces sixteen outputs, each generating a spike. The sequence of these spikes indicates the time disparities between the spikes received at their inputs from the initial ASSC block. Figure 6.14 visually illustrates the output of the SA-SRC when the inputs V1 and V2 of the ASSC are adjusted to 0 V and 0.2 V, respectively. Depicted in Figure 6.15 is another scenario depicting the SA-SRC's response to varied input voltage settings, where V1 and V2 are configured to 0.55 V and 0 V, respectively, within the ASSC. The outputs of the SA-SRC, identified as out1 to out16, serve as representations of distinct spike order codes. The numeric markings on the output waveforms signify the sequential order of these spike codes in relation to one another.

Based on the experimental outcomes, the SA-SRC cell's ability to generate 16 distinct spike order codes, each associated with specific temporal differences between its input signals, is ascertained. This translates to encoding the information into a 4-bit binary representation. To characterize the SA-SRC's input span, the time delay between signals in1 and in2 was manipulated and measured. The empirically measured range covered from -120 ns to +120 ns. Consequently, the Full Span Time Duration (FSTD) amounts to 240 ns, and the calculation outlined in equation 4.5 yields the Least Significant Bit (LSB) value at 15 ns.

In terms of speed, the SA-SRC accomplishes a conversion time of 370 ns. On Red Pitaya board 2, both the execution of the WTA circuit and algorithm occur. This entails converting the rank order code outputs from the SA-SRC cell into digital values and storing them in the block RAM of the PL. The translation from rank to dense digital code takes approximately 1.035 ns. The SA-SDC time represents the duration

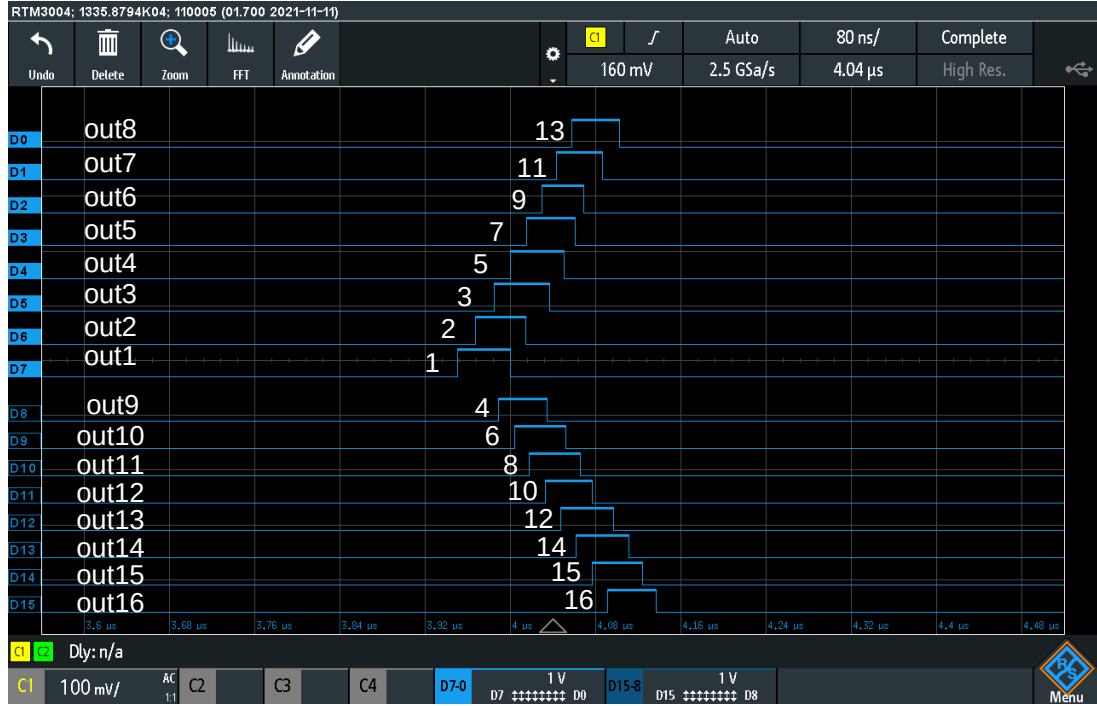


Figure 6.14: The SA-SRC output was recorded with ASSC inputs V1 at 0 V and V2 at 0.2 V.

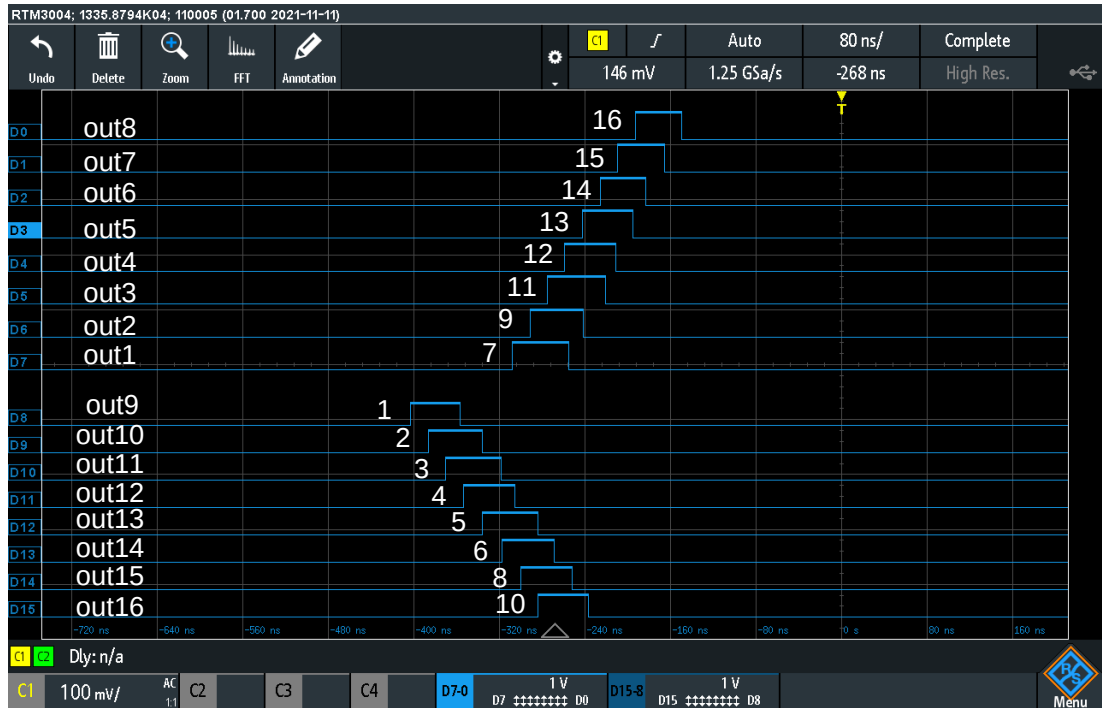


Figure 6.15: The SA-SRC output was recorded with ASSC inputs V1 at 0.55 V and V2 at 0 V.

needed for the SA-SDC to convert the temporal gap between two spikes captured at its input into digital code, as determined by equation 4.12, resulting in a total of 371.035

ns. The conversion speeds of the neuromorphic spiking sensory system were evaluated using equation 4.11, yielding a final result of 491.035 ns.

Assessing the functionality of the neuromorphic spiking sensory system includes examining diverse parameters. These specified parameters are categorized into two groups within the converter's specifications, those associated with the transfer function and those indicating the distortion introduced to the converted signal. Within the initial category, static parameters encompass integral non-linearity (INL), differential non-linearity (DNL), and missing code metrics. These measurements play a pivotal role in understanding the precision and operational characteristics of the system. The SA-SDC is designed to exhibit a step width of 1 LSB, signifying the smallest increment in its time-to-digital conversion process. Discrepancies from this ideal condition are quantified as differential non-linearity (DNL) errors. Furthermore, integral non-linearity (INL) gauges the maximum deviation from the actual response curve to the ideal curve. A proficient SA-SDC should remove missing code cases, where certain output codes are absent due to gaps in the digital output, typically arising from the absence of analog input values associated with specific codes.

The usual approach for assessing the DC characteristics of the SA-SDC, encompassing INL, DNL, missing code, and transfer function, entails a specific experimental configuration. Within this arrangement, a function generator is set to generate a gradual voltage ramp, spanning from the minimum to the maximum input voltage. This voltage ramp is then applied to the inputs of ASSC, denoted as V1 and V2. These inputs trigger the production of time delays in the ASSC outputs, identified as out1 and out2. The time delays transition across the range of -120 ns to +120 ns, effectively covering the entirety of the SA-SDC's input spectrum. This test offers a comprehensive evaluation of the device's performance characteristics. The SA-SDC codes are gathered as the input ramp systematically traverses the entire SA-SDC conversion range. The ascent rate of the ramp is carefully regulated to ensure multiple samplings of each SA-SDC code, typically around 20 instances in this specific experiment. Throughout this process, the ASSC gain is tuned to 'gain.1' by adjusting the synaptic weights within the ASSC, as depicted in Figure 6.3. Following this, the digital outputs produced by the SA-SDC are saved in the PL's block RAM for the whole duration of the linear ramp input.

The tests were carried out under standard conditions, maintaining a supply voltage

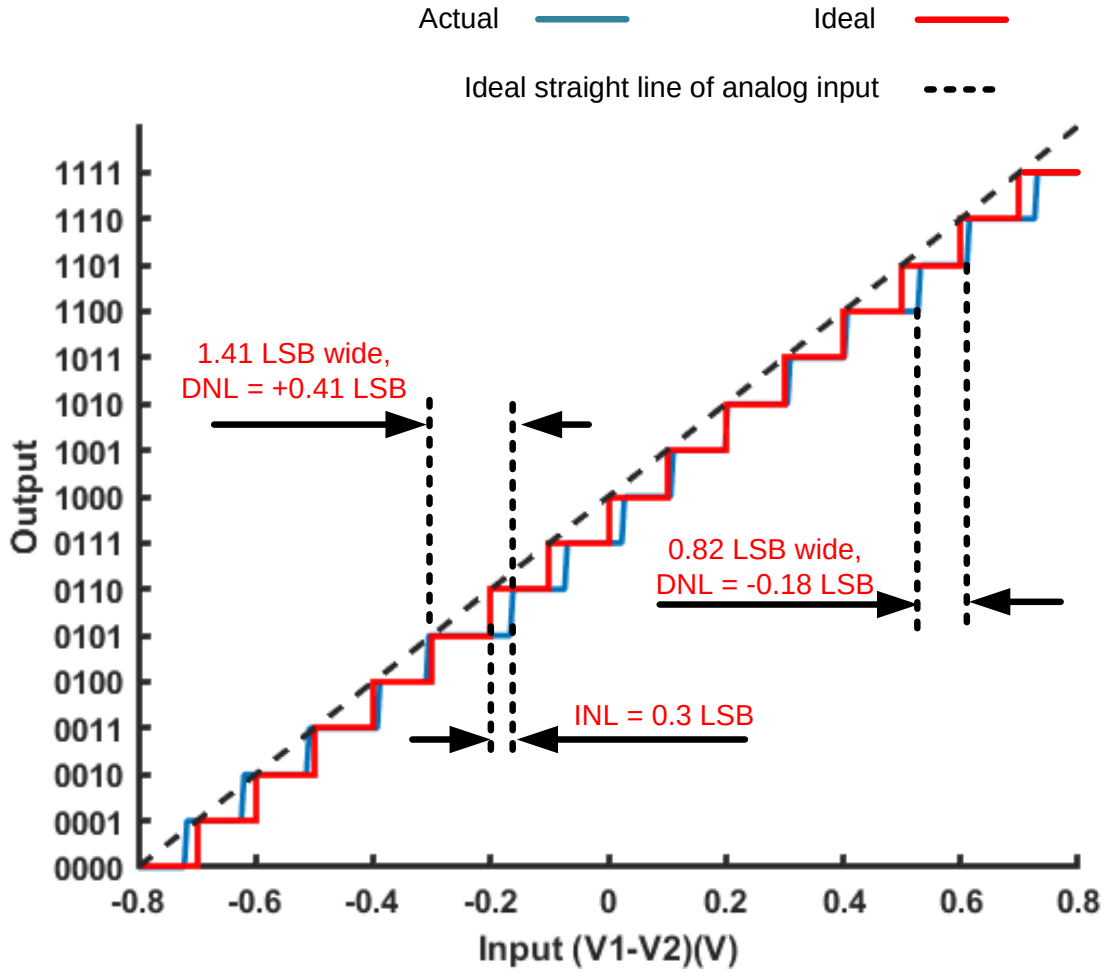


Figure 6.16: The transfer function of the neuromorphic spiking sensory system with self-X features for actual and ideal cases.

of 3.3 V and a temperature of 23°C. In Figure 6.16, the transfer function of the neuromorphic spiking sensory system during the experiment illustrates the correlation of the SA-SDC output with the voltage disparity between the input signals V1 and V2 of the ASSC along the horizontal axis. The experimental results demonstrate the SA-SDC's ability to generate 16 distinct spike order codes, efficiently representing temporal differences in its input signals and establishing a 4-bit binary encoding. The SA-SDC parameters, including INL, DNL, and the count of missing codes (NOMCs), exhibit values, with INL at 0.3, DNL at 0.41 LSB, and zero missing codes, as depicted in Figure 6.16. Additionally, Figure 6.17 presents detailed DNL and INL curves, giving a more comprehensive insight into the results presented in Figure 6.16.

The assessment of the neuromorphic spiking sensory system involves a second set of parameters that pertain to its dynamic characteristics. These metrics encompass vital

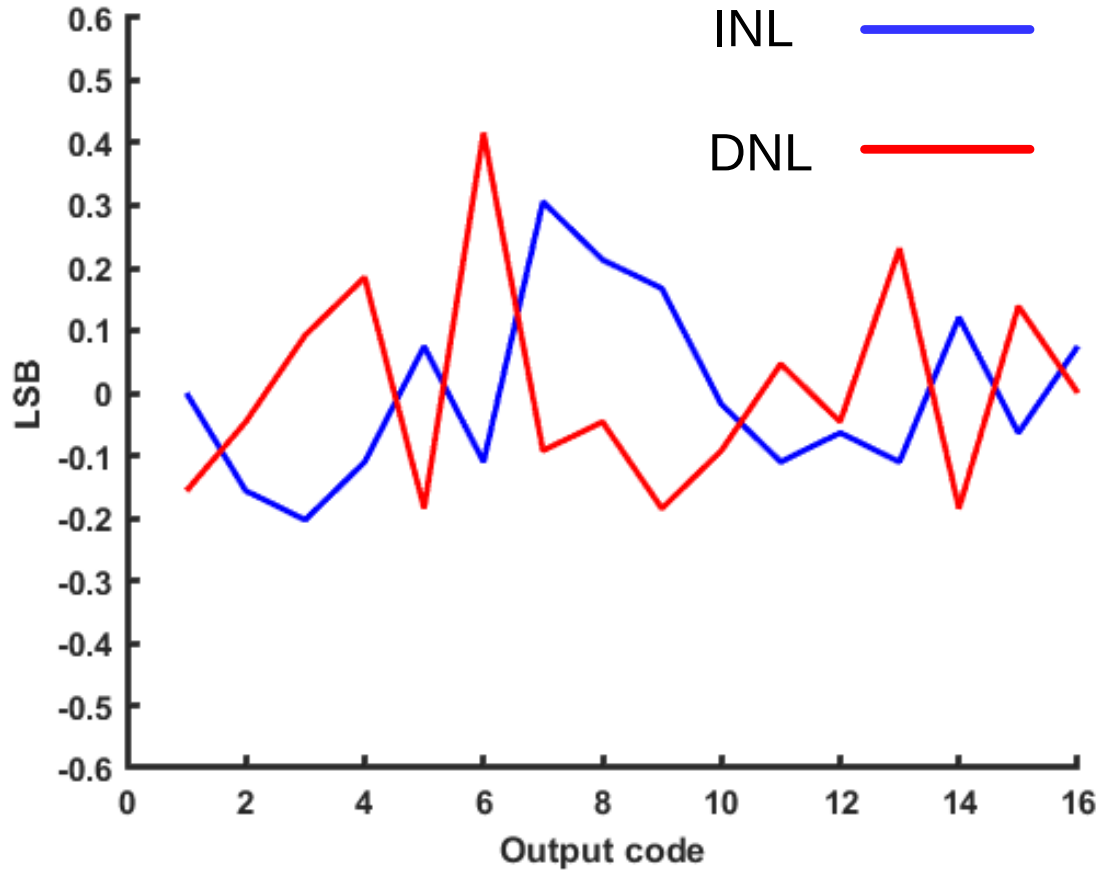


Figure 6.17: The measured DNL and INL curves align with the curve shown in Figure 6.16

aspects such as effective number of bits (ENOB) and signal-to-noise and distortion ratio (SINAD), significantly contributing to the evaluation of the system's performance. Typically, these metrics are extracted through a fast Fourier transform (FFT) analysis of the digital samples acquired from the converter's output when exposed to a sine wave input. The SINAD serves as a comprehensive metric, not solely measuring the signal-to-noise ratio but also taking into account harmonic distortion and other undesirable components present in the output of the neuromorphic spiking sensory system. It calculates the ratio between the power of the desired signal and the combined power of all unwanted elements, including noise and distortion. On the other hand, the ENOB indicates the system's performance measurement concerning its reaction to the input signal. It's essential to note that an increase in noise, particularly distortion components, leads to a decrease in the system's ENOB. These dynamic parameters play a vital role in providing a thorough insight into the system's performance and efficiency.

At the beginning, the system's performance was assessed by exposing it to a sinu-

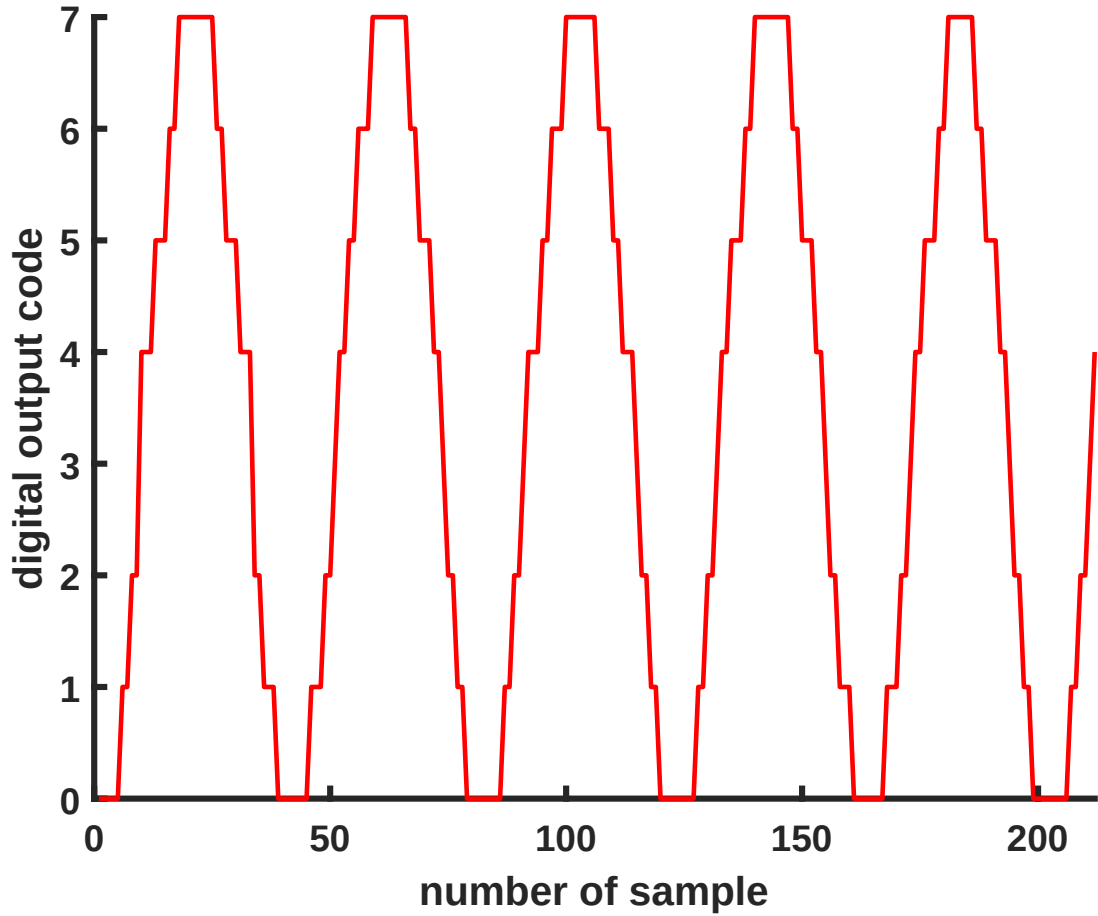


Figure 6.18: The neuromorphic spiking sensory system's response to a sinusoidal signal is analyzed, featuring a 0.8 Vp-p amplitude, 3 kHz frequency, and 0.4 V DC offset. V2 receives the input, while V1 remains at zero.

sinoidal signal with an amplitude of 0.8 Vp-p, a frequency of 3 kHz, and a DC offset of 0.4 V. The sampling frequency of the neuromorphic spiking sensory system was configured at 130 kHz, with V2 serving as the signal input and V1 being set to zero. The resultant output of the system is depicted in Figure 6.18.

In evaluating the dynamic performance, the system was subjected to fully differential sinusoidal input signals with an amplitude of 0.8 Vp-p, a frequency of 1 kHz, and a DC offset of 0.4 V applied to V1 and V2, as illustrated in Figure 6.19. The sampling frequency of the neuromorphic spiking sensory system was set at 130 kHz. The regulation of ASSC gain, indicated as 'gain_1,' involves the adjustment of synaptic weights within the ASSC, visually represented in Figure 6.3. following that, the digital outputs produced by the neuromorphic spiking sensory system are methodically saved in the PL's block RAM.

The comprehensive system output is visually depicted in Figure 6.20, where the sam-

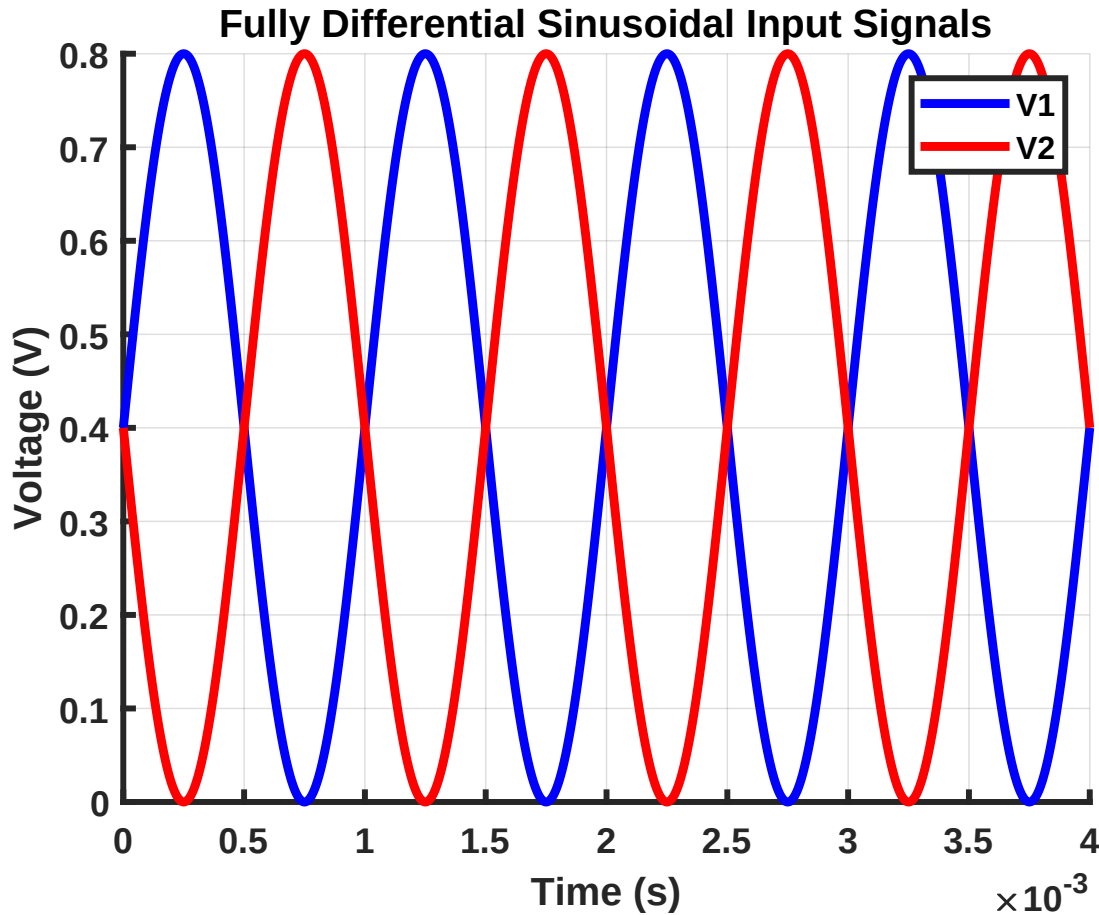


Figure 6.19: The image shows fully differential sinusoidal inputs applied to V1 and V2, with a 0.8 Vp-p amplitude, 1 kHz frequency, and 0.4 V DC offset.

ple number is represented on the x-axis, and the digital output data is indicated on the y-axis. Furthermore, Figure 6.21 offers an insight into the frequency characteristics of the output signal through the implementation of a fast Fourier transform (FFT). Dynamic parameters are extracted from the FFT analysis of the digital sample dataset. The assessment of the neuromorphic spiking sensory system's dynamic performance encompasses parameters such as SINAD and ENOB, resulting in specific values. The SINAD parameter is recorded at 24.79 dB, and ENOB is measured at 3.82 bits.

6.4 Neuromorphic System in Real-World Application

A prototype demonstration showcases the integration of a novel neuromorphic spiking sensory system with the AFF755B Tunnel Magnetoresistance (TMR) sensor from Sensitec. This setup was utilized to evaluate the performance of the adaptive spiking sensory system and the TMR sensor, as depicted in Figure 6.22. The TMR sensor features a

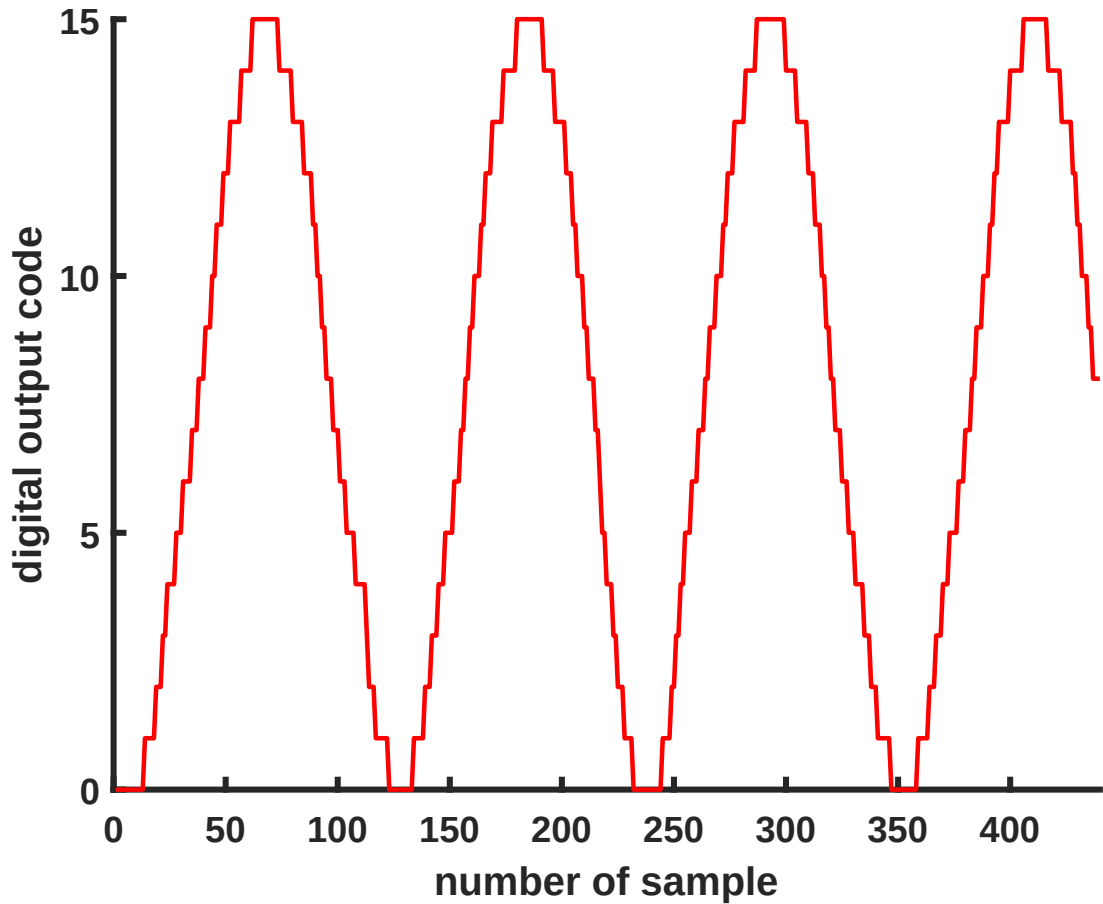


Figure 6.20: The neuromorphic spiking sensory system's response to fully differential sinusoidal inputs at V1 and V2 was analyzed, featuring a 0.8 V_{p-p} amplitude, 1 kHz frequency, and 0.4 V DC offset.

balanced, fully differential design, producing two distinct 90° phase-shifted outputs: sine and cosine signals. A block diagram of the proposed interface for the TMR sensor is provided in Figure 6.23. In the current lab setup, the hardware is configured to process a single differential signal, as shown in Figure 6.23. Future plans involve expanding the bit resolution, enabling the system to process two differential signals, and integrating these capabilities onto a single chip using cutting-edge technology. These improvements aim to refine angle measurement accuracy and position the system as a competitive alternative to current advanced solutions. At the same time, a team member is exploring the self-x concept for sensor systems across higher and multiple levels, using the angular decoder as a case study [271].

The main objective of this prototype was to verify the performance of the electrical interface in practical sensor applications, particularly in sensor signal digitization. Additionally, the focus was on the ASSC block's ability to align the sensor and SA-SDC

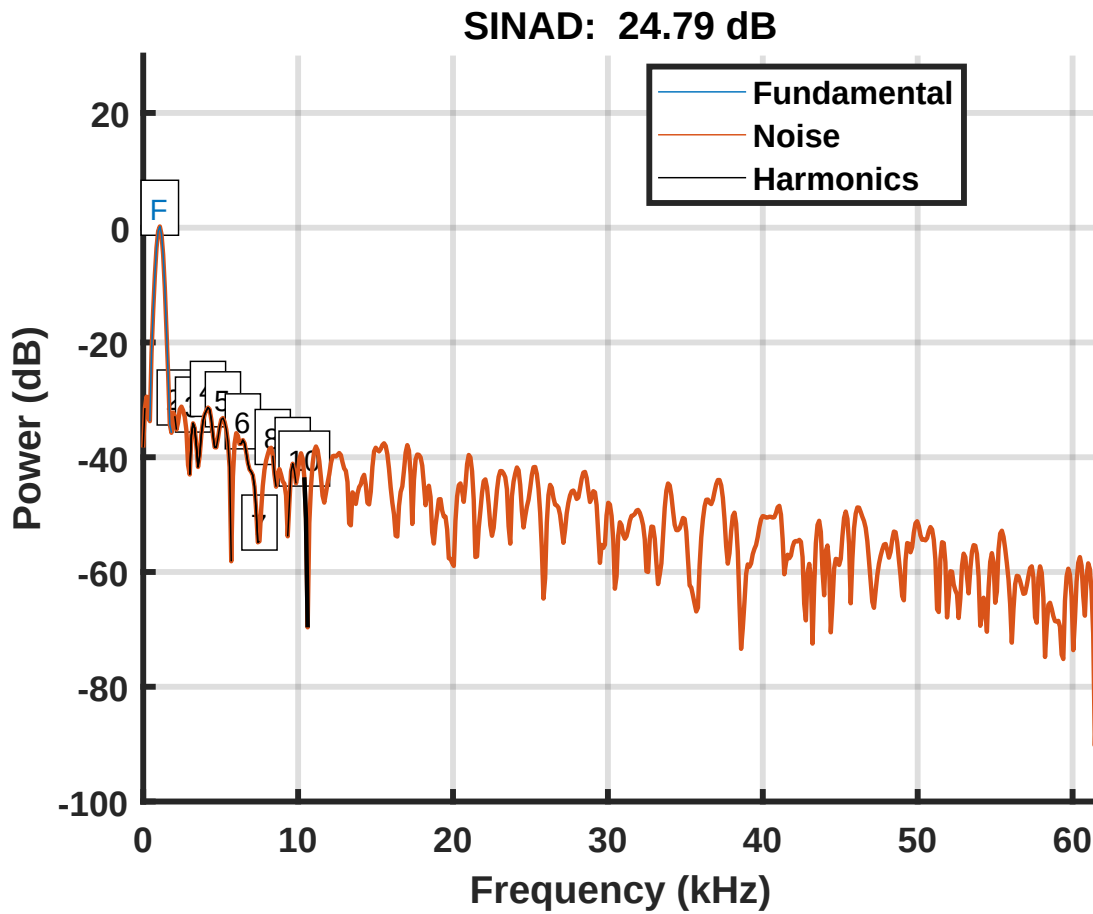


Figure 6.21: The FFT output reveals the neuromorphic spiking sensory system's response to fully differential sinusoidal inputs at V1 and V2, as shown in Figure 6.19

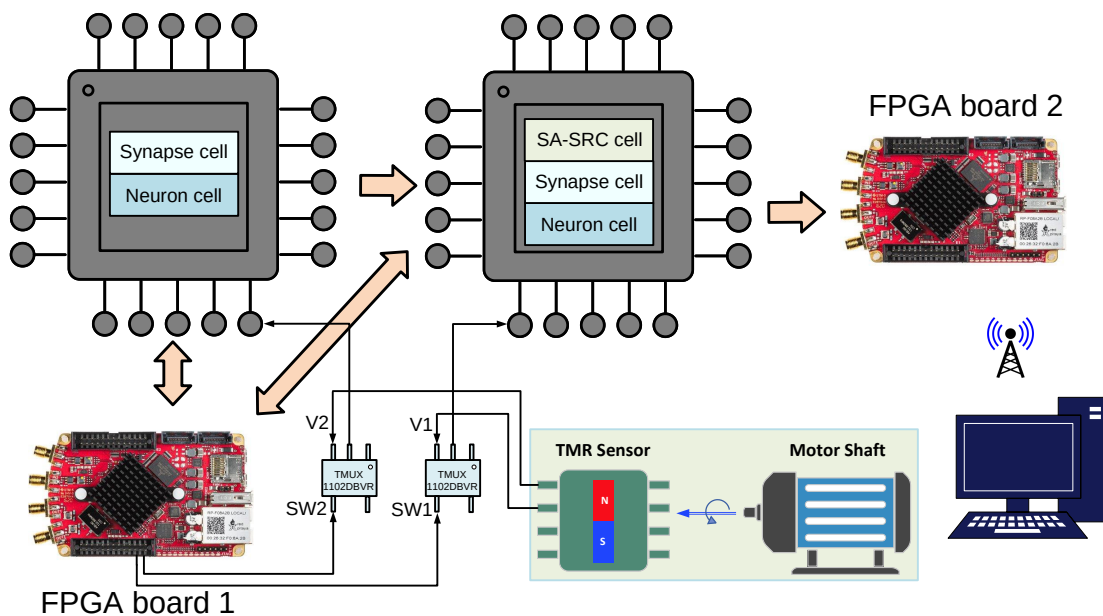


Figure 6.22: System configuration showcasing the TMR interface integration with the proposed neuromorphic spiking sensory system.

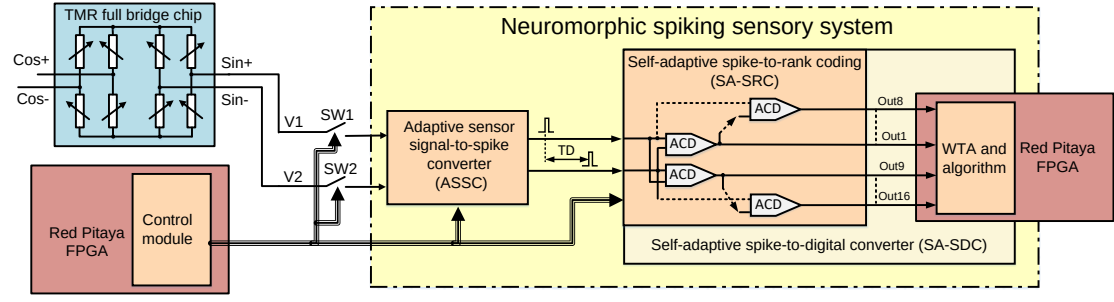


Figure 6.23: Block Diagram illustrating the TMR interface integration with the proposed neuromorphic spiking sensory system.

spans with changes in sensor signal amplitude. Figure 6.23 presents a block diagram of the proposed TMR sensor interface. The TMR sensor's outputs, $\sin+$ and $\sin-$, are connected to the ASSC inputs, labeled V1 and V2. The ASSC serves as a key conditioning circuit, aligning the spans of the sensor and SA-SDC. It efficiently amplifies and level-shifts the sensor signal in the time domain.

The magnet is attached to the front of the motor shaft, rotating as the motor operates, while the stationary PCB with the TMR sensor faces the magnet with an adjustable gap. Figure 6.24 illustrates the lab setup, highlighting its integration with the TMR sensor. The TMR sensor was initially placed 4 mm away from the magnetic detector in front of the motor shaft, producing differential outputs of approximately 0.225 Vp-p, as shown in Figure 6.25. To match the spans of the sensor and the SA-SDC, synapse weights, including offset and gain, were adjusted. In this configuration, the up-counters were set to 255, and both $vs1$ and $vs2$ were maintained at 1.8 V. The neuromorphic spiking sensory system operated at a sampling rate of 7.7 kHz, sufficient to capture the maximum frequency expected from the DC motor at full speed. The system's digital outputs were systematically stored in the PL block RAM. The overall output, illustrated in Figure 6.26, displays the sample count on the x-axis and the corresponding digital output data on the y-axis.

To overcome the channel limitation in this phase of the study, the sine bridge was first read and converted, followed by the cosine bridge. Zero crossings were manually aligned using shift operators, as shown in Figure 6.27a. These aligned signals were then used to calculate the angle using the following equation:

$$\theta = \arctan \left(\frac{2A_{\sin} \sin(\alpha + \phi) + \text{offset}_{\sin}}{2A_{\cos} \cos(\alpha) + \text{offset}_{\cos}} \right). \quad (6.1)$$

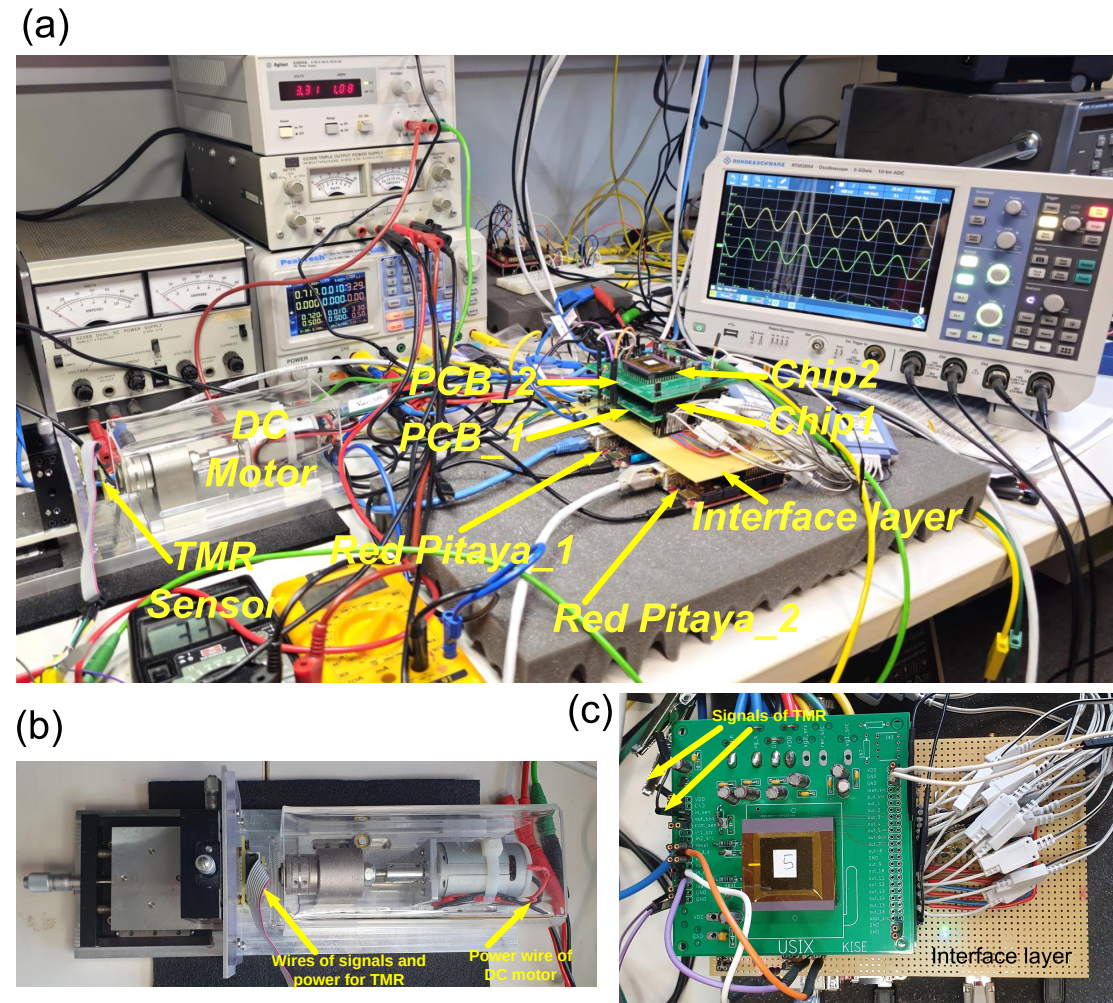


Figure 6.24: (a) Experimental setup for implementing the TMR interface with the proposed neuromorphic spiking sensory system. Figure 5.2 (c) and (d) depict the connection diagram linking Red Pitaya_1, Red Pitaya_2, PCB_1, the interface layer, and the PCB. (b) Top view layout of the TMR and DC motor. (c) Detailed top view emphasizing TMR signal connections to the neuromorphic spiking sensory system.

In this equation, θ is the measured angle, and α represents the magnet's rotational angle relative to the sensor. The terms $2A_{\sin}$ and $2A_{\cos}$ indicate the peak amplitudes of the sine and cosine signals, while ϕ accounts for the phase error between the two waveforms. $\text{Offset}_{\sin}$ and $\text{offset}_{\cos}$ represent the amplitude deviations of the sine and cosine signals, respectively.

Figure 6.27 presents the angle calculation and absolute error derived from fully differential TMR signals, with the sensor placed 4 mm away. The maximum absolute error observed in this design phase is 12.89° , determined by comparing the calculated angle to the ideal best-fit line. Due to the 4-bit ADC's limitations, the theoretical angular resolution is 360° divided into 32 steps per cycle (16 levels per half cycle), yielding a

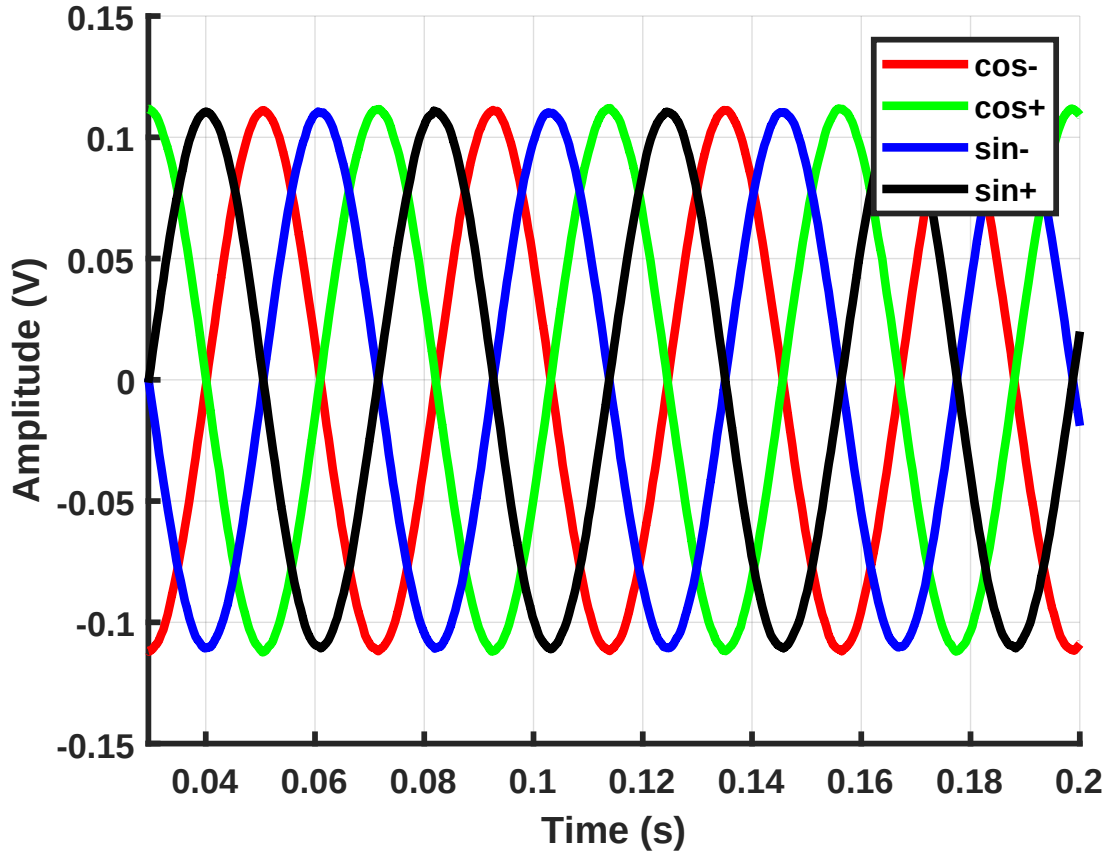


Figure 6.25: The TMR sensor outputs were captured from a 4 mm distance.

resolution error of 11.25° .

In the subsequent test, the TMR sensor was moved to a distance of 7 mm to examine how reduced signal amplitude affects angle error calculation. As shown in Figure 6.28, the sensor generated differential outputs of about 0.104 Vp-p. The ASSC synapse weights remained unchanged, with up-counters set to 255 and vs1 and vs2 at 1.8 V. Figure 6.29 depicts the angle calculations and absolute error for this configuration, with a maximum deviation of 24.95° . Experimental results revealed that the TMR signals introduced time delays in the ASSC outputs, labelled as out1 and out2, varying between -55 ns and +55 ns. This range did not fully encompass the input conversion spectrum of the SA-SRC. Within this delay range, the SA-SRC cell produced eight distinct spike-order codes, representing a 3-bit binary encoding of the data, as illustrated in Figure 6.29. The synapse weights of the ASSC were adjusted to match the spans of the sensor and SA-SDC, enabling full utilization of the SA-SRC's input conversion range. In this configuration, the upper counters were set to 255, and vs1 and vs2 were increased to 2.1 V. The neuromorphic spiking sensory system maintained a sampling rate of 7.7

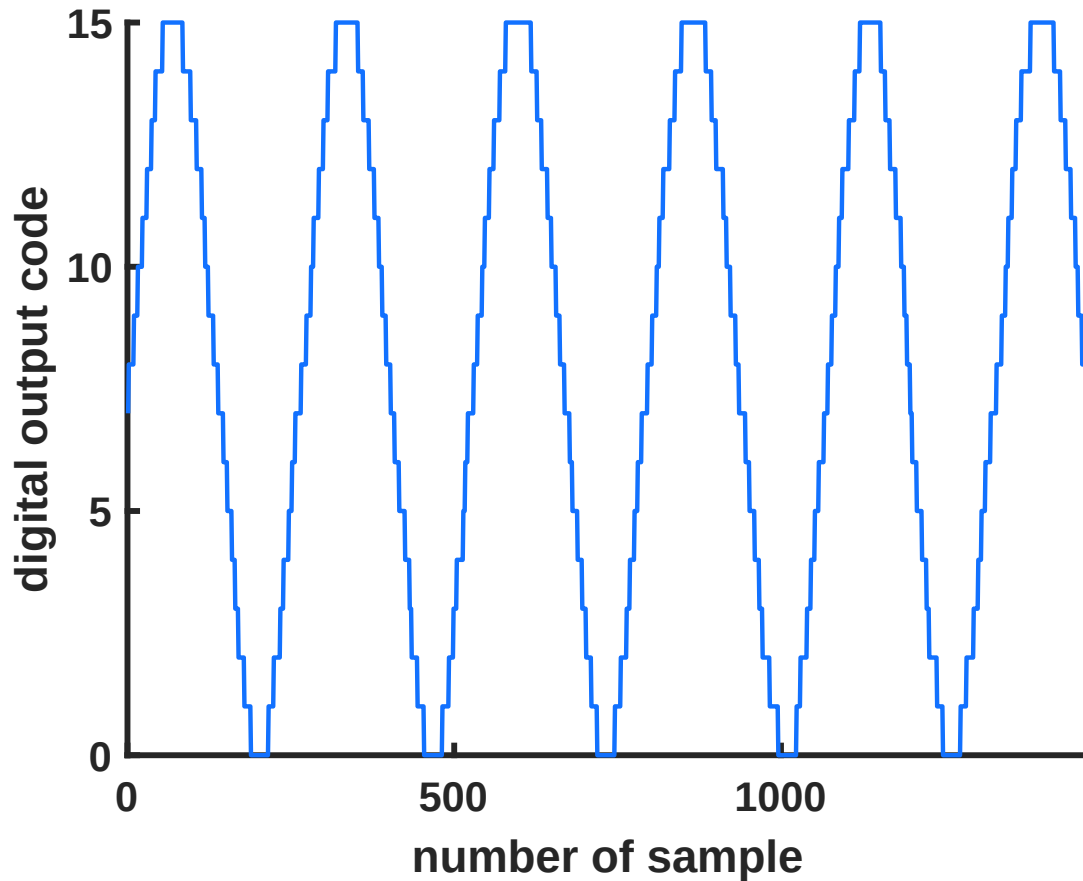


Figure 6.26: The neuromorphic spiking sensory system’s functionality was tested by applying the TMR sensor’s differential outputs to V1 and V2, with recordings taken at a 4 mm sensor distance.

kHz. After these adjustments, the TMR signals caused temporal delays in the ASSC outputs, ranging from -120 ns to +120 ns, fully covering the SA-SRC’s input conversion range. Within this interval, the SA-SRC cell generated 16 unique spike-order codes, corresponding to a 4-bit binary data representation. Figure 6.30a displays the system output, with the sample number on the x-axis and digital output data on the y-axis. After adjusting the ASSC synapse weights to align the sensor and SA-SDC spans, the angle calculations and overall errors with the TMR sensor placed 7 mm away are shown in Figure 6.30. The maximum absolute error observed is 12.72°.

The results with the sensor placed 4 mm and 7 mm from the magnetic detector confirm the system’s ability to digitize the sensor signal effectively. They also demonstrate the ASSC block’s role in aligning the sensor with the SA-SDC block. Notably, the SA-SDC hardware, utilizing its full 4-bit capacity, was fully employed in both cases. Additionally, the system showcased its adaptability by reducing the angle measurement

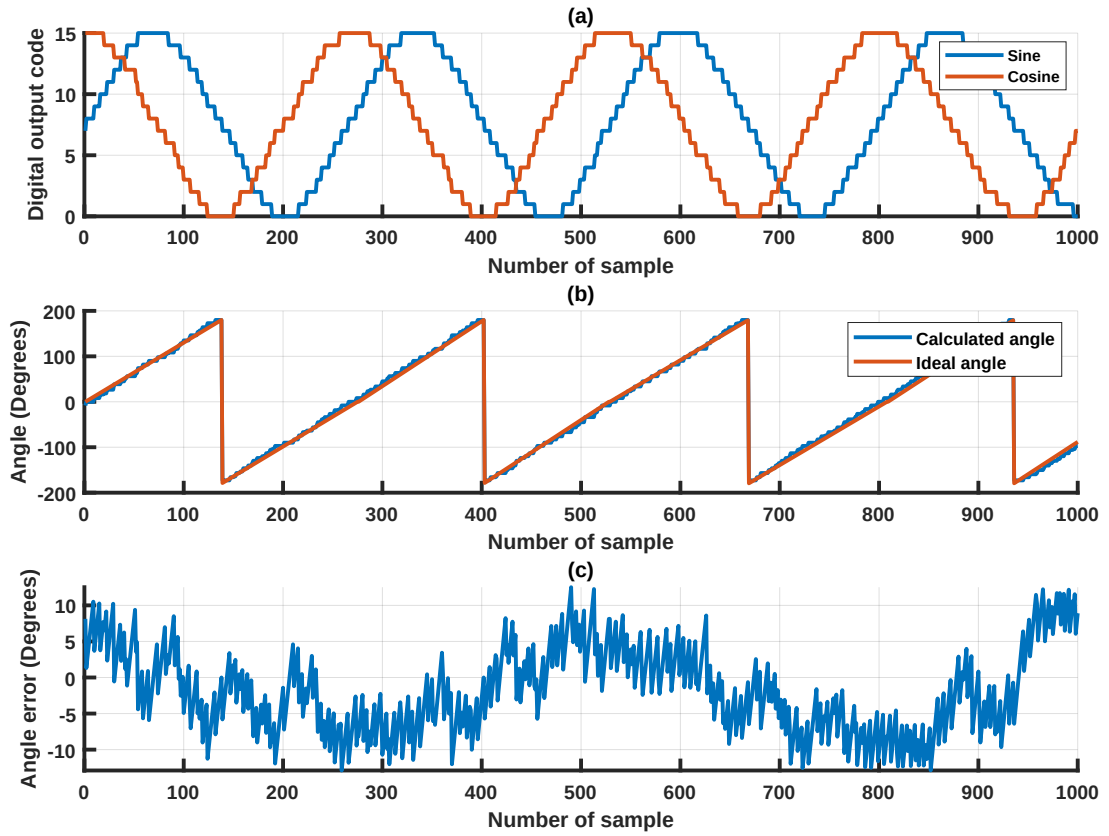


Figure 6.27: Angle calculation with a TMR sensor placed 4 mm from the motor shaft: (a) Differential sine and cosine signals. (b) Comparison of computed and ideal angles. (c) Absolute error analysis in measurement.

error from 24.95° to 12.72° throughout this phase of the study.

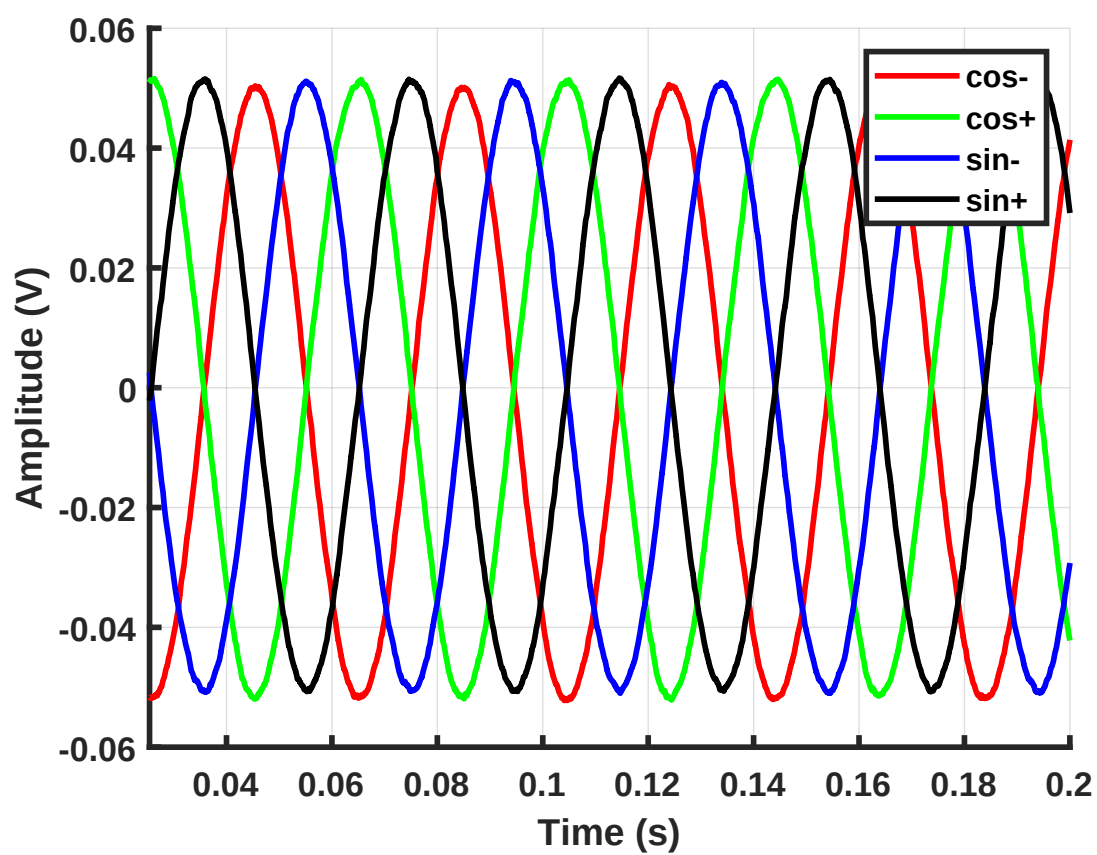


Figure 6.28: The TMR sensor outputs were captured from a 7 mm distance.

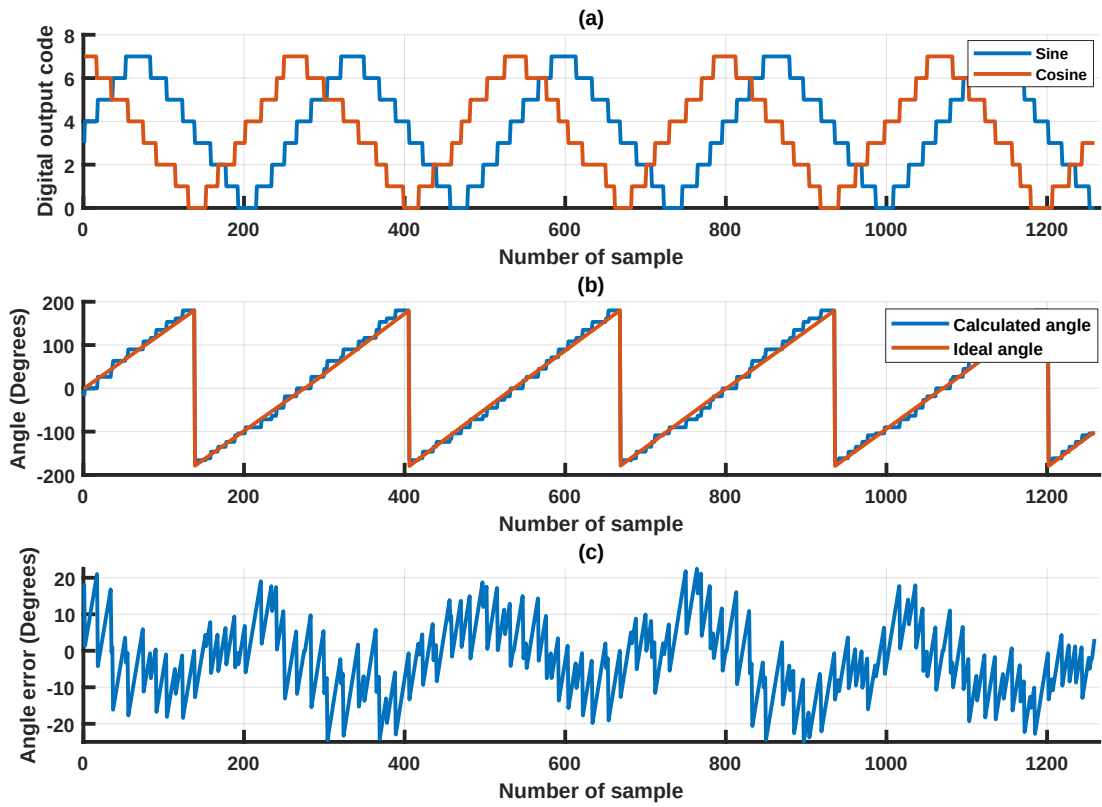


Figure 6.29: Angle calculation was conducted using a TMR sensor placed 7 mm from the motor shaft, maintaining the ASSC synapse weights from the 4 mm setup. The up counters were set to 255, with vs1 and vs2 at 1.8 V. (a) Differential sine and cosine signals. (b) Comparison of computed and ideal angles. (c) Absolute error analysis in measurement.

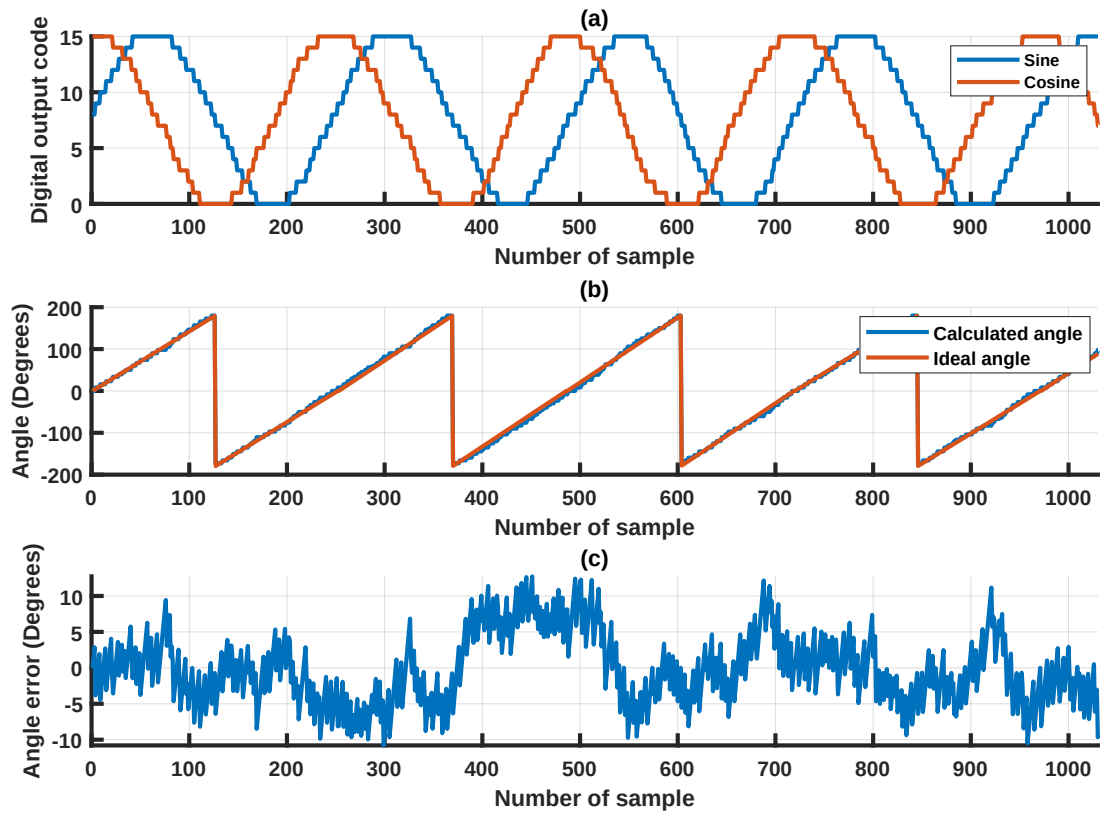


Figure 6.30: Angle calculation using a TMR sensor placed 7 mm from the motor shaft, with adjusted ASSC synapse weights, up counters set to 255, and vs1 and vs2 at 2.1 V. (a) Differential sine and cosine signals, (b) comparison of computed and ideal angles, and (c) Absolute error analysis in measurement.

Chapter 7

Conclusions

This thesis has presented a Neuromorphic Spiking Sensory System with Self-X Capabilities, designed to address the challenges of modern CMOS technologies while meeting the demands of Industry 4.0 and other advanced applications. Guided by the research goals outlined in the introduction, the system was developed as an integrated solution combining the Adaptive Sensor Signal-to-Spike Converter (ASSC) and the Self-Adaptive Spike-to-Digital Converter (SA-SDC). This chapter evaluates the outcomes of the research goals, highlights the novelties and contributions of the system, and outlines directions for future work.

7.1 Development of a Robust and Technology-Agnostic Signal Interface System

The objective of creating a robust and adaptable signal interface system that remains effective across diverse technological platforms was achieved to a significant extent. The ASSC, a central component of the system, demonstrated its capability to transform analog sensor inputs into spike timings. This approach eliminates the need for conventional amplitude-based signal processing methods, offering a compact and scalable alternative.

Through its adjustable synaptic weights and ability to perform gain and span alignment within the time domain, the ASSC successfully addresses challenges related to shrinking CMOS node dimensions and variability in manufacturing processes. Experimental results validated its effectiveness in maintaining functionality under process, voltage, and temperature (PVT) variations.

The SA-SDC further complements the ASSC by converting spike-order information into digital representations. Using rank-order coding and winner-take-all mechanisms, the SA-SDC demonstrated increased robustness and technology-agnostic behavior compared to amplitude-domain approaches. The current limited demonstrator provides initial evidence of the efficacy of this approach on a small scale. The combination of the ASSC and SA-SDC demonstrated the system's robustness, making it suitable for diverse applications such as industrial automation, healthcare devices, and robotics. To increase the number of bits, the number of ACDs must be increased accordingly. The required number of ACDs can be determined using Equation 4.9. For an 8-bit resolution, 256 ACDs are required, each occupying an area of $0.336 \text{ mm} \times 0.123 \text{ mm}$, resulting in a total area of 10.58 mm^2 . The area is calculated by multiplying the number of ACDs by the area of ACD. To provide a meaningful evaluation, the ADC size is compared against other ADCs with similar specifications, specifically an 8-bit resolution and a $0.35 \text{ }\mu\text{m}$ technology node. For reference, the ADC presented in [75] occupies an area of 8.5 mm^2 .

7.2 Adaptation of Natural Neural Coding Principles

The system effectively integrates principles of natural neural coding, specifically time-based spike processing inspired by biological systems. Drawing insights from the remarkable sensory adaptability observed in living organisms, this design emulates biological mechanisms such as interaural time differences (ITDs) for processing temporal disparities and transforming them into spatial representations. The Neuromorphic Spiking Sensory System leverages these principles to adapt dynamically to environmental changes and operational variations. A central aspect of this biological inspiration is the utilization of spiking neural networks (SNNs) modeled after foundational theories such as Jeffress' framework for auditory localization. The system adapts these concepts not merely to replicate natural mechanisms but to extend their application into novel domains. The first stage of the system, the Adaptive Sensor Signal-to-Spike Converter (ASSC), translates incoming analog signals into spike pairs with measurable time differences (TDs). This transformation is pivotal for ensuring the accurate encoding of sensory information. The second stage, the Self-Adaptive Spike-to-Digital Converter (SA-SDC), further exemplifies the integration of neural coding principles. Drawing on Jeffress' three as-

sumptions, the SA-SDC employs an array of adaptive coincidence detectors (ACDs) to interpret spike time differences, converting these temporal disparities into rank-ordered spike codes. The current SA-SRC cell on-chip features 16 outputs represented by sparse rank-coded spikes, which can be read from the chip. Implementing an ADC with 8 or more bits would produce 2^{bits} outputs, exceeding the chip's simplicity. To digitally convert the rank-order code outputs and interface with conventional computing systems, this research developed a WTA (Winner-Take-All) circuit and algorithm using Verilog. The WTA circuit was chosen as it extracts the rank information from the sparse spike codes, providing a bridge between the neuromorphic output and the denser codes required for conventional digital processing. Incorporating self-calibration and self-compensation mechanisms enhances the system's ability to maintain performance over its lifecycle. These features mitigate the effects of aging, drift, and external disturbances, ensuring operational stability under varying conditions. This biologically inspired design is particularly well-suited for applications in noisy or variable environments, such as autonomous systems, wearable devices, and robotics, where consistent performance is critical. Moreover, the integration of time-domain coding principles enables the system to operate effectively across different environmental conditions. By leveraging spike-timing mechanisms, the system achieves a balance between energy efficiency and signal precision, aligning with the demands of modern applications. This adaptation underscores the novelty of the design, which moves beyond emulation of biological systems to introduce a versatile framework applicable to dynamic technological landscapes. Experimental results further validate the system's ability to process sensory inputs inspired by biological auditory mechanisms. When paired with Tunnel Magnetoresistance (TMR) sensors, the system demonstrated its capacity to handle temporal disparities effectively, achieving signal digitization and alignment. The interplay between the ASSC and SA-SDC that biologically inspired coding principles are not only implemented but optimized for real-world applications, showcasing the resilience and adaptability of the design. By emulating the adaptability of natural neural networks and advancing these principles into engineered systems, the Neuromorphic Spiking Sensory System establishes itself as a robust and biologically inspired solution. It bridges the gap between theoretical neuroscience and practical applications, aligning with the stringent requirements of industrial, healthcare, and autonomous technologies.

7.3 Implementation of Self-X Capabilities

The development of self-X functionalities including self-calibration, self-repair, and self-optimization represents a key contribution of this thesis. These features enable the system to autonomously adjust to process, voltage, and temperature (PVT) variations, ensuring long-term reliability and adaptability. It is important to highlight that a key feature of the SAFEX approach is its ability to leverage manufacturing processes to achieve built-in corrections and continuous adaptation, increasing yield without requiring labor-intensive 'pick-and-place' operations for individual calibration or trimming. This process occurs automatically throughout the circuit's operation and life cycle, significantly reducing effort and production costs associated with manual interventions.

Furthermore, the system's intrinsic self-adaptation at the hardware level directly contributes to yield improvement by compensating for process variations. Unlike traditional methods that rely on external recalibration steps, the SAFEX system's ability to self-optimize ensures that performance metrics, such as Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), remain within acceptable ranges without additional human intervention. This not only enhances reliability but also lowers manufacturing complexity and cost by minimizing post-fabrication adjustments.

Experimental evaluations confirmed the effectiveness of self-X capabilities in scenarios involving Tunnel Magnetoresistance (TMR) sensors. The system demonstrated the ability to align sensor spans with the ASSC and SA-SDC, achieving digitization of analog signals. The adaptability of the system was evident in its ability to minimize errors and maintain performance across varying signal amplitudes and environmental conditions.

An evaluation of the SA-SRC's performance was conducted to identify any missing codes, as well as to assess the Differential Non-Linearity (DNL), Integral Non-Linearity (INL), and transfer functions. The tests were performed with power supply levels varying from 3.3 V to 3 V, and at ambient temperatures of 22 °C and 29.9 °C. The results revealed the presence of four missing codes (NOMC), indicating data gaps at specific steps. The DNL and INL measurements were recorded at 0.6 and 2.07 LSB, respectively. However, the automatic adaptation mechanism in the first layer successfully mitigated these discrepancies, eliminating missing codes and reducing the DNL and INL values to 0.34 and 0.53 LSB, respectively. This adaptive feature effectively stabilized performance

across the tests conducted under these conditions for chips 4, 5, and 6.

Additional tests were conducted by varying the power supply from 3.3 V down to 2.4 V. These tests revealed the presence of eight missing codes (NOMC), with DNL and INL values recorded at 1.53 and 4.4 LSB, respectively. To address these deviations, the variables $vg1$, $vg2$, and V_{RFR} were adjusted through an iterative tuning process. Specifically, $vg1$ and $vg2$ were incrementally varied in steps of 0.1 V within the range of 0 V to 2.3 V, while V_{RFR} was adjusted in steps of 0.01 V within the range of 0.65 V to 0.82 V. After each adjustment, the first layer's automatic adaptation mechanism was activated, and the resulting missing codes, Differential Non-Linearity (DNL), and Integral Non-Linearity (INL) values were evaluated. The process involved continuous iterations where voltages were modified, followed by first-layer adaptation and assessment of NOMC, DNL, and INL values. This loop repeated until the missing codes were eliminated and both DNL and INL were minimized. Ultimately, the values were determined to be 0.6 V for $vg1$, 0 V for $vg2$, and 0.74 V for V_{RFR} . Following this adjustment process, the SA-SRC parameters confirmed the elimination of missing codes (NOMC), with improved DNL and INL values of 0.4 and 0.46 LSB, respectively. The optimization of the three voltages was performed using a grid search approach. This method systematically explored a range of values for each voltage, testing possible combinations to identify the set of voltages that minimized the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) metrics. Additionally, the optimization was conducted at the hardware level, specifically on the chip and system (intrinsic) [270]. The adjustments and evaluations were performed directly on the physical hardware, focusing on chips 4, 5, and 6.

Looking ahead, to fully automate this adjustment process, future iterations will focus on integrating a feedback loop based on quality thresholds. The optimization unit will be designed to check for sufficiently satisfying results by continuously monitoring missing codes, DNL, and INL. The optimization criterion will prioritize the elimination of missing codes (NOMC) as a primary indicator of performance, while also ensuring that DNL and INL are minimized within acceptable limits. This feedback loop will enable the system to detect when first-layer adaptation alone is insufficient for instance, under reduced supply voltages and dynamically modify $vg1$, $vg2$, and V_{RFR} . The system will iterate these adjustments until the performance metrics meet the predefined thresholds. Such

an approach will streamline calibration, ensuring efficient and adaptive optimization without manual intervention, while maintaining a clear focus on the quality of results through the elimination of missing codes and the optimization of DNL and INL.

From these measurements, it was observed that minor changes, such as a power shift from 3.3 V to 3 V or a temperature variation from 22 °C to 29.9 °C, were effectively handled by the first layer. However, more significant changes, like a power shift from 3.3 V to 2.4 V, required the involvement of the second adaptation layer through adjustments to v_{g1} , v_{g2} , and V_{RFR} . This test was done for chips 4, 5, and 6.

7.4 Enhancement of Power Efficiency

The system achieves a balance between performance and energy consumption, primarily through its implementation of time-coded signal processing. This approach leverages the inherent advantages of spike-timing mechanisms, where information is encoded in the temporal patterns of spikes rather than their amplitude. By adopting this time-domain methodology, the system circumvents the high power demands typically associated with amplitude-based signal processing, enabling efficient operation across a range of applications.

Converting continuous input signals into pulse frequencies by utilizing a significant array of spikes may lead to escalated energy usage, particularly in extensive and complex spiking neural network (SNN) architectures. This increased energy demand is incompatible with the requirements of power-efficient and resilient devices, particularly in edge computing scenarios. To address this challenge, the neuromorphic spiking sensory system adopts spike-based or time-coded signals that significantly reduce the number of spikes utilized during operation.

A key contributor to this energy efficiency is the Adaptive Sensor Signal-to-Spike Converter (ASSC). The ASSC minimizes the number of spikes generated during signal transformation, reducing the computational burden on subsequent processing stages. By dynamically adjusting synaptic weights and optimizing signal spans in the time domain, the ASSC ensures spike timing while avoiding unnecessary spikes, directly contributing to reduced energy usage. This capability is particularly advantageous in scenarios where power resources are constrained, such as IoT edge devices, wearable electronics, and

autonomous systems.

The system's energy conscious design aligns with modern demands for both high performance and low power consumption. This balance is achieved without compromising the accuracy or adaptability of the sensory interface, ensuring its relevance for a broad range of real-world applications.

7.5 Future Work

1. The SAFEX system is designed with two levels of adaptivity to enhance performance under varying conditions. The first level features an automatic adaptation mechanism that effectively compensates for fluctuations in power supply levels ranging from 3.3 V to 3.0 V and ambient temperatures between 22 °C and 29.9 °C, as demonstrated in chip tests. When the power supply varies from 3.3 V down to 2.4 V, adjustments to the variables $vg1$, $vg2$, and V_{RFR} are required to maintain stable operation. In the current design phase, these adjustments are performed by incrementally tuning $vg1$ and $vg2$ in steps of 0.1 V within the range of 0 V to 2.3 V, and V_{RFR} in steps of 0.01 V within the range of 0.65 V to 0.82 V. For every adjustment, the missing codes, Differential Non-Linearity (DNL), and Integral Non-Linearity (INL) values are evaluated until the missing codes are eliminated and both DNL and INL are minimized. Based on these results, it was determined that the voltage ranges of $vg1$, $vg2$, and V_{RFR} can be effectively controlled using a 5-bit Neural DAC [272]. The second level of adaptivity involves an optimization unit working in conjunction with the 5-bit Neural DAC, as illustrated in Figure 7.1. The SAFEX output will serve as the cost or fitness function for the optimization unit, which will assess the missing codes, DNL, and INL values. The three variables ($vg1$, $vg2$, and V_{RFR}) will act as tuning parameters for the optimization process, continuously adjusting to eliminate missing codes and minimize DNL and INL, ensuring SAFEX achieves its desired output. Furthermore, the optimization unit will predict new values for these three variables based on the device's operating conditions.
2. Multi-Sensor Integration: Expanding the system to process signals from multiple sensors concurrently will enhance its functionality in complex applications, such

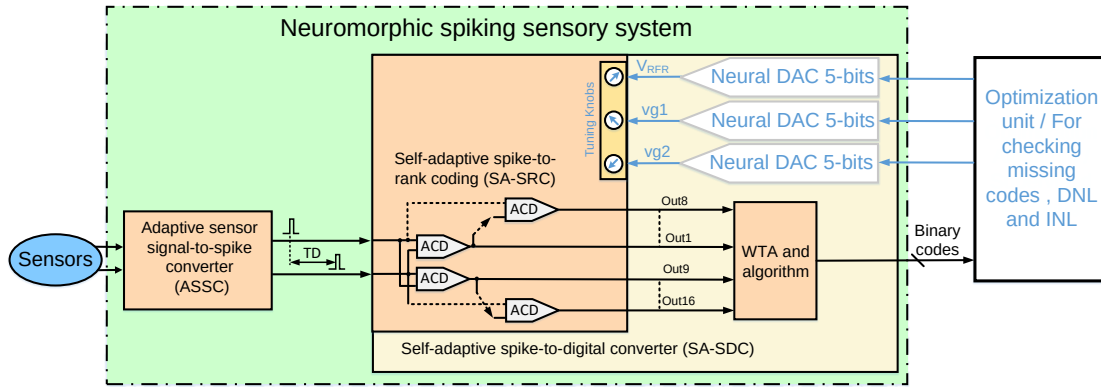


Figure 7.1: The Neuromorphic Spiking Sensory System, or SAFEX, incorporates a proposed second level of adaptivity, combined with an optimization unit working alongside the 5-bit Neural DAC.

as autonomous systems and robotics. Multi-sensor configurations would allow the system to provide richer data for decision making processes in dynamic environments.

3. Improved Resolution and Efficiency: Increasing the resolution of the SA-SDC and further optimizing its power consumption will enable the system to function effectively in resource constrained environments. This would enhance its suitability for IoT applications and edge computing devices.
4. Integration with Emerging Technologies: Exploring compatibility with advanced materials, such as memristors, and new CMOS technologies will open opportunities for further innovation in neuromorphic sensory systems. Such advancements could improve the system's scalability and efficiency.
5. Enhanced Real-World Applications: Future efforts should focus on testing the system in broader real-world applications, such as industrial automation, autonomous vehicles, and medical devices, to validate its performance and identify additional areas for improvement.

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Appendix A

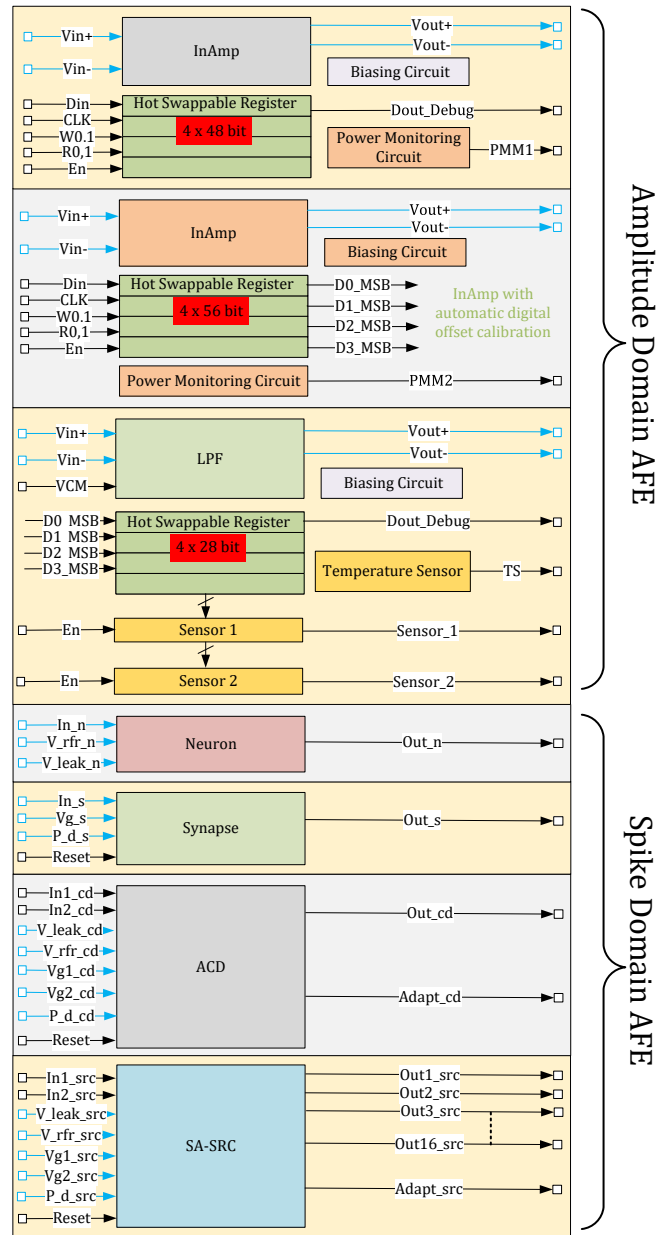


Figure A.1: Simplified chip block diagram featuring the custom Amplitude Domain AFE and Spike Domain AFE.

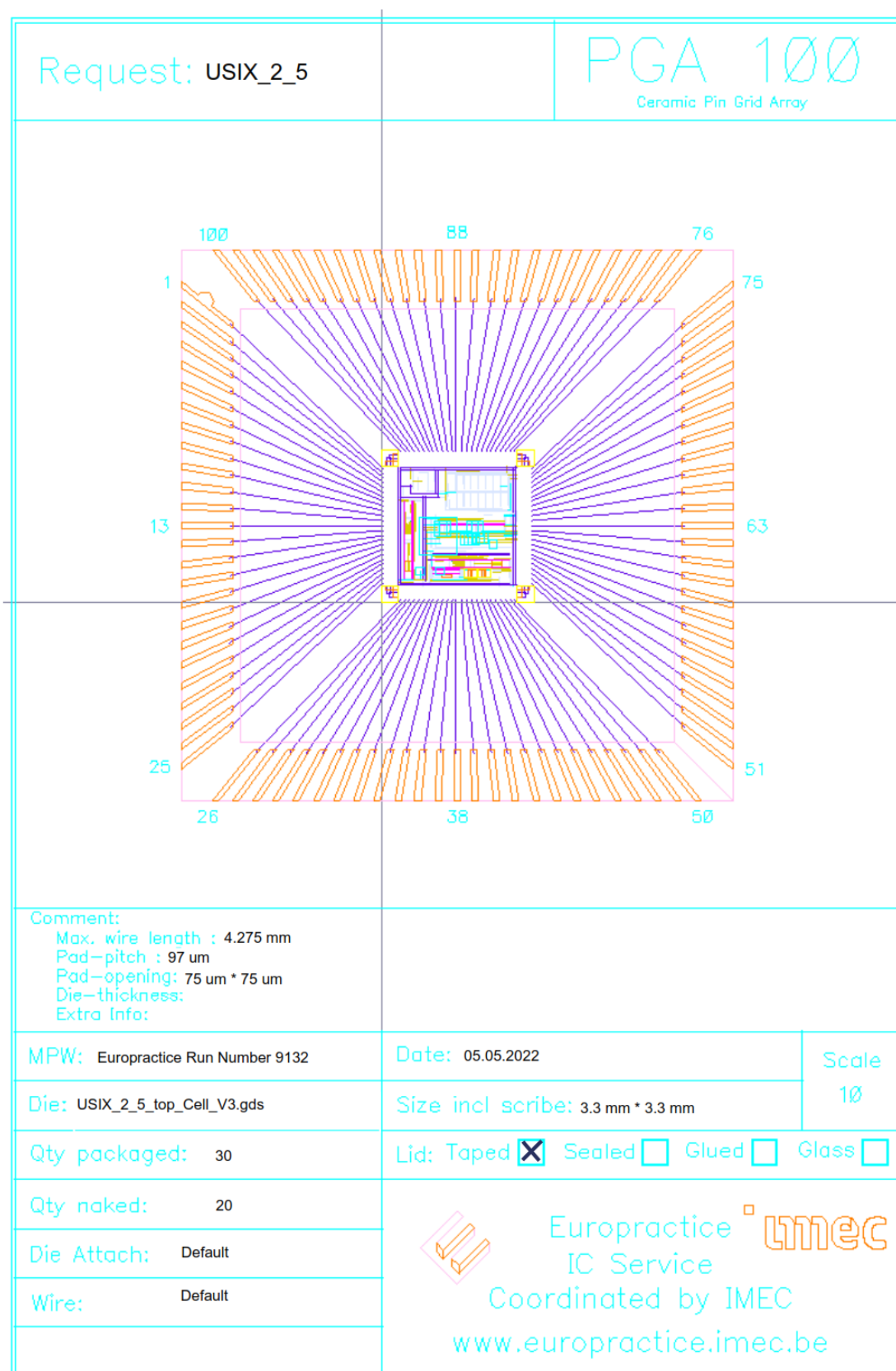


Figure A.2: Chip bonding layout with a CPGA100 package, manufactured through the Europractice program.

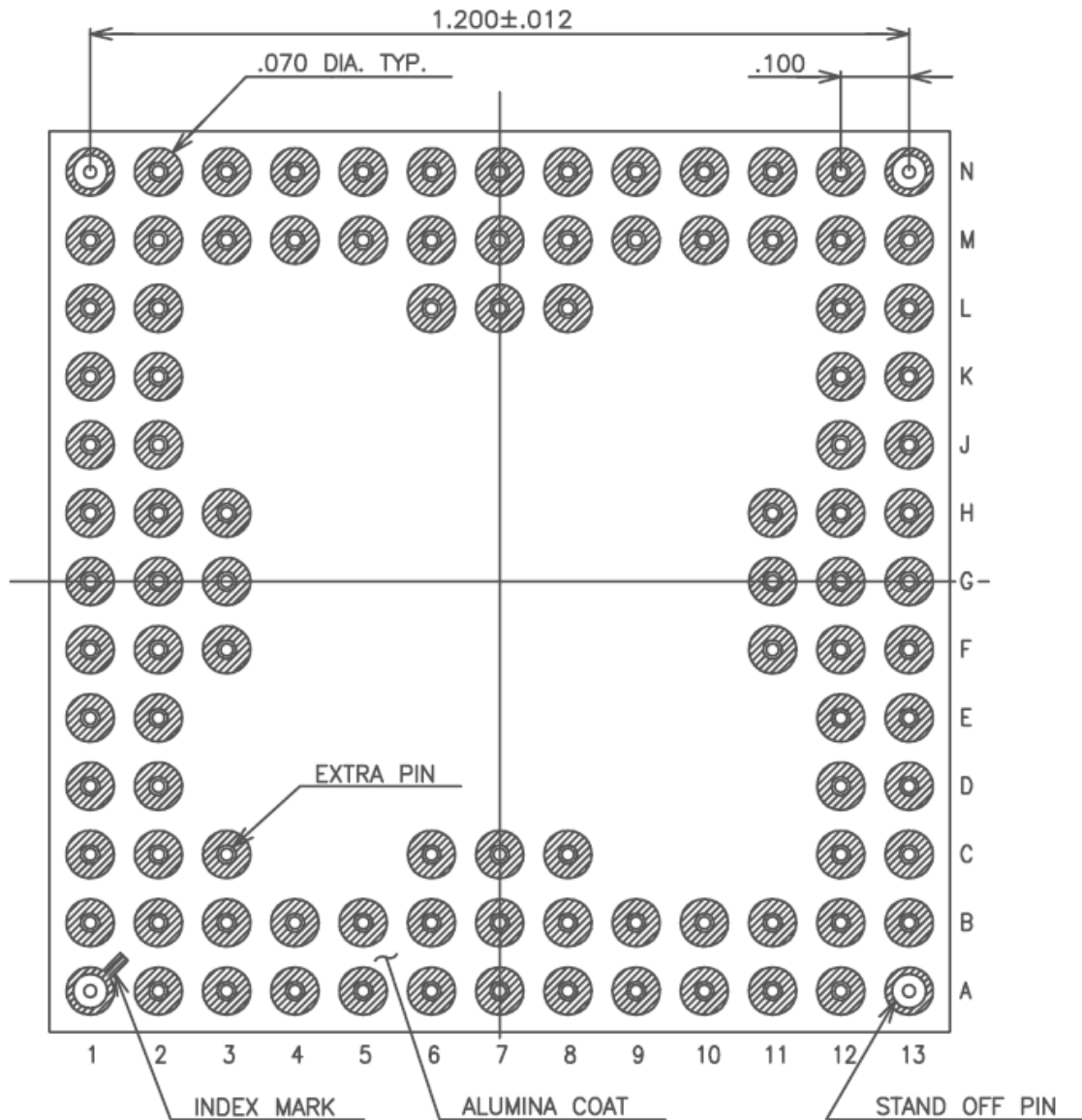


Figure A.3: The chip index layout of a CPGA100 package.

Neuron			
Nr. On Chip (PAD)	Chip index	Name	Description
5	D2	In_n	This is the input of the neuron. The pulse current can range from 500 nA to 1.38 mA.
6	D1	V_rfr_n	This is the refractory voltage of the neuron, which can range from 0.4 V to 1.5 V.
7	E2	V_leak_n	This is the leakage voltage, which can range from 0.3 V to 0.9 V.
8	E1	Out_n	This is the output of the neuron.
88	C7	Vdd!	This is the power pin used for the cell.
89	A7	VDDOR2	This is the power pin used for the pad.
90	A6	gnd!	This is the ground pin for the cell.

Figure A.4: The pin list of the neuron cell and its description..

Synapse			
Nr. On Chip (PAD)	Chip index	Name	Description
2	B1	In_s	The input of the synapse
3	C2	Vg_s	This is the voltage of the synapse, which is used as a second level of adaptation. It can range from 0 V to 2.2 V.
1	B2	p_d_s	This pin is the clock of the counter in the synapse.
91	B6	Reset	This is the reset pin. It resets the counter by applying a pulse with a width of 30 ns.
4	C1	Out_s	This is the output of the synapse.
88	C7	Vdd!	This is the power pin used for the cell.
89	A7	VDDOR2	This is the power pin used for the pad.
90	A6	gnd!	This is the ground pin for the cell.

Figure A.5: The pin list of the synapse cell and its description..

ACD			
Nr. On Chip (PAD)	Chip index	Name	Description
99	B3	In1_cd	The first input of the ACD
100	A1	In2_cd	The second input of the ACD
94	B5	Vg1_cd	This is the voltage of the first synapse of the ACD, which serves as a second level of adaptation. It can range from 0 V to 2.2 V.
92	C6	Vg2_cd	This is the voltage of the second synapse of the ACD, which serves as a second level of adaptation. It can range from 0 V to 2.2 V.
93	A5	V_rfr_cd	This is the refractory voltage of the neuron, which can range from 0.4 V to 1.5 V.
95	A4	V_leak_cd	This is the leakage voltage, which can range from 0.3 V to 0.9 V.
98	A2	Adapt_cd	The Adapt_cd signal reflects ACD self-adaptation status, with 0 indicating active adaptation.
97	A3	p_d_cd	Weights are adapted using the p_d_cd input, which has a 30 ns pulse width.
35	B6	Reset	This is the reset pin. It resets the counter by applying a pulse with a width of 30 ns.
96	B4	Out_cd	This is the output of the ACD.
88	C7	Vdd!	This is the power pin used for the cell.
89	A7	VDDOR2	This is the power pin used for the pad.
90	A6	gnd!	This is the ground pin for the cell.

Figure A.6: The pin list of the ACD cell and its description..

SA-SRC			
Nr. On Chip (PAD)	Chip index	Name	Description
86	A8	In1_src	The first input of the SA-SRC
87	B6	In2_src	The second input of the SA-SRC
77	A12	Vg1_src	This is the voltage of the first synapse of the ACD, which serves as a second level of adaptation. It can range from 0 V to 2.2 V.
80	B10	Vg2_src	This is the voltage of the second synapse of the ACD, which serves as a second level of adaptation. It can range from 0 V to 2.2 V.
76	B12	V_rfr_src	This is the refractory voltage of the neuron, which can range from 0.4 V to 1.5 V.
75	A13	V_leak_src	This is the leakage voltage, which can range from 0.3 V to 0.9 V.
64	G13	Adapt_src	The Adapt_cd signal reflects ACD self-adaptation status, with 0 indicating active adaptation.
73	B13	p_d_src	Weights are adapted using the p_d_src input, which has a 30 ns pulse width.
35	B6	Reset	This is the reset pin. It resets the counter by applying a pulse with a width of 30 ns.
85	B8	Out1_src	This is the output of SA-SRC number 1.
84	C8	Out2_src	This is the output of SA-SRC number 2.
83	A9	Out3_src	This is the output of SA-SRC number 3.
82	B9	Out4_src	This is the output of SA-SRC number 4.
81	A10	Out5_src	This is the output of SA-SRC number 5.
79	A11	Out6_src	This is the output of SA-SRC number 6.
78	B11	Out7_src	This is the output of SA-SRC number 7.
74	C12	Out8_src	This is the output of SA-SRC number 8.
72	C13	Out9_src	This is the output of SA-SRC number 9.
71	D12	Out10_src	This is the output of SA-SRC number 10.
70	D13	Out11_src	This is the output of SA-SRC number 11.
69	E12	Out12_src	This is the output of SA-SRC number 12.
68	E13	Out13_src	This is the output of SA-SRC number 13.
67	F11	Out14_src	This is the output of SA-SRC number 14.
66	F12	Out15_src	This is the output of SA-SRC number 15.
65	F13	Out16_src	This is the output of SA-SRC number 16.
88	C7	Vdd!	This is the power pin used for the cell.
89	A7	VDDOR2	This is the power pin used for the pad.
90	A6	gnd!	This is the ground pin for the cell.

Figure A.7: The pin list of the SA-SRC cell and its description.

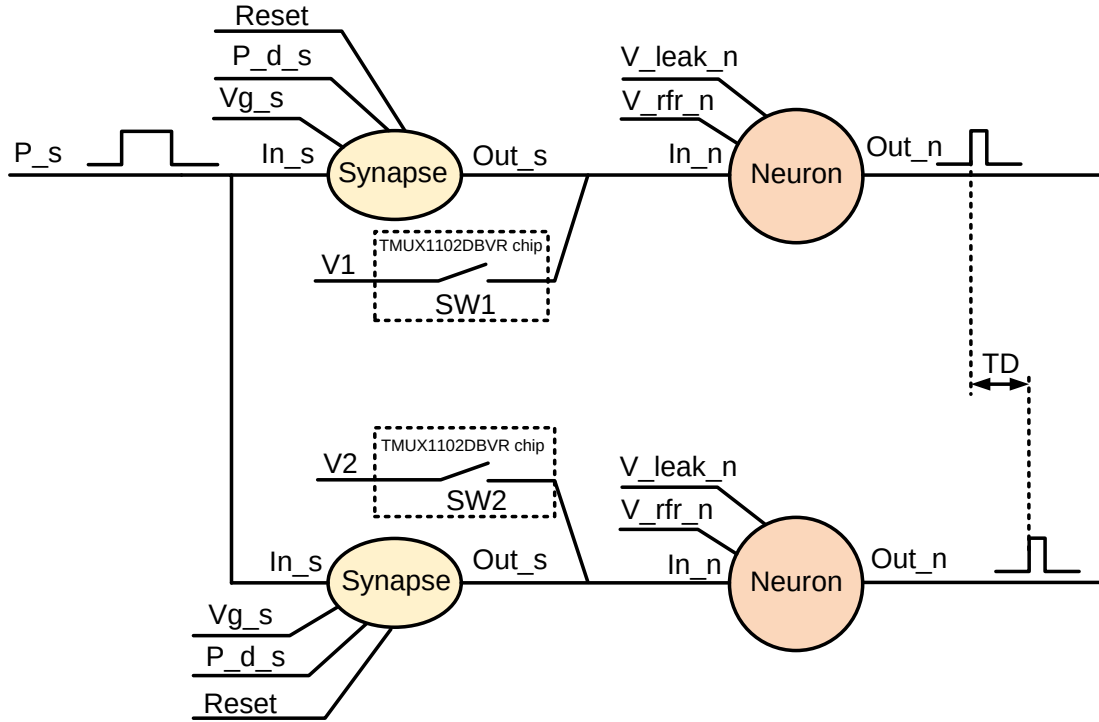


Figure A.8: The proposed Adaptive Sensor Signal-to-Spike Converter (ASSC) is depicted in the block diagram, including labeled pin names. The ASSC comprises two primary components: two synapses and two neurons. The synaptic inputs are shared, with each synapse transmitting its output to a corresponding neuron. Additionally, each neuron is connected to a dedicated switch (TMUX1102DBVR chip), which interfaces with the V1 and V2 input terminals. p_{d_s} serves as the clock for the synapse counter, incrementing by one with each pulse, up to 255. The ASSC operates in two phases: first, switches SW1 and SW2 charge the neuron membrane capacitors to V1 and V2. Then, the switches turn off, and a timed pulse (P_s) finalizes integration, driving neurons to the activation threshold and generating spikes.

Appendix B

Appendix B provides an architectural breakdown of the Jeffress model. It is included to motivate and justify the adoption and adaptation of this model within the context of the thesis, highlighting the rationale behind its implementation and modification for neuromorphic hardware. The Jeffress Model has two inputs and consists of two parts: a left part and a right part. The two inputs enter the left part from the top and bottom sides, respectively, while in the right part, the inputs enter oppositely. Specifically, the first input enters the left side from the top, and it enters the right side from the bottom. The second input enters both the left and right sides, but on opposite paths compared to the first input.

The left and right ears receive the sound simultaneously. The signals are balanced so that they arrive at the central tertiary fiber 4 at the same time, causing it to fire in both the right and left auditory tracts.

The left ear receives the sound slightly earlier than the right. The signal from the left ear travels along a longer neural path, while the right-ear signal takes a shorter route. As a result, both signals arrive simultaneously at coincidence detectors 5 or 6 in the left auditory tract and atcoincidence detectors 2 or 3 in the right auditory tract, causing these coincidence detectors to fire.

The left ear receives the sound much earlier than the right. The signal from the left ear travels along a significantly longer path, while the right-ear signal takes the shortest possible route. As a result, coincidence detectors 7 in the left auditory tract and coincidence detectors 1 in the right auditory tract fire.

The right ear receives the sound slightly earlier than the left. As a result, coincidence detectors 3 or 2 in the left auditory tract and coincidence detectors 5 or 6 in the right auditory tract fire, indicating that the sound source is slightly to the right.

The right ear receives the sound much earlier than the left. As a result, coincidence detectors 1 in the left auditory tract and coincidence detectors 7 in the right auditory tract fire.

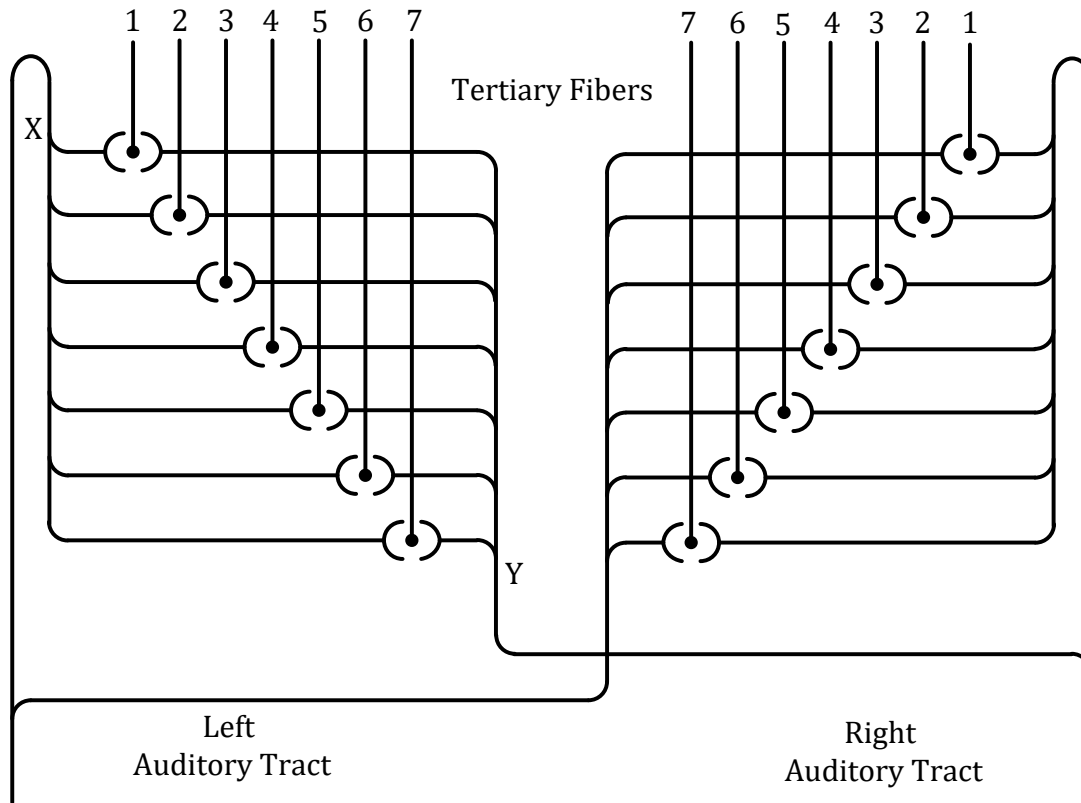


Figure B.1: Jeffress Model [207]

In the paper, 14 coincidence detectors were used to cover a time difference range of 0.5 ms between the right and left ears, with a step size of 0.1 ms. A group of coincidence detectors from both the right and left auditory tracts fires at each step.

The Jeffress model can generate approximately five distinct codes to represent the time difference using 14 coincidence detectors. As mentioned in the paper, in order to increase the time difference range, the delay chain must be extended.

The Jeffress model of sound localization is based on a place-coding principle that relies on whether specific neurons fire or not, depending on the timing difference between signals arriving from the left and right ears. When the sound reaches both ears simultaneously (0.0 ms interaural time difference), the signals converge on the central coincidence detector 4 in both the left and right auditory tracts, causing it to spike. If the left ear receives the sound slightly earlier by 0.1 ms, the signal from the left travels through a longer delay path, and coincidence occurs at coincidence detectors 5 or 6 in

the left tract and coincidence detectors 2 or 3 in the right tract. When the left ear leads by 0.2 ms, the delay compensation causes coincidence detector 7 in the left tract and coincidence detector 1 in the right tract to fire. Conversely, if the right ear receives the sound 0.1 ms earlier, coincidence detectors 3 or 2 in the left tract and coincidence detectors 5 or 6 in the right tract are activated. Finally, when the right ear leads by 0.2 ms, the firing shifts to coincidence detector 1 in the left tract and coincidence detector 7 in the right tract.

ITD (ms)	Sound Arrives Earlier At	Left Tract CD Firing	Right Tract CD Firing
0	Same time (center)	4	4
0.1	Left ear	5 or 6	2 or 3
0.2	Left ear	7	1
-0.1	Right ear	3 or 2	5 or 6
-0.2	Right ear	1	7

Table B.1: Interaural time difference (ITD) and coincidence detector (CD) response in Jeffress Model

B.1 Architectures for Sound Localization

Three new architectures are proposed as outlined below. The first architecture (Point 1) emulates the Jeffress model. The second architecture (Point 2) models only one side of the Jeffress model. The third architecture (Point 4) is a hybrid that combines elements of the Jeffress model with the Kammara model. Only the third model has been simulated so far, as shown below. The first and second models have been analysed based on the Jeffress model as described in his paper, "A Place Theory of Sound Localization."

These three architectures are based on the ACD (Adaptable Computational Device) design presented in the thesis. They demonstrate how the ACD can be adapted and reused in the development of new architectures. Unlike the original design in the thesis, which requires only the ACD, these new architectures, as well as the Kammara model, also require delay units. The inclusion of delay units increases area and power consumption, adds complexity to the overall design, and introduces uncertainty. Therefore, the delay units must be adaptable to compensate for variations and deviations.

B.1.1 Jeffress model

According to the Jeffress Model, when both inputs arrive simultaneously, outputs out-4-L and out-4-R should activate and generate spikes. Additionally, if the first input arrives slightly earlier than the second, their signals can still reach the same time at ACD 5 or 6 on the left side and at ACD 2 or 3 on the right side, triggering those ACDs to fire. The design shown in Figure B.2 is proposed to emulate the behaviour of the Jeffress Model.

According to the Jeffress model described in his paper 'A Place Theory of Sound Localization' (B.1), the design shown in Figure B.2 can generate seven codes in total, which corresponds to 2.8 bits in binary representation. To increase the number of codes, both the chain delay and the number of ACDs must be increased. Each additional code requires two more ACDs and four additional delay units.

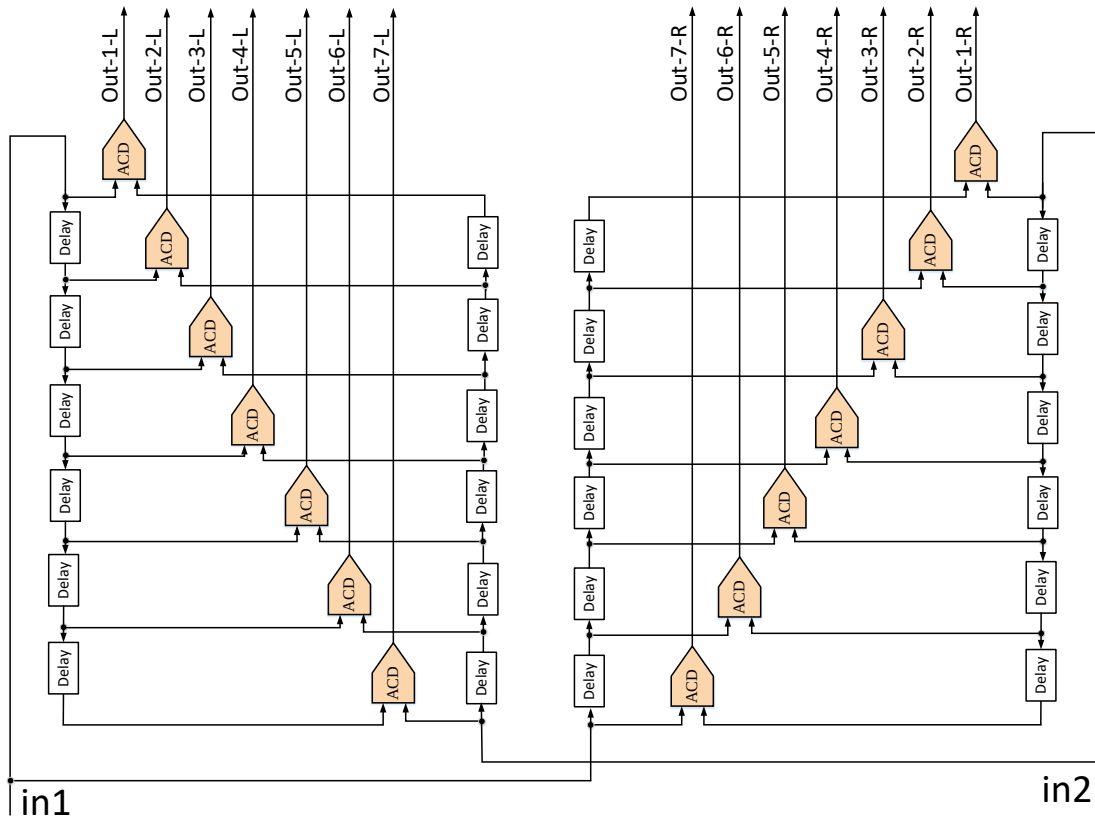


Figure B.2: Architectural representation of the proposed Jeffress Model

B.1.2 Jeffress-One-Side Modell

Since the right and left auditory pathways in the Jeffress model are symmetrical, it is sufficient to model only one side, eliminating the need for four delay lines. Therefore,

an architecture that models a single side of the Jeffress model is proposed, as shown in Figure B.3. The proposed design can generate a total of seven codes, equivalent to 2.8 bits in binary representation. To increase the number of codes, both the chain delay and the number of ACDs must be increased. Each additional code requires one more ACD and one additional delay unit.

B.1.3 Kammara's model

He changed the Jeffress model. In the original Jeffress model, the two inputs enter the left side from the top and bottom, while in the right side, the inputs enter in the opposite manner. In Kammara's model, however, both inputs enter from the left side in both parts. Additionally, he used two delay chains instead of the four used in the Jeffress model. Furthermore, the Kammara model relies on a wide ACD window for rank assignment, as shown in Figure B.4, whereas the Jeffress model with delay chains operates using a narrower ACD window. In the Kammara model, increasing the number of codes requires increasing both the chain delay and the number of ACDs. Each additional code requires one more ACD and one additional delay unit.

B.1.4 Hybrid Model

Here, a new model is proposed. This model is designed using the ACD described in the thesis, which has the ability to adapt its window size. It combines the Jeffress and Kammara models. The architecture from Kammara's model is used, where both inputs enter from the left side in both sections, and two delay chains are incorporated. In this new model, the adaptive ACD mechanism from the thesis is applied to narrow the ACD window, similar to the approach in the Jeffress model.

From the Table B.2, the design with delay shown in Figure B.5 can generate eight codes when in2 precedes in1, as indicated in Table B.2. Similarly, the design in Figure B.5 generates another eight codes when in1 precedes in2. This results in a total of 16 distinct codes within the ACD window, which is 10 ns, corresponding to 4 bits in binary representation. To increase the number of codes, it is necessary to increase both the chain delay and the number of ACDs. Each additional code requires one more ACD and one more delay unit.

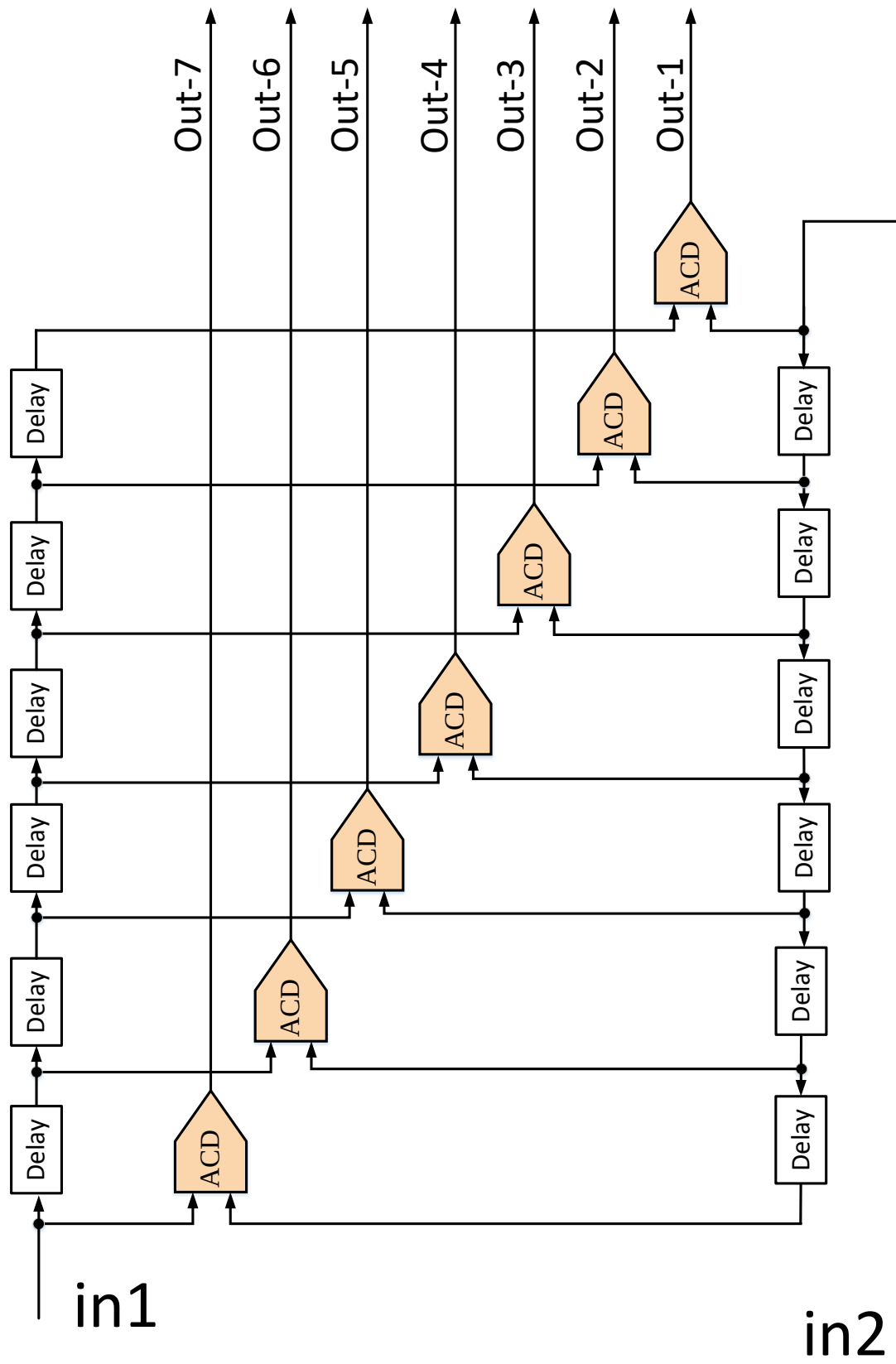


Figure B.3: Proposed architecture of the Jeffress One-Sided model

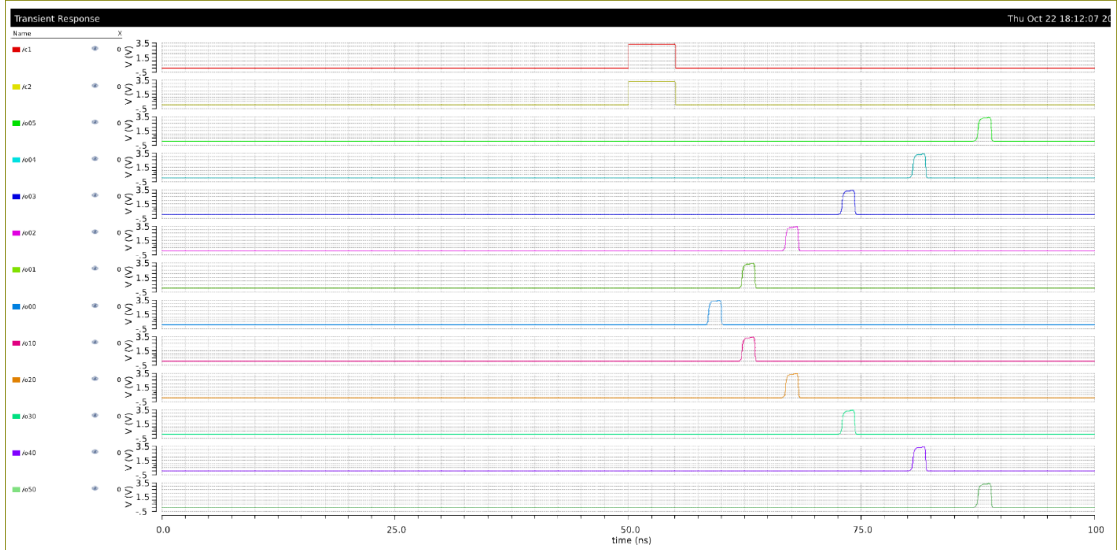


Figure B.4: Output corresponding to a 0 ns time difference between incoming pulses (Figure 6.8, Kammara's thesis) [76].

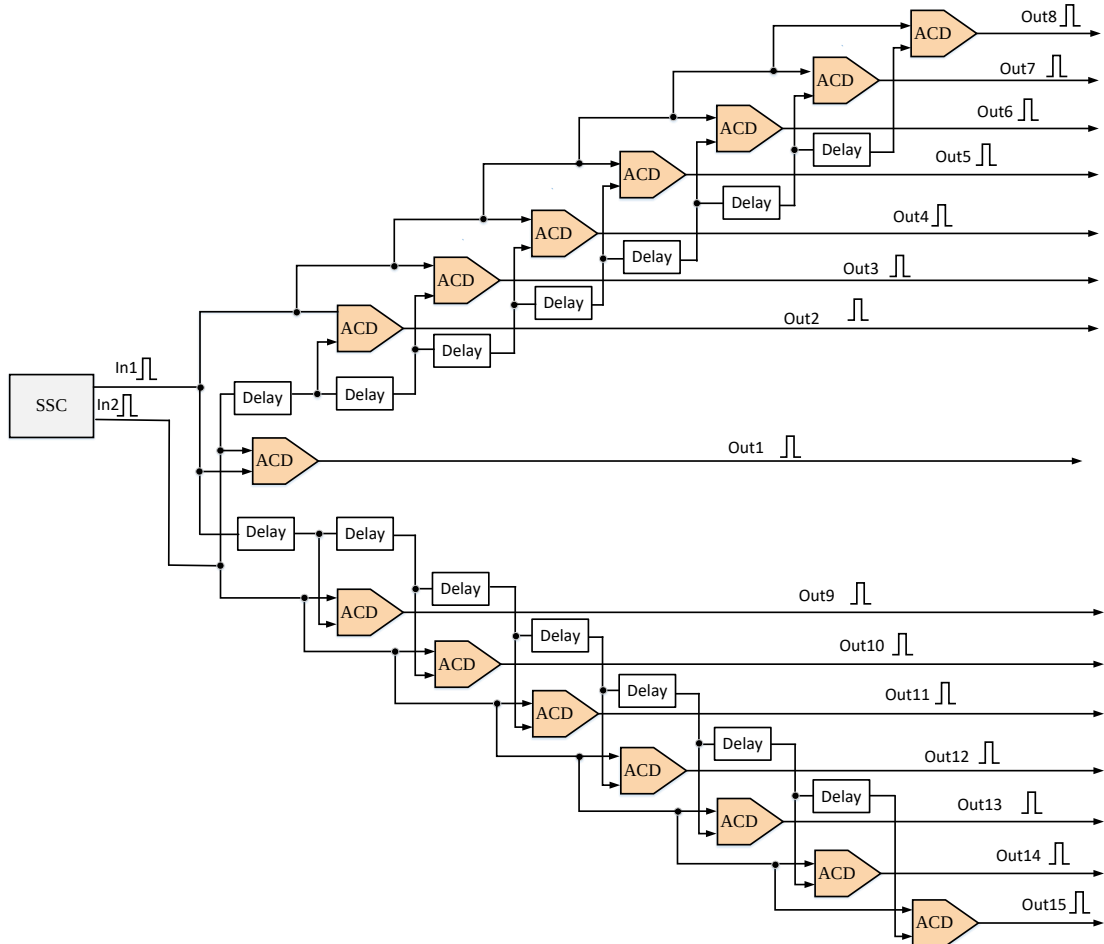


Figure B.5: Proposed architecture inspired by the Jeffress model and Kammara model .

B.1.5 Thesis Model

The model in the thesis has two parts, where the architecture is built using ACDs without delay units in order to save area and power. The design presented in the thesis generates

	15 ns	30 ns	45 ns	60 ns	75 ns	90 ns	105 ns	120 ns
Out1	0	0	0	0	0	0	0	0
Out2	1	1	0	0	0	0	0	0
Out3	0	2	2	0	0	0	0	0
Out4	0	0	3	3	0	0	0	0
Out5	0	0	0	4	4	0	0	0
Out6	0	0	0	0	5	5	0	0
Out7	0	0	0	0	0	6	6	0
Out8	0	0	0	0	0	0	7	7
Out9	0	0	0	0	0	0	0	0
Out10	0	0	0	0	0	0	0	0
Out11	0	0	0	0	0	0	0	0
Out12	0	0	0	0	0	0	0	0
Out13	0	0	0	0	0	0	0	0
Out14	0	0	0	0	0	0	0	0
Out15	0	0	0	0	0	0	0	0
Out16	0	0	0	0	0	0	0	0

Table B.2: Showing the output spike order corresponding to Figure B.5, where in2 precedes in1. The Table indicates the sequence of firing outputs to identify which output occurred first, second, and so on.

eight codes when in2 precedes in1, as shown in Table B.3, Table B.4, and another eight codes when in1 precedes in2 as shown in Table B.5, Table B.6. This results in a total of 16 distinct codes within the ACD window, which is 240 ns, corresponding to 4 bits in binary representation. However, to increase the number of codes in this design, only the number of ACDs needs to be increased, one additional ACD per added code, with no need for extra delay units. As a result, the chip area required for the thesis design is smaller than that of the design in Figure B.5, due to the absence of delay units. Additionally, the design in Figure B.5 consumes more power because of the delay units.

B.2 Quantitative Comparison of the Jeffress, Hybrid, and Thesis Models

To enable a clear and quantitative comparison, the adaptive delay unit used in the Jeffress and Hybrid Models was designed as shown in Figure B.6. This unit consumes 74.25 μm of power and occupies an area of 0.044 mm^2 .

	7 ns	15 ns	22 ns	30 ns	37 ns	45 ns	52 ns	60 ns
Out1	1	1	1	1	1	1	1	1
Out2	3	3	2	2	2	2	2	2
Out3	5	5	4	4	3	3	3	3
Out4	7	7	6	6	5	5	4	4
Out5	9	9	8	8	7	7	6	6
Out6	11	11	10	10	9	9	8	8
Out7	13	13	12	12	11	11	10	10
Out8	15	15	14	14	13	13	12	12
Out9	2	2	3	3	4	4	5	5
Out10	4	4	5	5	6	6	7	7
Out11	6	6	7	7	8	8	9	9
Out12	8	8	9	9	10	10	11	11
Out13	10	10	11	11	12	12	13	13
Out14	12	12	13	13	14	14	14	14
Out15	14	14	15	15	15	15	15	15
Out16	16	16	16	16	16	16	16	16

Table B.3: Output spike order corresponding to the design presented in the thesis, where in2 precedes in1. The numbers in the Table indicate the spike order relative to the other outputs.

	67 ns	75 ns	82 ns	90 ns	97 ns	105 ns	112 ns	120 ns
Out1	1	1	1	1	1	1	1	1
Out2	2	2	2	2	2	2	2	2
Out3	3	3	3	3	3	3	3	3
Out4	4	4	4	4	4	4	4	4
Out5	5	5	5	5	5	5	5	5
Out6	7	7	6	6	6	6	6	6
Out7	9	9	8	8	7	7	7	7
Out8	11	11	10	10	9	8	8	8
Out9	6	6	7	7	8	9	9	9
Out10	8	8	9	9	10	10	10	10
Out11	10	10	11	11	11	11	11	11
Out12	12	12	12	12	12	12	12	12
Out13	13	13	13	13	13	13	13	13
Out14	14	14	14	14	14	14	14	14
Out15	15	15	15	15	15	15	15	15
Out16	16	16	16	16	16	16	16	16

Table B.4: Output spike order corresponding to the design presented in the thesis, where in2 precedes in1. The numbers in the Table indicate the spike order relative to the other outputs.

B.2.1 Hardware Requirements for 4-bit Resolution

The power is calculated by measuring the average current from the simulation and multiplying it by Vdd. The areas of the Jeffress Model and the Hybrid Model are determined by summing the area of each cell in the delay unit, then adding 20% to account for wire

	7 ns	15 ns	22 ns	30 ns	37 ns	45 ns	52 ns	60 ns
Out1	2	2	3	3	4	4	5	5
Out2	4	4	5	5	6	6	7	7
Out3	6	6	7	7	8	8	9	9
Out4	8	8	9	9	10	10	11	11
Out5	10	10	11	11	12	12	13	13
Out6	12	12	13	13	14	14	14	14
Out7	14	14	15	15	15	15	15	15
Out8	16	16	16	16	16	16	16	16
Out9	1	1	1	1	1	1	1	1
Out10	3	3	2	2	2	2	2	2
Out11	5	5	4	4	3	3	3	3
Out12	7	7	6	6	5	5	4	4
Out13	9	9	8	8	7	7	6	6
Out14	11	11	10	10	9	9	8	8
Out15	13	13	12	12	11	11	10	10
Out16	15	15	14	14	13	13	12	12

Table B.5: Output spike order corresponding to the design presented in the thesis, where in1 precedes in2. The numbers in the Table indicate the spike order relative to the other outputs.

	67 ns	75 ns	82 ns	90 ns	97 ns	105 ns	112 ns	120 ns
Out1	6	6	7	7	8	9	9	9
Out2	8	8	9	9	10	10	10	10
Out3	10	10	11	11	11	11	11	11
Out4	12	12	12	12	12	12	12	12
Out5	13	13	13	13	13	13	13	13
Out6	14	14	14	14	14	14	14	14
Out7	15	15	15	15	15	15	15	15
Out8	16	16	16	16	16	16	16	16
Out9	1	1	1	1	1	1	1	1
Out10	2	2	2	2	2	2	2	2
Out11	3	3	3	3	3	3	3	3
Out12	4	4	4	4	4	4	4	4
Out13	5	5	5	5	5	5	5	5
Out14	7	7	6	6	6	6	6	6
Out15	9	9	8	8	7	7	7	7
Out16	11	11	10	10	9	8	8	8

Table B.6: Output spike order corresponding to the design presented in the thesis, where in1 precedes in2. The numbers in the Table indicate the spike order relative to the other outputs.

connections. The area of each cell is obtained from its layout by multiplying its width by its length. For a 4-bit implementation, the resource requirements and hardware costs of the three models are as follows:

- **Jeffress Model:**

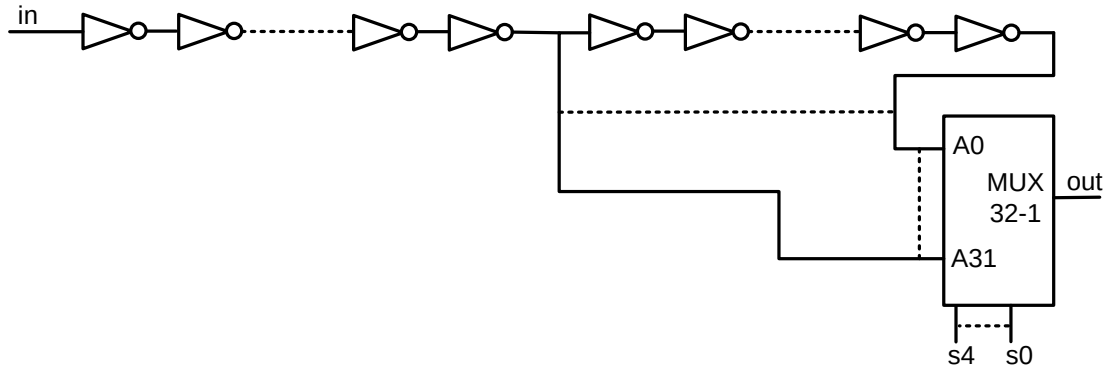


Figure B.6: Adaptive delay unit.

- Requires 32 ACDs and 64 adaptive delay units.
- Total area: 4.768 mm²
- Total power consumption: 5.349 mW
- Uses 1-of-N encoding

- **Hybrid Model:**

- Requires 16 ACDs and 16 adaptive delay units.
- Total area: 1.680 mm²
- Total power consumption: 1.486 mW
- Uses 1-of-N encoding

- **Thesis Model:**

- Requires only 16 ACDs with no adaptive delay units.
- Total area: 0.975 mm²
- Total power consumption: 0.297 mW
- Uses spike order (rank) coding

B.2.2 Comparative Advantages and Efficiency of the Thesis Model

Compared to the other two models, the Thesis Model offers significant reductions in both area and power consumption:

- Area reduced by approximately 79.5% compared to the Jeffress Model and 41.9% compared to the Hybrid Model.

- Power consumption reduced by approximately 94.4% compared to the Jeffress Model and 80.0% compared to the Hybrid Model.

In terms of area and power efficiency per bit of resolution:

- Approximately $5\times$ less area per bit and $18\times$ less power per bit than the Jeffress Model.
- Approximately $1.7\times$ less area per bit and $5\times$ less power per bit than the Hybrid Model.

These results confirm the scalability and efficiency of the Thesis Model, making it a practical and scalable solution for hardware implementations where area and energy constraints are critical.

B.2.3 Resource Composition per Processing Stage

All three models use 8 processing stages to achieve 4-bit resolution, but the resource composition of each stage differs significantly:

- **Jeffress Model:** 4 ACDs + 8 delay units per stage; high area and power overhead.
- **Hybrid Model:** 2 ACDs + 2 delay units per stage; more efficient but still reliant on analog delays.
- **Thesis Model:** Only 2 ACDs per stage; no delay units; minimal complexity, area, and energy.

B.2.4 Summary and Practical Implications

The Thesis Model's efficient spike order coding and simplified hardware design lead to improvements in area and power consumption without sacrificing resolution. This makes it suitable for systems where physical space and energy constraints are paramount. The consistent stage count across models highlights that the Thesis Model's advantage lies in its leaner resource use per stage, making it a practical and scalable solution for future neuromorphic hardware designs.

Metric	Jeffress	Hybrid	Thesis
Resolution (bits)	4	4	4
Number of Stages	8	8	8
Total ACDs	32	16	16
Total Delay Units	64	16	0
Area (mm ²)	4.768	1.680	0.975
Power (mW)	5.349	1.486	0.297
Area per Bit (mm ² /bit)	1.192	0.420	0.244
Power per Bit (mW/bit)	1.337	0.372	0.074
ACDs per Stage	4	2	2
Delay Units per Stage	8	2	0
Stage Size (ACDs + Delays)	12	4	2

Table B.7: Comparison of Area, Power, and Stage Resource Requirements for 4-Bit Resolution

B.3 Scalability of the ACD Chain for Extended Temporal Resolution in SA-SRC Architecture

The SA-SRC generates spike sequences that represent the temporal difference between two input spikes (in1 and in2), with the current input time range spanning 120 ns. The proposed solution is inherently scalable to accommodate longer ACD chains. To achieve this, the ACD coincidence window needs to be extended to cover the temporal span of the SA-SRC inputs. Simulation results confirm this scalability: by reducing the leakage voltage V_{LEAK} from 0.8 V to 0.55 V, the coincidence window of the ACD chain can be extended from 600 ns up to 60,600 ns. This demonstrates the feasibility of scaling the architecture to support higher resolution, such as six-bit configurations.

B.3.1 Extension of the Design to a 6-bit

To evaluate the scalability of the design, the architecture was extended to a 6-bit resolution, focusing on the positive side of the ACD array, as illustrated in Figure B.7. Only the positive array was designed in this extension to reduce simulation time. Also, the ACD window was extended to 600 ns. Figure B.8 and Figure B.9 present the simulation results for a test case where input signal in2 arrives before in1.

The architecture was then extended to a 6-bit resolution for both the positive and negative sides of the ACD array, as illustrated in Figure B.10. Figure B.11 presents the simulation results for a test case in which the input signal in1 arrives before in2

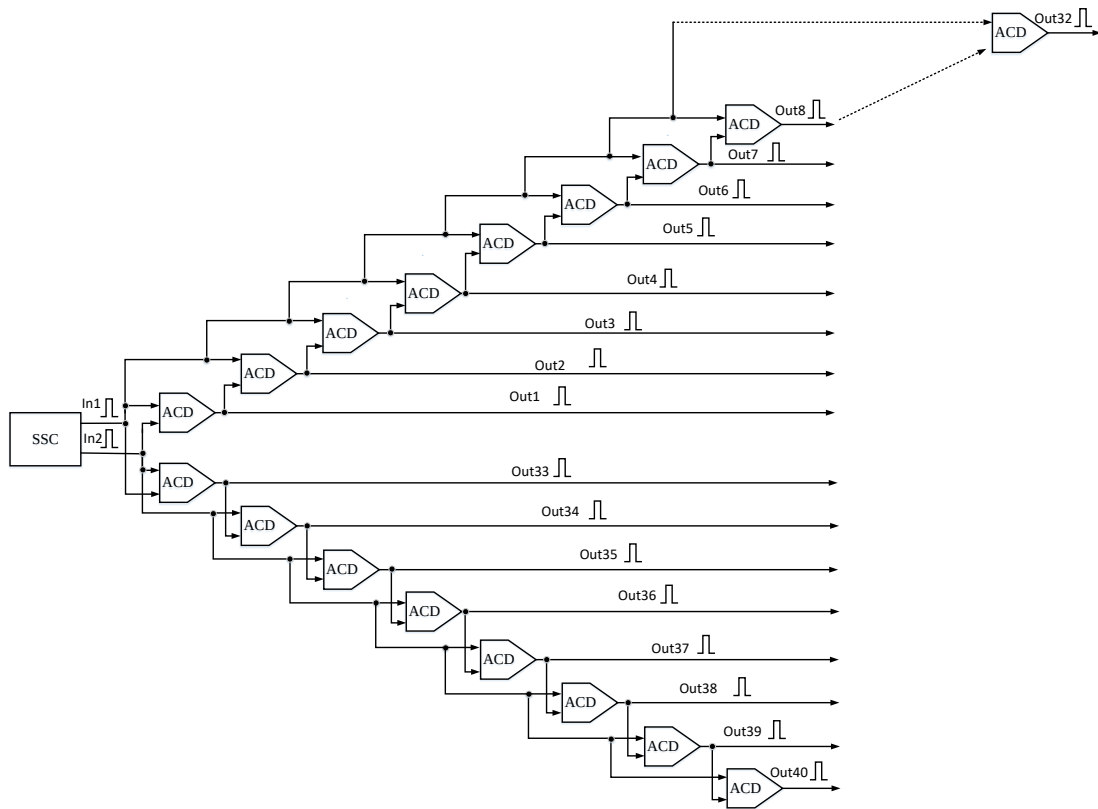


Figure B.7: Architecture of the extended 6-bit positive ACD array used for evaluating design scalability.

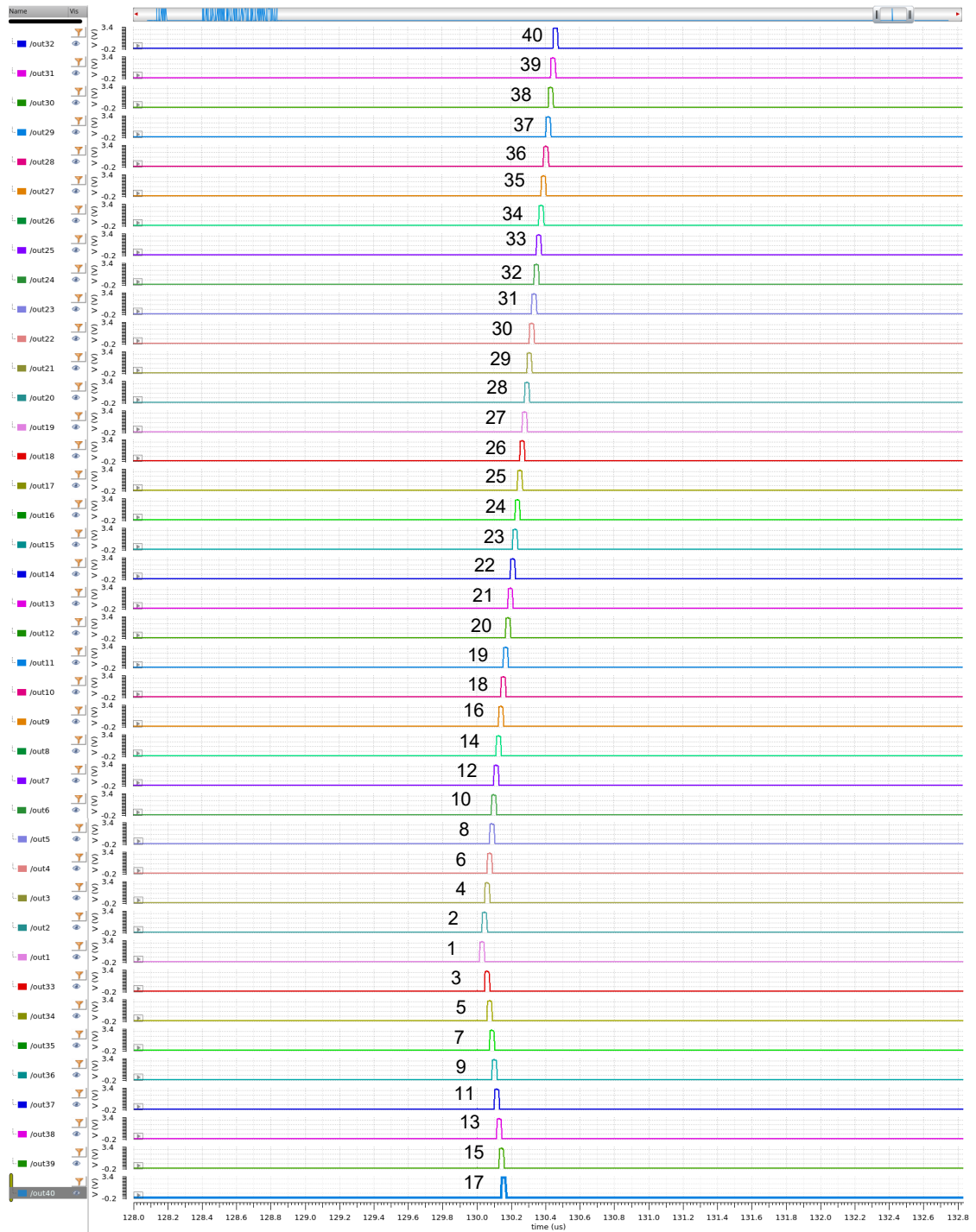


Figure B.8: Simulation results showing the system response when input in2 precedes input in1 by 30 ns.

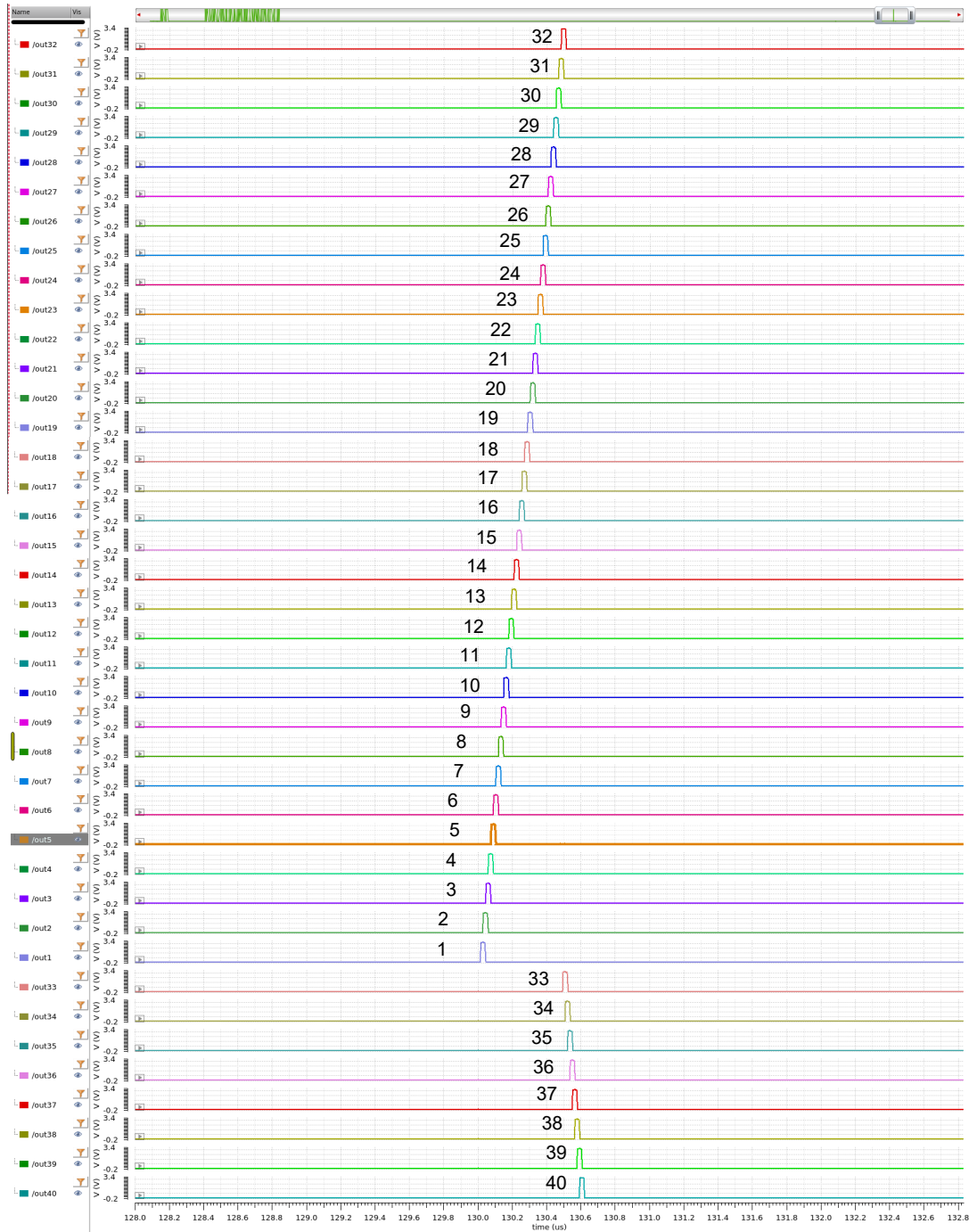


Figure B.9: Simulation results showing the system response when input in2 precedes input in1 by 480 ns.

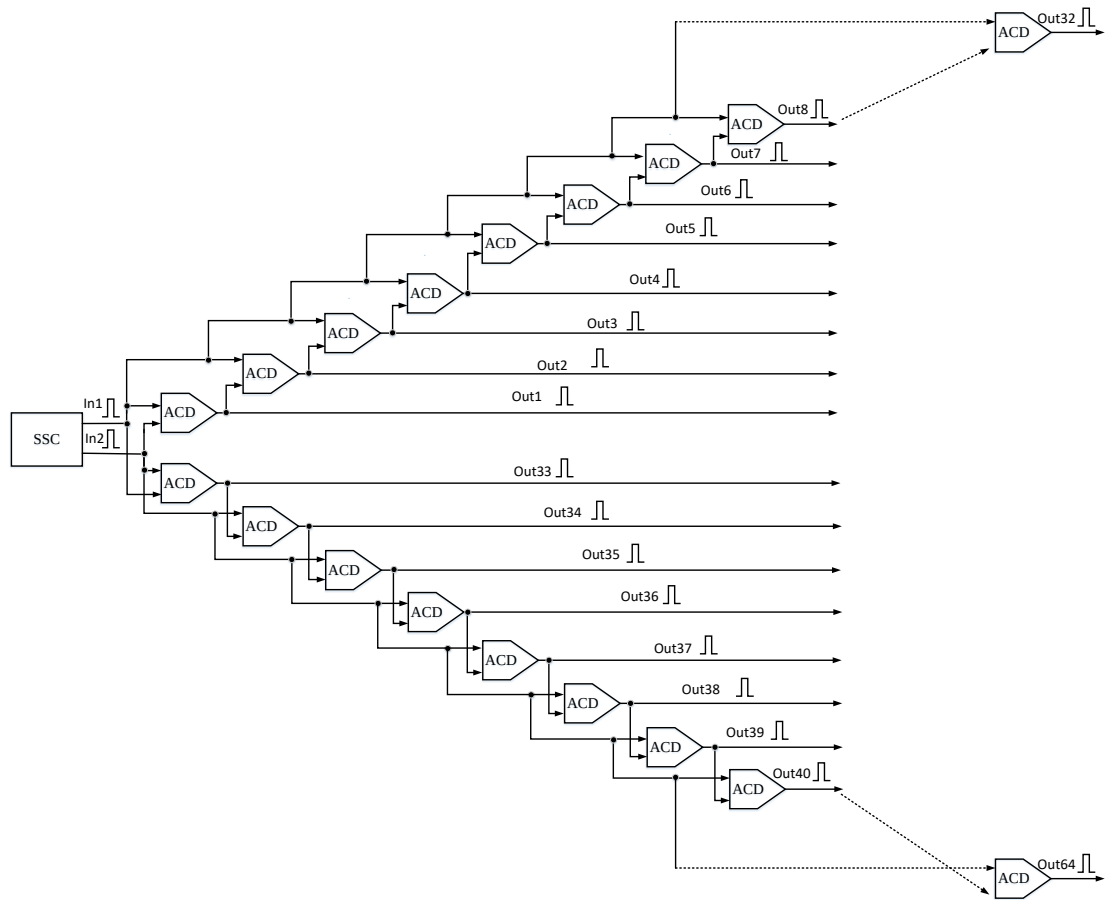


Figure B.10: Architecture of the extended 6-bit design for both the positive and negative sides of the ACD array, used to evaluate design scalability.

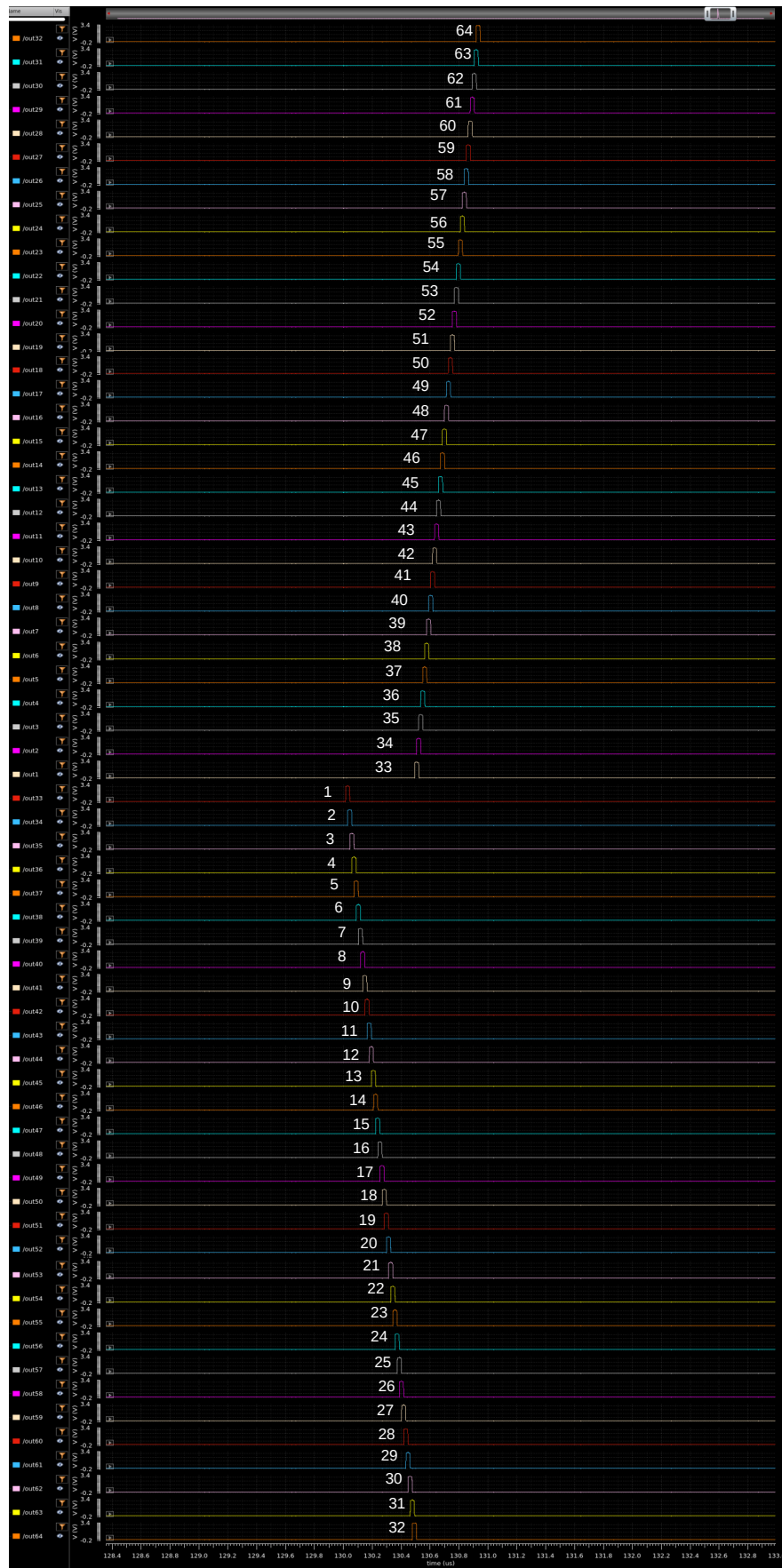


Figure B.11: Simulation results showing the system response when input in1 precedes input in2 by 480 ns.

Appendix C

Curriculum Vitae

Hamam Abd

Education

- **PhD in Electrical Engineering**, RPTU, Kaiserslautern, Germany (2019 – 2025)
- **MSc in Electrical Engineering**, TU Kaiserslautern, Germany (2009 – 2012)
- **BS in Electronics Engineering**, Mosul University, Iraq (2002 – 2006)

Areas of Interest

- xCMOS mixed-signal circuit design
- IC layout engineering
- Neuromorphic systems
- Spiking neural networks
- Bio-inspired integrated
- Intelligent sensor systems
- Digital system design

- Self-X adaptive spiking
- Sensory systems
- Power electronics.
- Electrical Measurement and Instrumentation

Research Publications (Selected)

1. Abd, H. and König, A., 2020. A compact four transistor CMOS-design of a floating memristor for adaptive spiking neural networks and corresponding self-X sensor electronics to industry 4.0. *tm-Technisches Messen*, 87(s1), pp.s91-s96.
2. Abd, H. and König, A., 2021. Adaptive Spiking Sensor System Based on CMOS Memristors Emulating Long and Short-Term Plasticity of Biological Synapses for Industry 4.0 Applications. *tm-Technisches Messen*, 88(s1), pp.s114-s119.
3. Abd, H. and König, A., 2022. Design of a CMOS memristor emulator-based, self-adaptive spiking analog-to-digital data conversion as the lowest level of a self-x hierarchy. *Journal of Sensors and Sensor Systems*, 11(2), pp.233-262.
4. Alraho, S., Zaman, Q., Abd, H. and König, A., 2022. Integrated sensor electronic front-ends with self-x capabilities. *Chips*, 1(2), pp.83-120.
5. Abd, H. and König, A., 2023. On-Chip Adaptive Implementation of Neuromorphic Spiking Sensory Systems with Self-X Capabilities. *Chips*, 2(2), pp.142-158.
6. Abd, H. and König, A., 2023. Characterization of Adaptive Implementation of Neuromorphic Spiking Sensory Systems On-Chip with Self-X Abilities: Charakterisierung der adaptiven Implementierung von neuromorphen Spiking-Sensoriksystemen auf einem Chip mit Selbst-X-Fähigkeiten. *tm-Technisches Messen*, 90(s1), pp.126-131.
7. Abd, H., Zaman, Q., Alraho, S. and König, A., 2024. Neuromorphic Spiking Sensory System with Self-X Capabilities. *IEEE Access*.