Application study: RRAM for Low-Power Microcontrollers

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***Abstract*—The energy efficiency of today's microcontrollers is supported by the extensive usage of low-power mechanisms. A full power-down requires in many cases a complex, and maybe error prone, administration scheme, because data from the volatile memory have to be stored in a flash based back-up memory. New types of non-volatile memory, e.g. in RRAM technology, are faster and consumes a fraction of the energy compared to flash technology. This paper evaluates power gating for WSN with RRAM as back-up memory.**

I. Introduction

In wireless sensor networks many devices are distributed in a certain area. In most cases the battery determines the life time of these devices. A frequent replacement of the batteries can be avoided, if power saving strategies are well implemented in the sensor node.

Clock gating, as power saving mechanism, is responsible to avoid unnecessary dynamic switching activities. In operation mode parts of the ASIC, which are not in use, do not get the clock signal. Since the power supply is not switched off, every register keeps its value. This power saving approach is very common. The advantage of clock gating, that all cells are still powered on, is the disadvantage too. The cells have a static power consumption, the leakage. With further progress in down scaling the transistor size the leakage is increased. In older technologies, usually used for sensor nodes, the leakage does not have a strong effect on the power consumption (see Fig. 1). In the future, smaller technologies will be used in WSN and the leakage is getting an important factor in the power budget.

A typical microcontroller has different types of memories. A flash based memory is used to store the program. The power supply can be disconnected without loosing the operating system and application program. In addition to the program memory a data memory is required, which is implemented as SRAM. Therein contents of variables are written, which are necessary for complex programs, whereby the register file is not sufficient. The register file itself contains flip flops and it stores the program counter and some variables.

To support energy saving strategies most types of microcontrollers have different sleep modes. E.g. the MSP430, a microcontroller from TI [1], has the sleep modes LPM0 to LPM4. The difference between them is mostly the controlling of the three clock domains.

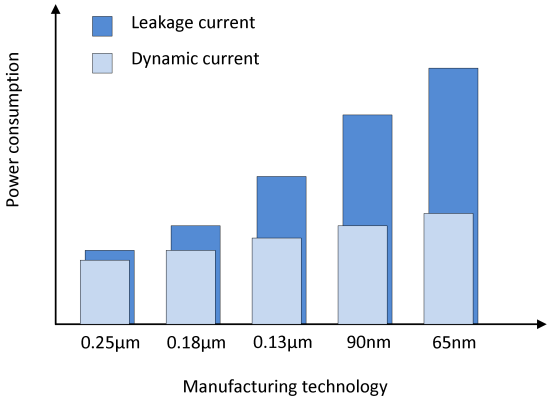

Fig. 1: Dynamic vs. static power consumption, depending on minimal transistor size

Furthermore the sleep modes LPM3.5 and LPM4.5 are implemented. In these deep sleep modes all volatile memories are disconnected from the power supply. So the content of SRAM and register file are lost. After wake-up the following start sequence is the same like after a regular power-on or a reset. E.g. measurement values stored in SRAM or variables into register files are lost, if they have not been saved in a flash memory before.

II. RRAM

The technical prerequisite to store an information as alterable resistor is known since 1960's [2]. But the integration into silicon-based ASICs is described in [3] for the first time in 2008. The RRAM memory type is a non-volatile memory with improved access time for write and read compared to flash memory. A single memory cell consists of a transistor and a alterable resistor (Fig. 2a). Such a resistor is very small and it is integrated into a via as shown in Fig 2b. Compared to a default via, which connects wires on different metalization layers, this via is modified with a a thin hafnium oxide layer. A defined current flow set or reset the bit value. The write operations are limited from 10^4 to 10^6 [4]. Above this value

the bit cell does not work reliable any more. The number of read cycles is not limited. The access time for write is between 10 and 30 μs and for read less than 20ns.

(a) Schematic

(b) Cross section of a via for RRAM purpose

Fig. 2: RRAM cell

III. Simulation

For IHP technology different memory types are available. In Tab. I an overview about the power consumption of every memory is given. The values are generated by analogue simulations for flip flop, SRAM and flash. For the RRAM memory the values are measurement values [5].

Memory type	Energy (write)	Energy (read)	Leakage
Flip flop in register file	0.195pWs	0.07pWs	250 pW
SRAM	10.7pWs	10.03pWs	45 pW
Flash	80,400pWs	31.25pWs	0 pW
RRAM	11,500pWs	8.04pWs	0 pW

TABLE I: Energy for write/read of a bit for different memory types in 0.25 μm technology

IV. Application Area

A possible application area of the RRAM is a back-up memory for all volatile memories in a microcontroller. To minimize the leakage of microcontrollers in current and future technologies, the usage of power gating mechanism has to be increased. As described in Sec. I the content of register file and data memory will be lost in case of power gating, which is used during long deep sleep mode. To avoid a full reboot of the system, the data has to be stored into an RRAM and restored after wake-up.

The goal is to save energy using the power gating technology. This means that the energy which is required to back-up the data has to be less than the leakage energy for the sleep time. For a back-up of a flip flop of the register file, the content of the flip flop has to be read and the value stored in the RRAM. After the sleep phase the value from the RRAM has to be read and copied to the flip flop. All these four operations require a energy of 11,508.3 pWs (see Tab. I). This amount of energy consumes a flip flop in 46 seconds for leakage. This means that the usage of RRAM as back-up memory in sleep periods greater than 46 seconds, saves energy. The same calculation with a flash as back-up memory results in a sleep period greater than 320 seconds.

For back-up one SRAM bit the break even point is reached after 256 seconds in deep sleep mode, because the leakage of the SRAM cell is smaller than for the flip flop.

The simulation in Tab. I shows that the required energy to store a bit value into a RRAM is less than for storage one bit in flash technology. Every single bit in an RRAM can be set or reset independent of any other. In a flash memory the whole block has to be erased at first. The effort for the data management is increased in this case. Furthermore the design of an RRAM memory block is less complex compared to a flash memory. The high voltage generator is not necessary and the complex structure of the transistor with a double gate is replaced by a transistor and a modified via. So an RRAM memory seems to be an ideal back-up memory for low-power microcontrollers.

V. Future Work

In current state the idea of RRAM as back-up memory is a case study only. For a real test scenario some steps are necessary. To back-up the data memory to an RRAM a type of DMA controller has to be implemented, which transfers the data from/to the RRAM automatically in case of entering a deep sleep mode. Alternatively the copy operations can be implemented in software. In contrast to program and data memory a register file is not direct accessible via internal data bus. So in a next step a module has to be implemented, which transfers the data to the RRAM and vice versa, and it has to be integrated into a microcontroller design.

Nevertheless the additional hardware consumes additional power. This point has to be considered during the evaluation. Furthermore a kind of partitioning can be implemented, whereby frequently written data are stored in a volatile memory and rarely written data stored into a RRAM.

VI. Conclusion

The work shows a possible approach for a power-saving strategy in the area of microcontrollers. RRAM as additional memory allows a fast entering of a very deep sleep mode, whereby the power can be switched off fully and the leakage is reduced to zero. The required time to store and restore the data from the RRAM and the required energy is low, so that an aggressive power saving strategy is possible. Even sleep times of less one minute are increasing the life time of the battery respectively the life time of the sensor node.

References

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